UXN6M9M Datasheet

9 GHz Divide-by-8 to 511 Programmable Integer Divider

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was the first publication of this document.

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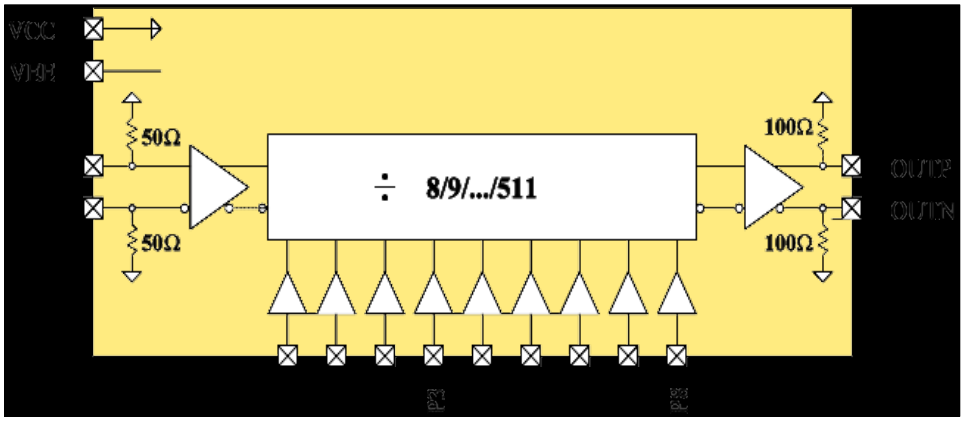
2 Product Overview

The UXN6M9M device is a highly programmable integer divider covering all integer divide ratios between 8 and 511.

The device features single-ended or differential inputs and outputs. Parallel control inputs are CMOS- and LVTTL-compatible for ease of system integration. The UXN6M9M device is packaged in a 40-pin, 6 mm × 6 mm leadless plastic surface mount package.

Figure 1 Functional Block Diagram



2.1 Applications

The UXN6M9M device can be used as a general-purpose, highly configurable divider in a variety of high-frequency synthesizer applications. Fast switching combined with a wide range of divide ratios make the UXN6M9M device an excellent choice for fractional-N and integer-N PLLs. Fractional division may be achieved by applying a sequence to the divider control lines, such as a delta-sigma modulated sequence.

2.2 Key Features

The following are key features of the UXN6M9M device:

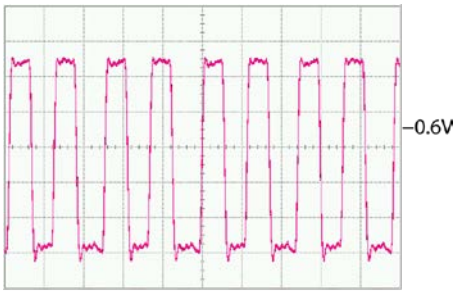
- Wide operating range: DC–9 GHz
- Contiguous divide ratios: 8 to 511
- Large output swings: >1 V_{PP}/side
- Single-ended and/or differential drive
- Size: 6 mm × 6 mm
- Parallel control lines
- Low-SSB phase noise: –147 dBc at 10 kHz offset

3 Functional Description

3.1 Frequency Divider Application

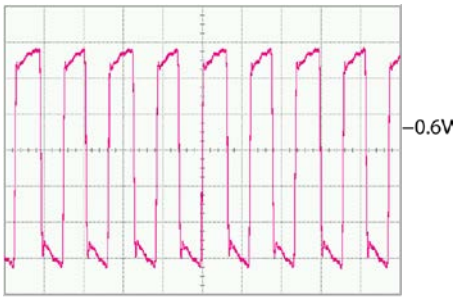
The following graphs show the frequency divider application of the UXN6M9M device.

Figure 2 Output Power (500 ps/DIV)



500 ps/DIV, 200mV/DIV

Figure 3 Output Power (1 ns/DIV)

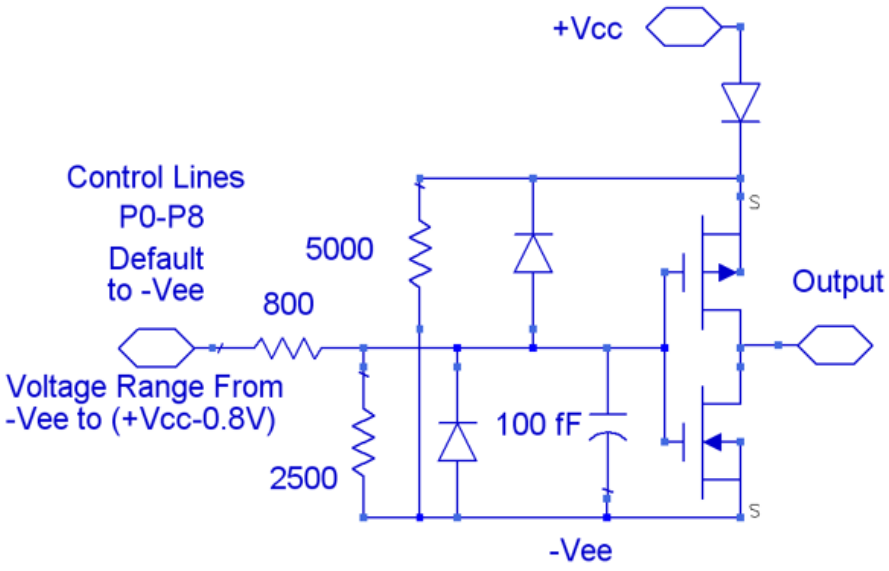


1 ns/DIV, 200mV/DIV

3.2 Control Logic

The following illustration shows the simplified control logic for the UXN6M9M device.

Figure 4 Simplified Control Logic Schematic



3.3 CML Logic Levels

The following table shows the CML logic levels for DC coupling for the UXN6M9M device, where temperature is 25 °C. The table below assumes 50 Ω terminations at inputs and outputs.

Table 1 CML Logic Levels for DC Coupling

	Parameter		Min	Typ	Max
Input	Differential	Logic input$_{HIGH}$ Logic input$_{LOW}$	V_{CC} V_{CC} – 0.05 V	V_{CC} V_{CC} – 0.3 V	V_{CC} V_{CC} – 1 V
	Single	Logic input$_{HIGH}$ Logic input$_{LOW}$	V_{CC} + 0.05 V V_{CC} – 0.05 V	V_{CC} + 0.3 V V_{CC} – 0.3 V	V_{CC} + 1 V V_{CC} – 1 V
Output	Differential and Single	Logic input$_{HIGH}$ Logic input$_{LOW}$	V_{CC} – 0.9 V V_{CC} – 1.1 V	V_{CC} + 0.6 V V_{CC} – 1.6 V	V_{CC} + 0.5 V V_{CC} – 1.7 V

The UXN6M9M achieves contiguous divisions by retiming the input controls for the divide ratio during each output cycle. This feature is fitting for applications where the divide ratio requires quick programmability, such as in fractional-N synthesizers. Figure 6 below is a representative diagram of how the part might be used in such an application is shown below. In this setup, the divider output is used to clock (or update) the control circuitry. The polarity of the output edge is chosen by the user depending on the relative timing of the control transitions to the output edge.

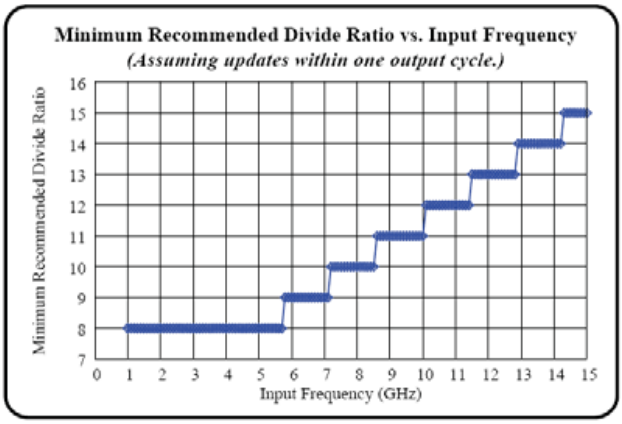
T setup as defined in the timing diagram is given by the following formula:

$$T\ setup = 4*T_{INPUT} + 0.7\ ns$$

where T_{INPUT} is the input period. Notice that for N = 8 and input frequencies above 6 GHz (T_{INPUT} < 165 ps), T setup exceeds the output period. Thus, an appropriate latency must be introduced to achieve proper updating. T_{HOLD} shows the region to avoid updating the control signal.

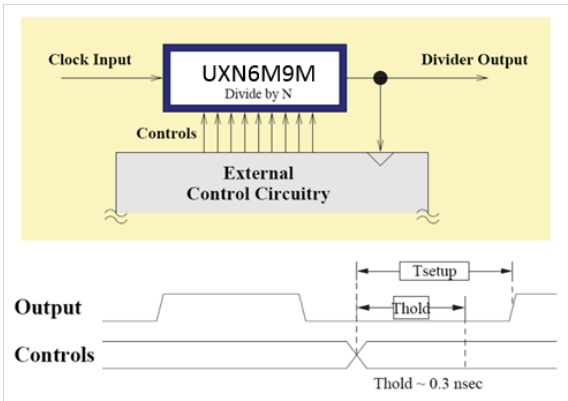
The chart in Figure 5 shows the recommended minimum divide ratios plotted against input frequency, assuming that the divide controls are updated within one output cycle of the output rising edge. This means for a given input frequency, all divide ratios above the minimum recommended divide ratio will achieve smooth divisions, whereas any divide ratio below the minimum may produce momentary errors. These values are a general guideline and may vary depending on the exact situation in which it is used.

Figure 5 Minimum Recommended Divide Ration vs. Input Frequency



The following diagram shows how the UXN6M9M can be used in applications where the divide ratio requires quick programmability.

Figure 6 Sample Use Case



4 Electrical Specifications

4.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the UXN6M9M device.

Table 2 Absolute Maximum Ratings

Parameter	Value	Unit
Supply voltage ($V_{CC} – V_{EE}$)	4	V
RF input power (INP, INN)	10	dBm
Operating temperature	–40 to 85	°C
Storage temperature	–85 to 125	°C
Junction temperature	125	°C

4.2 Electrical Characteristics

The following table shows the electrical characteristics of the UXN6M9M device at 25 °C, where V_{EE} = –3.3 V, I_{EE} = 340 mA, and Z_O = 50 Ω.

Table 3 Electrical Characteristics

Parameter	Description	Min	Typ	Max
F_{IN} (GHz)	Input frequency	DC[1]		14
P_{IN} (dBm)	Input power		0	9
P_{OUT} (dBm)	Output power		4	
PDC (W)	DC power dissipation		1.1	
θ_{JC} (°C/W)	Junction-case thermal resistance		14	

1. The low-frequency limit is dependent on input edge speed.

4.3 CMOS Levels

The following table shows the CMOS levels for the control line P0-P8 for the UXN6M9M device.

Table 4 CMOS Levels

Logic Level	Minimum	Typical	Maximum
1 (high)	V_{CC} – 1.25 V	V_{CC} – 0.8 V	V_{CC} – 0.8 V
0 (low)	V_{EE}	V_{EE}	V_{EE} + 1.25 V

5 Pin Descriptions

The following table describes the pins for the UXN6M9M device.

Table 5 Pin Descriptions

Port Name	Description	Notes
INP	Divider input, positive terminal	CML signal levels
INN	Divider input, negative terminal	CML signal levels
OUTP	Divider output, positive terminal	CML signal levels
OUTN	Divider output, negative terminal	CML signal levels
P0-P8	Divider modulus control (P8 = MSB)	CMOS levels, see Equation 1, defaults to logic 0
V_{CC}	RF and DC ground	The paddle is connected to $+V_{CC}$ inside the package
V_{EE}	–3.3 V at 340 mA	Negative supply voltage

Use the following equation below to find the divider modulus:

Equation 1: Divider Modulus = $N = P0 \cdot 20 + P1 \cdot 21 + P2 \cdot 22 + ... + P8 \cdot 28$ for $8 \le N \le 511$

The following table defines the pins for the UXN6M9M device.

Table 6 Pin Definitions

Pin	Function	Notes
5–7, 14, 24, 39, paddle (V_{CC})	RF and DC ground	0 V
2–4, 11, 17, 25, 36, 40 (V_{EE})	Negative supply voltage	Nominally 3.3 V
37 (INN)	Divider input	Negative terminal of differential input
38 (INP)	Divider input	Positive terminal of differential input
15 (OUTP)	Divider output	Positive terminal of differential output
16 (OUTN)	Divider output	Negative terminal of differential output
26 (P8)	Divide modulus control (MSB)	Defaults to logic 0, connect to V_{CC} –0.8 V for logic 1
27 (P7)	Divide modulus control	Defaults to logic 0, connect to V_{CC} –0.8 V for logic 1
28 (P6)	Divide modulus control	Defaults to logic 0, connect to V_{CC} –0.8 V for logic 1
29 (P5)	Divide modulus control	Defaults to logic 0, connect to V_{CC} –0.8 V for logic 1
30 (P4)	Divide modulus control	Defaults to logic 0, connect to V_{CC} –0.8 V for logic 1
31 (P3)	Divide modulus control	Defaults to logic 0, connect to V_{CC} –0.8 V for logic 1
32 (P2)	Divide modulus control	Defaults to logic 0, connect to V_{CC} –0.8 V for logic 1
33 (P1)	Divide modulus control	Defaults to logic 0, connect to V_{CC} –0.8 V for logic 1

Pin	Function	Notes
34 (P0)	Divide modulus control (LSB)	Defaults to logic 0, connect to V_{CC} –0.8 V for logic 1
Paddle (backside of package)	V_{CC} (heat sink)	Should be tied to V_{CC}. Paddle is also used for heat dissipation. Isolate the paddle from the ground if using a positive supply (V_{CC} = 3.3 V).

6 Package Information

6.1 Pad Metallization

The QFN package pad metallization consists of a 300 µin–800 µin (typical thickness 435 µin or 11.04 µm) 100% matte Sn plate. The plating covers a Cu (C194) leadframe.

The packages are manufactured with a >1hr 150 °C annealing/heat-treating process and matte (non-glossy) plating specifically to mitigate tin whisker growth.

6.2 ESD Sensitivity

Although SiGe ICs have robust electrostatic discharge (ESD) sensitivities, preventive ESD measures should be taken while storing, handling, and assembling this device.

Inputs are more ESD susceptible as they could expose the base of a BJT or the gate of a MOSFET. For this reason, all the inputs are protected with ESD diodes. These inputs have been tested to withstand voltage spikes up to 400 V.

6.3 Physical Characteristics

The following illustration and table show the physical characteristics of the UXN6M9M device.

Figure 7 Physical Characteristics

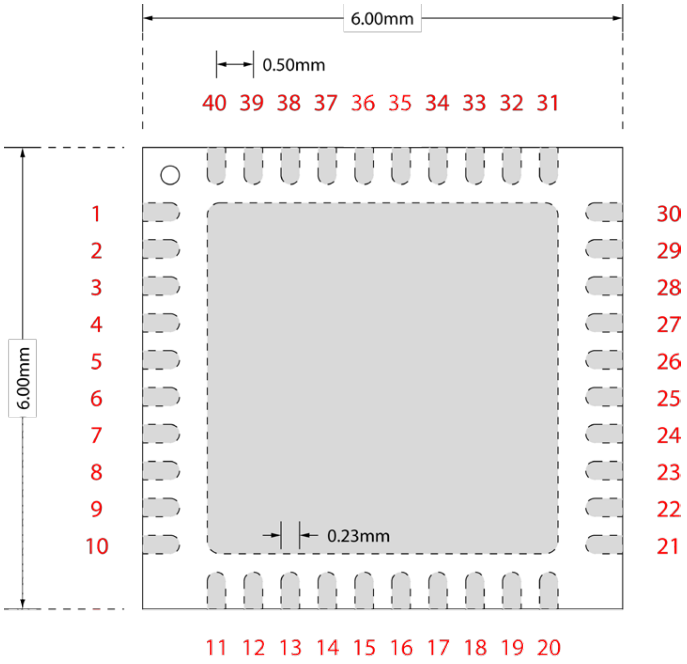


Table 7 Physical Dimensions

Parameter	Dimensions
Package size	6.00 mm × 6.00 mm
Package size tolerance	±0.25 mm
Package thickness	0.9 mm ±0.1 mm
Pad dimensions	0.23 mm × 0.4 mm
Center paddle	4.20 mm × 4.20 mm
JEDEC designator	MO-220

7 Design Guidelines

7.1 Low Frequency Operation

Low frequency operation is limited by external bypass capacitors and the slew rate of the input clock. The next paragraph shows the calculations for the bypass capacitors. If DC-coupled, the device operates down to DC for square-wave inputs. Sine-wave inputs are limited to approximately 50 MHz due to the 10 dBm maximum input power limitation.

The values of the coupling capacitors for the high-speed inputs and outputs (I/Os) are determined by the lowest frequency at which the IC will be operated.

$$C >> \frac{1}{2 \bullet \pi \bullet 50\Omega \bullet f_{lowest}}$$

For example, to use the device below 30 kHz, coupling capacitors should be larger than 0.1 uF.

7.2 IC Assembly

The device is designed to operate with either single-ended or differential inputs. Figures 13, 14, and 15 show the IC assembly diagrams for positive and negative supply voltages. In either case, the supply should be capacitively bypassed to the ground in order to provide a good AC ground over the frequency range of interest. The backside of the chip should be connected to a good thermal heat sink.

All RF I/Os are connected to V_{CC} through on-chip termination resistors. This implies that when V_{CC} is not DC-grounded (as in the case of positive supply), the RF I/Os should be AC-coupled through series capacitors (unless the connecting circuit can generate the correct levels through level shifting).

7.3 Differential vs. Single-Ended

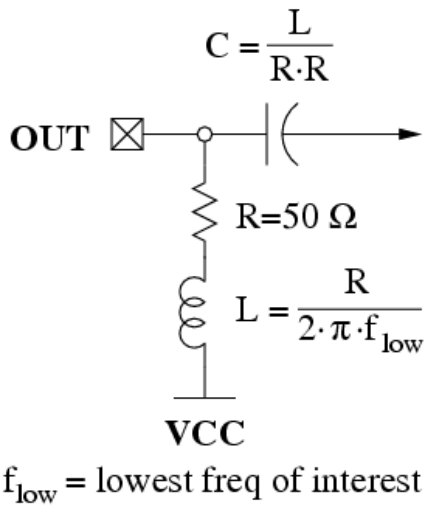
The UXN6M9M is fully differential to maximize signal-to-noise ratios for high-speed operation. All high-speed inputs and outputs are terminated to V_{CC} with on-chip resistors (refer to the functional block diagram for specific resistor values). The maximum DC voltage on any terminal must be limited to $V_{CC} \pm 1$ V in order to prevent damaging the termination resistors with excessive current. Regardless of bias conditions, the following equation should be satisfied when driving the inputs differentially:

$$V_{CC} - 1 < VAC/4 + VDC < V_{CC} + 1$$

where VAC is the input signal p-p voltage and VDC is common-mode voltage.

The outputs require a DC return path capable of handling approximately 30 mA per side. If DC coupling is employed, the DC resistance of the receiving circuits should be 50 Ω to V_{CC}. If AC coupling is used, a bias tee circuit should be used as shown below. The discrete R/L/C elements should be resonance-free up to the maximum frequency of operation for broadband applications.

Figure 8 Bias Tee Circuit



In addition to the maximum input signal levels, single-ended operation imposes additional restrictions: the average DC value of the waveform at IC should be equal to V_{CC} for single-ended operations. In practice, this is easily achieved with a single capacitor on the input acting as a DC block. The value of the capacitor should be large enough to pass the lowest frequencies of interest.

Note: A potential oscillation mechanism exists if both inputs are static and have identical DC voltages—a small DC offset on either input is sufficient to prevent possible oscillations. Connecting a 10k Ω resistor between the unused input and V_{EE} should provide sufficient offset to prevent oscillation.

The following illustrations show the negative supply for DC and AC coupling of the UXN6M9M device.

Figure 9 Negative Supply (DC Coupling)

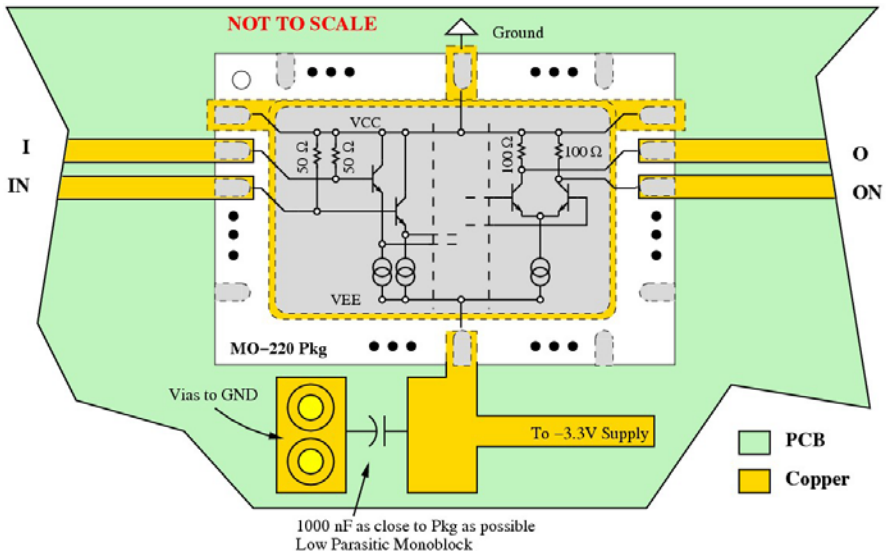
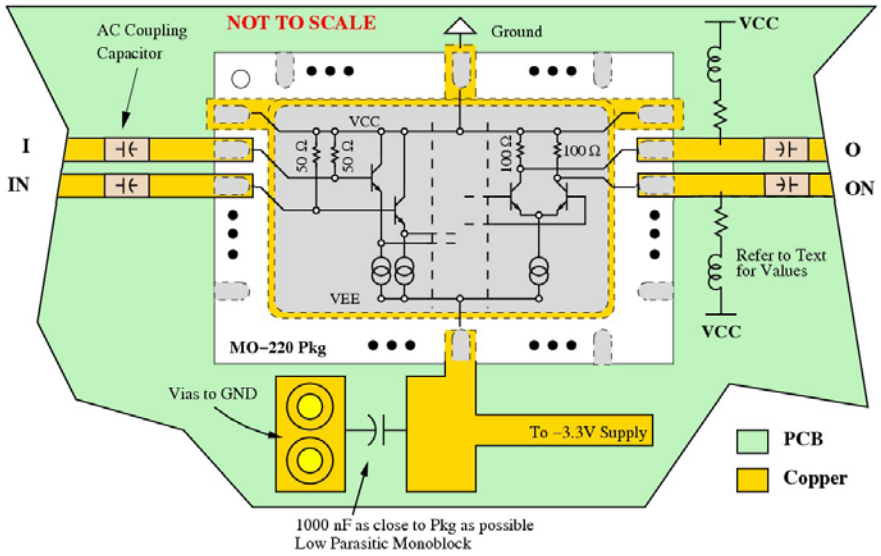


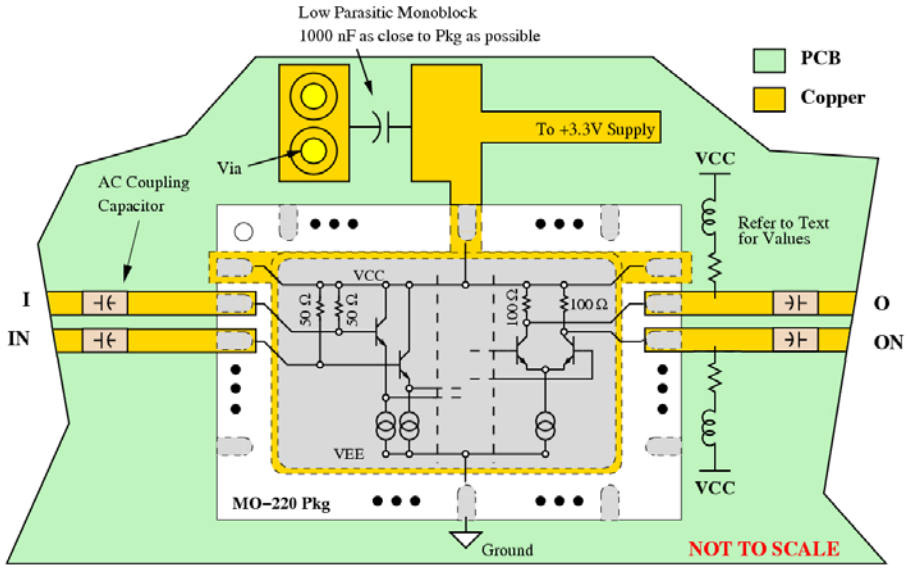
Figure 10 Negative Supply (AC Coupling)



The metalized backside of the QFN package (the paddle) is internally connected to V_{CC}, therefore will be a +3.3 V potential for the positive supply case. The paddle needs to be soldered to a pad on the PCB to provide a heat sink for the divider. Special attention to the PCB design is required to isolate the PCB pad from ground.

The following illustration shows the positive supply for AC coupling of the UXN6M9M device.

Figure 11 Positive Supply (AC Coupling)

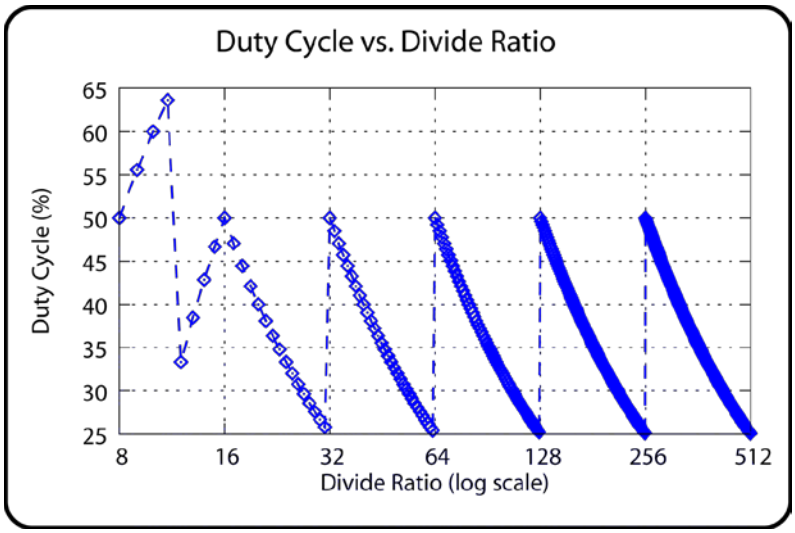


7.4 Duty Cycle

The UXN6M9M output duty cycle varies between 25% and 64% as a function of the divide ratio. For divide ratios between 16 and 511, the pulse width remains constant in each octave band (e.g., between 128 and 255), and gives a duty cycle of 50% for powers of 2. Thus, the duty cycle is

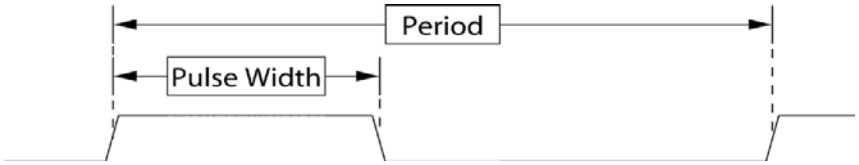
bounded between 25% and 50% for divide ratios between 16 and 511. For divide ratios between 8 and 15, the pulse width does not stay fixed, but varies with the divide ratio. The duty cycle ranges from 33% to 64% for these divide ratios. Table 8 gives pulse width and other necessary information for computing the duty cycle, given the divide ratio. The following graph summarizes the duty cycles for all possible divide ratios.

Figure 12 Duty Cycle vs. Divide Ration



The following illustration shows the period–pulse width relationship for the UXN6M9M device.

Figure 13 Period–Pulse Width Relationship



The following table shows a summary of the duty cycle for the UXN6M9M device.

Table 8 Duty Cycle Summary

Divide Ratio	Pulse Width (Input Cycles)	Duty Cycle (%)
8	4	50
9	5	55.6
10	6	60
11	7	63.6
12	4	33.3
13	5	38.5
14	6	42.9
15	7	46.7
16–31	8	50–25
32–63	16	50–25
64–127	32	50–25

Divide Ratio	Pulse Width (Input Cycles)	Duty Cycle (%)
128–255	64	50–25
256–511	128	50–25

8 Ordering Information

The following table shows the ordering information for the UXN6M9M device.

Table 9 Ordering Information

Part Number	Package
UXN6M9M	40-pin plastic QFN