PIC24FJ256DA210 Family Silicon Errata and Data Sheet Clarification

The PIC24FJ256DA210 Family devices that you have received conform functionally to the current Device Data Sheet (DS39969**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24FJ256DA210 Family silicon.

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

> **Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24FJ256DA210 Family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	
		A3	A4
PIC24FJ256DA210	410Eh	03h	04h
PIC24FJ256DA206	410Ch	03h	04h
PIC24FJ256DA110	410Fh	03h	04h
PIC24FJ256DA106	410Dh	03h	04h
PIC24FJ128DA210	410Ah	03h	04h
PIC24FJ128DA206	4108h	03h	04h
PIC24FJ128DA110	410Bh	03h	04h
PIC24FJ128DA106	4109h	03h	04h

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC24FJXXXDA1/DA2/GB2 Families Flash Programming Specification"* (DS39970) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]	
				A3	A4
Oscillator	Two-Speed Start-up	1.	Feature is not functional.	X	X
Resets	—	2.	POR flag also set on BOR and External Reset.	X	X
Enhanced PMP	—	3.	Write incompatibility with certain slave devices.	X	X
A/D Converter	—	4.	Module continues to draw current when disabled.	X	X
Interrupts	INTx	5.	External interrupts missed when writing to INTCON2	X	X
Output Compare	Cascaded Mode	6.	Some modes unavailable in Cascaded mode.	X	X
USB	Host Mode	7.	Low speed devices, when connected to a hub, will not work.	X	X
USB	Device and Host Modes	8.	ACTVIF wake-up behavior differs from previous documentation.	X	X
USB	OTG Mode	9.	VBUS comparators may trip at values outside of the required range for USB OTG operation.	X	X
USB	Device Mode	10.	EPSTALL bit behavior differs from previous documentation.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: Oscillator (Two-Speed Start-up)

Two-Speed Start-up is not functional. Leaving the IESO Configuration bit in its default state (Two-Speed Start-up enabled) may result in unpredictable operation.

Work around

None. Always program the IESO Configuration bit to disable the feature (CW2<15> = `0`).

Affected Silicon Revisions

A3	A4						
X	X						

2. Module: Resets

On Brown-out Resets and External (Master Clear) Resets, the POR bit may also become set. This may cause Brown-out and External Reset conditions to be indistinguishable from a Power-on Reset.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

3. Module: Enhanced PMP

The module is not write-compatible with slave devices that require data to be present before the Write strobe is asserted. The module has no configuration provision to output data before asserting the Write strobe.

Since most slave devices require valid input data to be present before the Write strobe is de-asserted, the significance of this issue is thought to be limited.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

4. Module: A/D Converter

Once the A/D module is enabled (AD1CON1<15> = `1`), it may continue to draw extra current even if the module later is disabled (AD1CON1<15> = `0`).

Work around

In addition to disabling the module through the ADON bit, set the corresponding PMD bit, ADC1MD (PMD1<0>), to power it down completely.

Affected Silicon Revisions

A3	A4						
X	X						

5. Module: Interrupts (INTx)

Writing to the INTCON2 register may cause an external interrupt event (inputs on INT0 through INT4) to be missed. This only happens when the interrupt event and the write event occur during the same clock cycle.

Work around

If this cannot be avoided, write the data intended for INTCON2 to any other register in the interrupt block of the SFR (addresses, 0080h to 00E0h); then write the data to INTCON2.

Be certain to write the data to a register not being actively used by the application, or to any of the interrupt flag registers, in order to avoid spurious interrupts. For example, if the interrupts controlled by IEC5 are not being used in the application, the code sequence would be:

```
IEC5 = 0x1E;
INTCON2 = 0x1E;
IEC5 = 0;
```

It is the user's responsibility to determine an appropriate register for the particular application.

Affected Silicon Revisions

A3	A4						
X	X						

6. Module: Output Compare (Cascaded Mode)

When 32-bit Cascaded mode is enabled (OCxCON2<8> = 1), these modes are unavailable:

- Single-Shot operations when OCM (OCxCON1<2:0> = 110 or 111 and OCTRIG (OCxCON2<7>) = 1 and TRIGMODE (OCxCON1<3>) = 1.
- Synchronous modes when the SYNCSEL bits (OCxCON2<4:0>) ! = 00000 and OCTRIG (OCxCON2<7>) = 0.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

7. Module: USB

While operating in Host mode and attached to a low-speed device through a full-speed USB hub, the host may persistently drive the bus to an SE0 state (both D+/D- as '0') which would be interpreted as a bus Reset condition by the hub; or the host may persistently drive the bus to a J state, which would make the hub detach condition undetectable by the host.

Work around

Connect low-speed devices directly to the host USB port and not through a USB hub.

Affected Silicon Revisions

A3	A4						
X	X						

8. Module: USB (Device and Host Modes)

In previous literature for this module, the ACTVIF interrupt flag (U1OTGIR<4>) is described as being asserted, based on state changes detected on D+, D- or VBUS, when the microcontroller is in Sleep mode. In actual implementation, state changes on the RF3/USBID pin also cause the ACTVIF flag to be asserted.

As a result, logic input level changes on RF3/USBID may cause ACTVIF to be asserted, even in non-OTG applications that do not use the USBID function. This may cause the microcontroller to wake up unexpectedly.

Work around

For On-The-Go (OTG) based applications: No work around is needed.

For non-OTG Device, Host or dual-role applications: If ACTVIF is used as a wake-up source, it is recommended that the application be designed so that RF3/USBID does not see any changes while the microcontroller is in a power-saving mode.

If RF3/USBID is not needed in the application, it is recommended to configure it as a digital output.

If the RF3/USBID pin is configured as a digital input, ensure that the signal provider does not change the pin state while ACTVIF is enabled as a wake-up source. If the pin is used as a general purpose input, which can change while in the USB Suspend state, check the IDIF flag (U1OTGIR<7>) after waking up from an ACTVIF event to determine if the wake-up event was caused by a state change on RF3/USBID.

Affected Silicon Revisions

A3	A4						
X	X						

9. Module: USB (OTG Mode)

When using the on-chip VBUS comparators, the comparators may trip at values outside of the required range for USB OTG operation.

Work around

For Device mode operation: Use the SESVDIF interrupt flag and SESVD status bit for detection of VBUS, instead of the VBUSVDIF interrupt and VBUSVD status bit.

For OTG operation: Use the External Comparator mode for proper level detection. This is enabled by setting the UVCMPDIS bit (U1CNFG2<1>).

Note that the External Comparator mode requires the application to include external comparators and logic to generate signals for the VCMPST or VBUSVLD/SESSVLD/SESSEND digital input pins, according to the bus conditions (Table 3). It is the user's responsibility to provide the appropriate circuit design for this application.

Affected Silicon Revisions

A3	A4						
X	X						

10. Module: USB (Device Mode)

In previous literature for this module, the EPSTALL bits (U1EPn<1>) are described as being only stall status indicator bits in Device mode. In actual implementation, the EPSTALL bits function as both status and control bits.

If the EPSTALL bit for endpoint 'n' is set (either by the SIE hardware or manually in firmware), both the IN and OUT endpoints, associated with the endpoint, will send STALL packets when the endpoint's UOWN bit (BDnSTAT<15>) is also set.

Work around

For Host applications: No work around is needed, as hosts do not send STALL packets.

For Device mode applications: When it is necessary to stop sending STALL packets on an endpoint, clear the endpoint's respective BSTALL (BDnSTAT<10>) and EPSTALL bits. If the application firmware was developed based on one of the examples in the Microchip USB framework, this is already the default behavior of the USB stack firmware (except Version 2.8); no further work around is normally needed.

If a Device mode application was based upon Version 2.8 of the USB framework, and the application uses STALL packets on any of the application endpoints (1-15), it is suggested to update the application to the latest version.

Affected Silicon Revisions

A3	A4						
X	X						

TABLE 3: EXTERNAL COMPARATOR MODE INPUTS FOR VARIOUS VBUS CONDITIONS

When UVCMPSEL = 0:

VCMPST1	VCMPST2	Bus Condition
0	0	VBUS < VB_SESS_END
1	0	VB_SESS_END < VBUS < VA_SESS_VLD
0	1	VA_SESS_VLD < VBUS < VA_VBUS_VLD
1	1	VBUS > VVBUS_VLD

When UVCMPSEL = 1:

VBUSVLD	SESSVLD	SESSEND	Bus Condition
0	0	1	VBUS < VB_SESS_END
0	0	0	VB_SESS_END < VBUS < VA_SESS_VLD
0	1	0	VA_SESS_VLD < VBUS < VA_VBUS_VLD
1	1	0	VBUS > VVBUS_VLD

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39969**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Guidelines for Getting Started with 16-Bit Microcontrollers

Section 2.4 Voltage Regulator Pins (ENVREG/DISVREG and VCAP/VDDCORE) has been replaced with a new and more detailed section. The entire text follows:

2.4 Voltage Regulator Pins (ENVREG/DISVREG and VCAP/VDDCORE)

The on-chip voltage regulator enable pin must always be connected directly to a supply voltage.

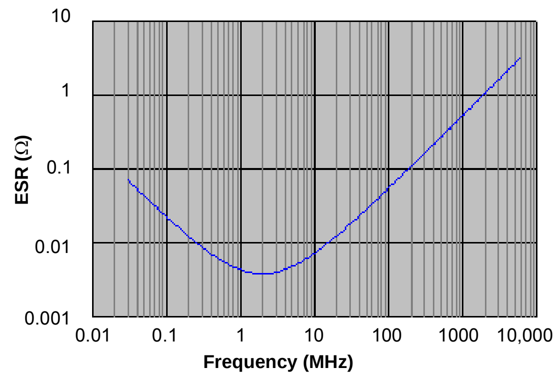
Refer to **Section 27.2 "On-Chip Voltage Regulator"** for details on connecting and using the on-chip regulator.

When the regulator is enabled, a low-ESR (< 5Ω) capacitor is required on the VCAP pin to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD and must use a capacitor of 10 µF connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in Table 2-1. Capacitors with equivalent specifications can be used.

Designers may use Figure 2-3 to evaluate ESR equivalence of candidate devices.

The placement of this capacitor should be close to VCAP. It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to **Section 30.0 "Electrical Characteristics"** for additional information.

FIGURE 2-3 FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP



Note: Typical data measurement at 25°C, 0V DC bias.

TABLE 2-1 SUITABLE CAPACITOR EQUIVALENTS

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage	Temp. Range
TDK	C3216X7R1C106K	10 µF	±10%	16V	-55 to 125ºC
TDK	C3216X5R1C106K	10 µF	±10%	16V	-55 to 85ºC
Panasonic	ECJ-3YX1C106K	10 µF	±10%	16V	-55 to 125ºC
Panasonic	ECJ-4YB1C106K	10 µF	±10%	16V	-55 to 85ºC
Murata	GRM32DR71C106KA01L	10 µF	±10%	16V	-55 to 125ºC
Murata	GRM31CR61C106KC31L	10 µF	±10%	16V	-55 to 85ºC

2.4.1 CONSIDERATIONS FOR CERAMIC CAPACITORS

In recent years, large value, low-voltage, surface mount ceramic capacitors have become very cost effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the internal voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

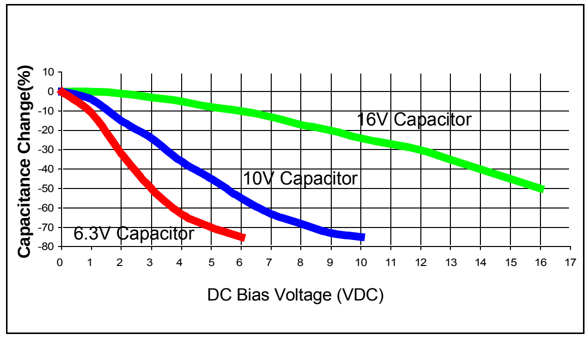
Typical low-cost, 10 µF ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as ±10% to ±20% (X5R and X7R), or -20%/+80% (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

The X5R and X7R capacitors typically exhibit satisfactory temperature stability (ex: ±15% over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of +22%/-82%. Due to the extreme temperature tolerance, a 10µF nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum internal voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the internal voltage regulator if the application must operate over a wide temperature range.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

A typical DC bias voltage vs. capacitance graph for 16V, 10V and 6.3V rated capacitors is shown in Figure 2-4.

FIGURE 2-4 DC BIAS VOLTAGE vs. CAPACITANCE CHARACTERISTICS



When selecting a ceramic capacitor to be used with the internal voltage regulator, it is suggested to select a high-voltage rating, so that the operating voltage is a small percentage of the maximum rated capacitor voltage. For example, choose a ceramic capacitor rated at 16V for the 1.8V V_{CAP} voltage. Suggested capacitors are shown in Table 2-1.

2. Module: Electrical Specifications

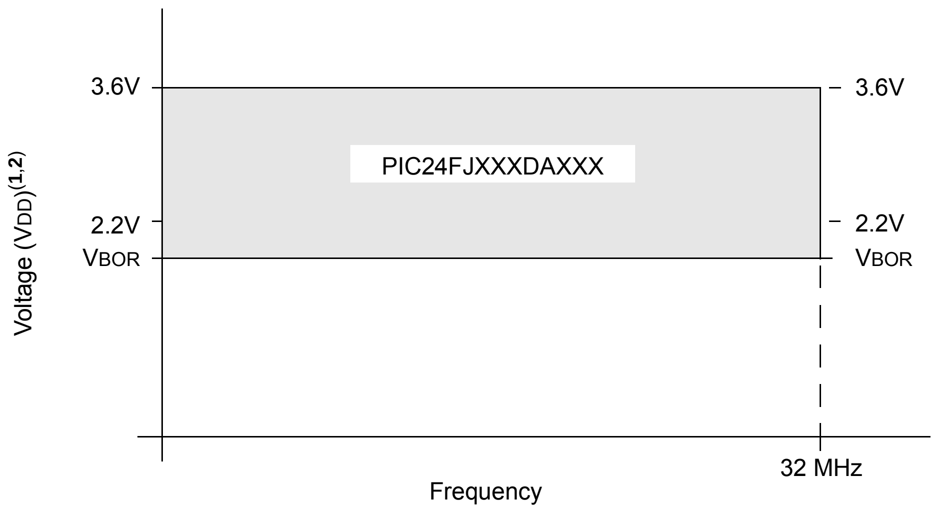
The "Absolute Maximum Ratings" listed on page 371 are amended by adding the following specification:

Voltage on VUSB with respect to VSS.................. (VDDCORE – 0.3V) to 4.0V

3. Module: Electrical Specifications (DC Characteristics)

Figure 30-1 ("PIC24FJ256DA210 Family Voltage-Frequency Graph") is amended by adding an additional footnote. The updated figure is shown below (changes in **bold**; bold in original removed for clarity).

FIGURE 30-1: PIC24FJ256DA210 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



Note 1: VCAP (nominal On-Chip Regulator output voltage) = 1.8V.

2: When the USB module is enabled, VUSB should be provided at 3.0V to 3.6V. When the USB module is not enabled, the wider limits shaded in grey apply. The voltage on the VUSB pin should be maintained at (VDD – 0.3V) or greater. Optionally, the pin may be left in a high-impedance state when the USB module is not in use, but doing so may result in higher IPD currents than specified.

4. Module: Electrical Specifications (DC Characteristics)

Table 30-3 ("DC Characteristics: Temperature and Voltage Specifications") is amended by adding a new specification, VUSB, and an explanatory footnote. The changes are shown below in **bold** (bold text in original removed for clarity).

TABLE 30-3: DC CHARACTERISTICS: TEMPERATURE AND VOLTAGE SPECIFICATIONS (PARTIAL REPRESENTATION)

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Symbol	Characteristic	Min	Typ(1)	Max	Units	Conditions
Operating Voltage							
	VUSB	**USB Supply Voltage**	**Greater of: 3.0 or (VDD – 0.3V)**	**3.3**	**3.6**	**V**	**USB module enabled**
			(VDD – 0.3V)(3)	**—**	**3.6**	**V**	**USB disabled, RG2/RG3 unused and externally pulled low or left in high-impedance state**
			(VDD – 0.3V)	**VDD**	**3.6**	**V**	**USB disabled, RG2/RG3 used as general purpose I/O**

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: This is the limit to which VDD can be lowered without losing RAM data.

3: The VUSB pin may also be left in a high-impedance state under these conditions. However, if the voltage floats below (VDD – 0.3V), this may result in higher IPD currents than specified.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (6/2010)

Initial release of this document; issued for revision A3. Includes silicon issues 1 (Oscillator – Two-Speed Start-up), 2 (Resets), 3 (Enhanced PMP), 4 (A/D), 5 (Interrupts – INTx), and 6 (Output Compare – Cascaded Mode).

Rev B Document (9/2010)

Revised silicon issue 4 (A/D Converter) to reflect updated definition of issues.

Added data sheet clarification issue 1 (Guidelines For Getting Started with 16-Bit Microcontrollers).

Rev C Document (1/2011)

Added silicon issue 7 (USB).

Rev D Document (6/2011)

Added silicon revision A4. Adds existing silicon issues 1 through 7 from revision A3 without changes. No new data sheet clarifications added. No issues removed.

Rev E Document (9/2011)

Added silicon issues 8 (USB – Device and Host Modes), 9 (USB – OTG Mode) and 10 (USB – Device Mode) to all revisions.

Added data sheet clarification issues 2, 3 and 4 (Electrical Characteristics).

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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