Isolated, Constant Current LED Driver

Features

- Programmable true constant current operation
- ±3% LED current accuracy
- Adaptive to external component tolerances and parasitics
- Primary-side current sensing
- Output open circuit protection
- Output short circuit protection
- Input under voltage lockout
- PWM dimming / enable
- Universal 80-264VAC operation

Applications

- Low-power lighting fixtures

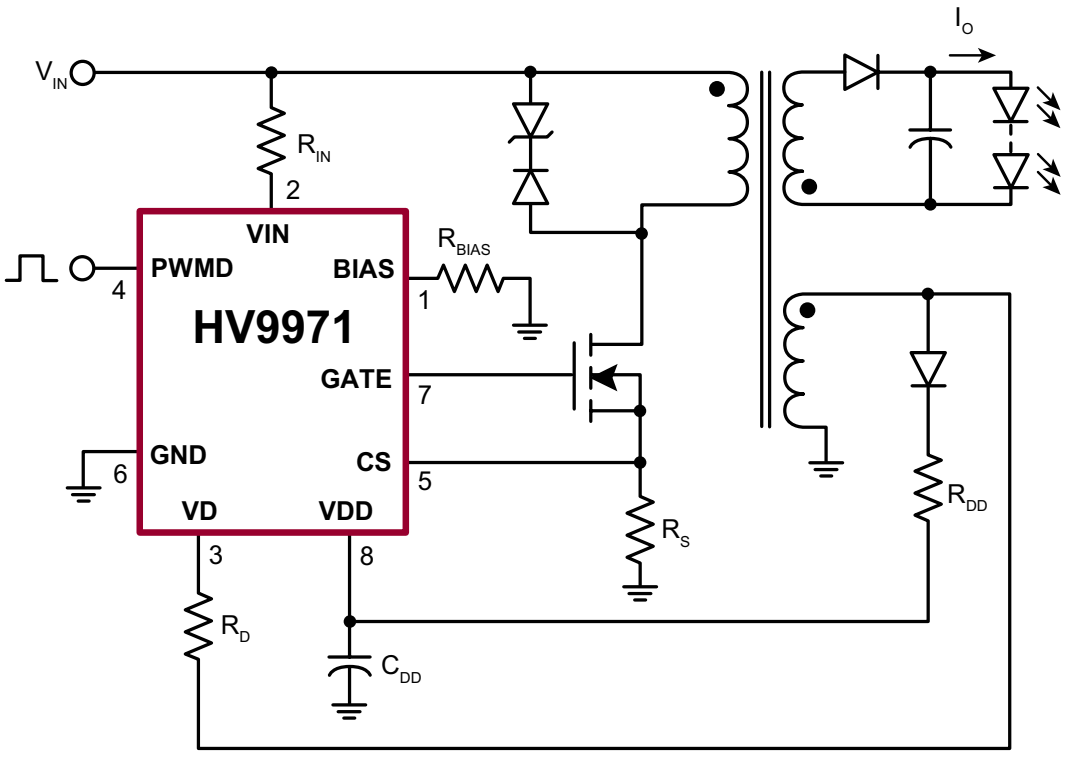
General Description

The HV9971 is a primary-side control IC for driving a discontinuous conduction mode (DCM) flyback LED driver. The IC is optimized for operation at a constant full-load switching frequency of 100kHz and the universal input AC voltage range of 80-264VAC. It maintains 3% variation of the LED current setting, and features tight line and load regulation. The proprietary primary-side output current control employed in the HV9971 makes the output current setting insensitive to most component tolerances and parasitics without use of an opto-feedback.

The HV9971 LED driver is fully protected against output open and short circuit conditions and input under-voltage. It also offers a logic input for dimming the LED light output by means of pulse-width modulation of the output current.

The HV9971 is ideally suited for driving high-brightness LEDs in low-power lighting fixtures such as incandescent bulb retrofits.

Typical Application Circuit

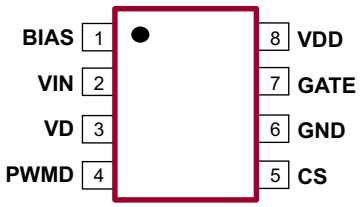


Ordering Information

Part Number	Package Option	Packing
HV9971LG-G	8-Lead SOIC	2500/Reel

-G denotes a lead (Pb)-free / RoHS compliant package

Pin Configuration



8-Lead SOIC

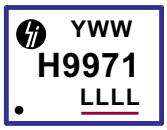
Absolute Maximum Ratings*

Parameter	Value
VIN, VD, BIAS current	±5.0mA
VDD voltage	-0.3V to V_{SHUNT}
VDD current	10mA
GATE voltage	-0.3V to V_{DD} +0.3V
CS, PWMD voltage	-0.3V to 6.0V
Operating temperature range	-40°C to +125°C
Storage temperature range	-65°C to +150°C
Continuous power dissipation (T_A = +25°C) (derate 6.3mW/°C above +25°C)	630mW

** All voltages referenced to GND pin.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Product Marking



Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead SOIC

Typical Thermal Resistance

Package	θ_{ja}
8-Lead SOIC	101°C/W

Electrical Characteristics

(Specifications are at T_A = 25°C, V_{DD} = 10V, I_{IN} = 200µA, C_{GATE} = 750pF, BIAS open, unless otherwise noted).

Sym	Description		Min	Typ	Max	Units	Conditions
Power Supply (VDD)							
V_{DD}	Shunt voltage	*	10.5	11.0	11.5	V	---
$V_{DD(START)}$	Start voltage	*	9.95	10.50	11.45	V	V_{DD} rising
$V_{DD(STOP)}$	Under voltage threshold	*	6.65	7.00	7.70	V	V_{DD} falling
I_{DDQ}	Supply standby current	-	-	-	1.0	mA	Gate open
$I_{DDQ(START)}$	Start-up current	*	-	-	65	µA	V_{DD} = 10V

Notes:

* *Specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C.*

† *Parameters guaranteed by design*

Electrical Characteristics

Sym	Description		Min	Typ	Max	Units	Conditions
Feed Forward Inputs (VD, VIN) and Oscillator							
I_{IN}	Operating current range	*	0	-	1000	µA	---
I_D	Operating current range	*	0	-	1000	µA	---
$\Delta Q_{IN(MAX)}$	VIN Input charge swing	*†	-	-	460	pC	I_{IN} = 400µA, I_D = 0
K_{Osc}	Oscillator coefficient	*†	0.32	0.33	0.34	-	---
V_D	VD voltage	*	2.406	2.440	2.474	mV	---
$F_{S(START)}$	Start-up frequency	-	-	10	-	kHz	---
K_C	Effective integrator capacitance ratio V_{IN} to V_D	-	-	1	-	-	---
Bias Current Generator (BIAS)							
V_{BIAS}	Output voltage	*	1198	1220	1242	mV	---
GATE Output							
T_{RISE}	GATE output rise time	-	-	40	75	ns	---
T_{FALL}	GATE output fall time	-	-	20	40	ns	---
Current Sense Comparator							
$V_{CS(TH)}$	CS trip threshold	*	1198	1220	1242	mV	---
T_{DELAY}	Propagation delay CS to GATE	*	-	-	100	ns	(V_{CS} - $V_{CS(TH)}$) = 20mV
T_{BLANK}	Leading edge blanking delay	*	200	300	400	ns	---
VIN Under Voltage Comparator							
$I_{IN(UVLO)}$	V_{IN} undervoltage threshold current	-	80	-	101	µA	V_{IN} falling
$\Delta I_{IN(UVLO)}$	V_{DD} undervoltage lockout hysteresis	-	-	15	-	µA	V_{IN} rising
Open Circuit Protection							
$I_{D(OV)}$	Output open circuit threshold	-	133	-	147	µA	---
PWM Dimming							
$V_{PWMD,HI}$	PWMD input high voltage	*	2.0	-	-	V	---
$V_{PWMD,LO}$	PWMD input low voltage	*	-	-	0.8	V	---
Effective Current Sense Reference Voltage							
V_{EFF}	Effective reference voltage	-	195.5	-	207.6	mV	I_{IN} = 170µA, I_D = 120µA, See Note 1.
$\Delta V_{EFF}/V_{EFF}$	I_{IN}, I_D regulation of V_{EFF}	†	-	3.0	-	%	110µA ≤I_{IN} ≤ 350µA, 40µA ≤I_D ≤ 120µA

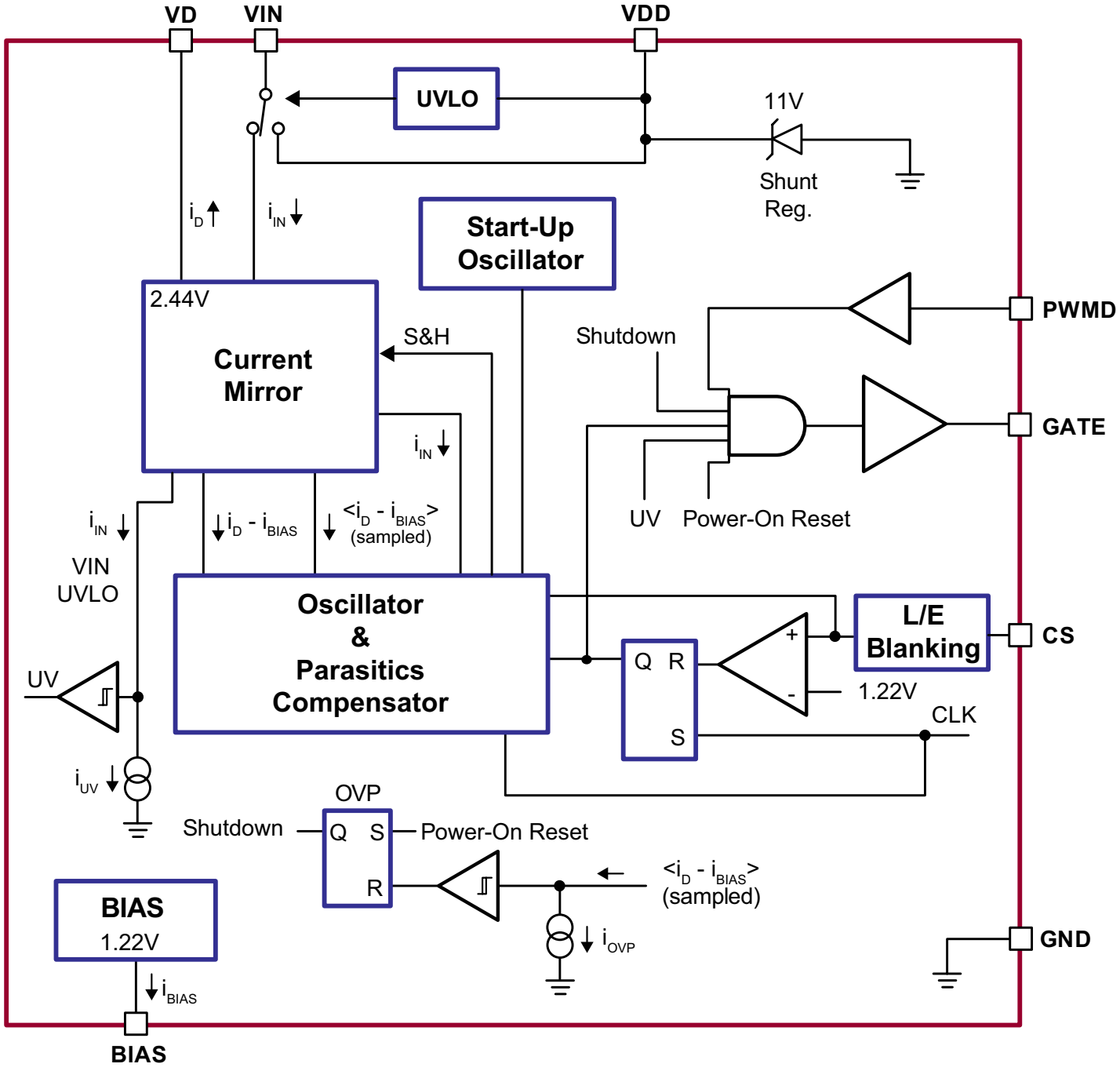
Notes:

* *specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C.*

† *Parameters guaranteed by design.*

1. *Effective output current V_{EFF} = 0.5 • V_{CS} • K_{Osc}. Trimmed to the product of V_{CS} • K_{Osc}.*

Functional Block Diagram



Functional Description

Power Topology and Control Method

The HV9971 regulates constant output current of a discontinuous conduction mode (DCM) flyback converter. Although it can be used in other applications, it is optimized for operating from a universal AC line input voltage of 85-264VAC. The HV9971 is a fully integrated peak-current PWM controller IC. It does not require an optocoupler feedback and includes protection from output open-circuit, short-circuit, and input under-voltage conditions. A proprietary control scheme permits accurate primary-side control of output current insensitive to most circuit parasitics, external component tolerances and output voltage variation.

Output current of an HV9971 flyback converter can be expressed as:

$$I_O = \frac{I_{PK} \bullet n \bullet T_{COND}}{2 \bullet T_{SW}} = \frac{I_{PK} \bullet n \bullet K_{Osc}}{2} \quad (1)$$

Where:

$$K_{Osc} = \frac{T_{COND}}{T_{SW}} = 0.33$$

is an oscillator coefficient (HV9971 Control Law), n is the flyback transformer turns ratio of primary to secondary winding.

I_{PK} is primary winding peak current given by:

$$I_{PK} = \frac{V_{CS(TH)}}{R_S} \quad (2)$$

In (2), $V_{CS(TH)}$ is the reference voltage of the current sense comparator at CS, and R_S is the current sense resistance.

Combining (1) and (2), we can express the output current as:

$$I_O = \frac{V_{CS(TH)} \bullet n \bullet K_{Osc}}{2 \bullet R_S} = \frac{n \bullet V_{EFF}}{R_S} \quad (3)$$

The effective reference voltage V_{EFF} = 200mV. Hence, the desired LED current is programmed by mere selecting the current sense resistor as:

$$R_S = \frac{n \bullet V_{EFF}}{I_O} \quad (4)$$

Note that the output current of the HV9971 LED driver is independent of the input and output voltage, the switching frequency or the transformer inductance.

The switching frequency at a given output voltage V_O can be estimated, based on (1) as:

$$F_S = \frac{1}{T_{SW}} = \frac{K_{Osc}}{T_{COND}} = \frac{n \bullet (V_O + V_F) \bullet K_{Osc}}{L_M \bullet I_{PK}} = \frac{V_{OR} \bullet K_{Osc}}{L_M \bullet I_{PK}} \quad (5)$$

Where V_{OR} is reflected output voltage at the primary side:

$$V_{OR} = n \bullet (V_O + V_F) \quad (6)$$

In the equation (5), L_m is magnetizing inductance of the transformer primary winding, and V_F is the forward voltage drop at the output rectifier diode. (Note that the switching frequency is not a function of the internal timing components of the HV9971 or the absolute value of R_{IN} and R_D).

Proper selection of maximum switching frequency $F_{S(MAX)}$ at full load in combination with maximum $V_{OR(max)}$ is critical for proper operation of the HV9971. The oscillator circuit ramp may saturate when the maximum charge swing $\Delta Q_{IN(MAX)}$ = 400pC is exceeded at VIN. Therefore, the circuit components should be selected such that:

$$\Delta Q_{IN} = \frac{V_{IN} \bullet T_{ON}}{R_{IN}} \le \Delta Q_{IN(MAX)} \quad (7)$$

*(*Note that the HV9971 is protected against careless oscillator setup. When saturation of the oscillator ramp occurs, the HV9971 shuts off and attempts to go through a start-up cycle again.)

The transformer magnetic flux equals the volt-seconds at the transformer winding in the DCM flyback converter:

$$V_{IN} \bullet T_{ON} \approx L_M \bullet I_{PK} \quad (8)$$

Therefore, the charge swing ΔQ_{IN} varies only as a function of external component tolerances and circuit parasitic, and it is the same for all V_{IN} and V_O operating conditions. Combining equations (5), (7) and (8), and taking into consideration tolerances for L_m, R_S and $V_{CS(TH)}$, we get the following design criterion:

$$V_{OR(MAX)} \le \frac{F_{S(MAX)} \bullet \Delta Q_{IN(MAX)} \bullet R_{IN(MIN)}}{K_{Osc}} \bullet \frac{L_{M(MIN)} \bullet R_{IN(MIN)} \bullet R_{S(MIN)} \bullet V_{CS(TH)MIN}}{L_{M(MAX)} \bullet R_{IN(NOM)} \bullet R_{S(MAX)} \bullet V_{CS(TH)MAX}} \quad (9)$$

We can now rearrange (9):

$$V_{OR(MAX)} \leq \frac{F_{S(MAX)} \bullet \Delta Q_{IN(MAX)} \bullet R_{IN(MIN)}}{K_{Osc(MAX)}} \bullet K_{TOL} \quad (10)$$

Where:

$$K_{TOL} = \frac{L_{M(MIN)} \bullet R_{IN(MIN)} \bullet R_{S(MIN)} \bullet V_{CS(TH)MIN}}{L_{M(MAX)} \bullet R_{IN(NOM)} \bullet R_{S(MAX)} \bullet V_{CS(TH)MAX}} \quad (11)$$

K_{TOL} being a function of tolerances only.

For a typical inductor tolerance of ±10%, we get:

$$\frac{L_{M(MIN)}}{L_{M(MAX)}} = \frac{0.9 \bullet L_{M(NOM)}}{1.1 \bullet L_{M(NOM)}} = 0.818$$

For resistors with tolerance of ±1%, we get:

$$\frac{R_{S(MIN)}}{R_{S(MAX)}} = \frac{0.9 \bullet R_{S(NOM)}}{1.01 \bullet R_{S(NOM)}} = 0.980$$

$$\frac{R_{S(MIN)}}{R_{S(NOM)}} = \frac{0.9 \bullet R_{S(NOM)}}{R_{S(NOM)}} = 0.990$$

We can also have a numeric value for:

$$\frac{V_{CS(TH)MIN}}{V_{CS(TH)MAX}} = \frac{1198}{1242} = 0.965$$

Plugging all the numeric coefficients into (11), we eventually get:

$$K_{TOL} = 0.77 \quad (12)$$

The equation (10) gives the condition for selecting proper ratio of $V_{OR(MAX)}/F_{S(MAX)}$, which guarantees $\Delta Q_{IN} \leq \Delta Q_{IN(MAX)}$. Selection of the resistor R_{IN} is dictated by the desired input under-voltage (UV) and output over-voltage (OV) protection thresholds. For example, selection of R_{IN} = 1MΩ produces a UV shutdown at V_{IN} < 90V, adequate for a universal AC line voltage range of 85 - 265VAC, and an OV shutdown at V_{OR}>140V for nominal values of $I_{IN(UVLO)}$ and $I_{D(OV)}$. The choice of optimal values for $F_{S(MAX)}$ and R_{IN} with consideration of tolerances will be considered later.

The above approach takes full advantage of the available V_{IN} input dynamic range, and, therefore, achieves the most accurate control over the LED current. Given, the primary-to-secondary turn ratio is determined simply as:

$$n = \frac{V_{OR(MAX)}}{(V_{O(MAX)} + V_F)} \quad (13)$$

The maximum magnetizing inductance of the primary winding $L_{m(MAX)}$ is obtained by combining the equations (2), (7) and (8):

$$L_{M(MAX)} = \frac{\Delta Q_{IN(MAX)} \bullet R_{IN(MIN)} \bullet R_{S(MIN)}}{V_{CS(TH)MAX}} \quad (14)$$

If we assume the primary inductance tolerance of ±10%, the nominal value of L_M is determined simply as:

$$L_M = \frac{L_{M(MAX)}}{1.1} \quad (15)$$

Selection of the maximum magnetizing inductance in accordance with (14) guarantees DCM operation in the entire working range of the input voltage with the proper selection of the input under-voltage and output over-voltage thresholds. (See “Input Under-Voltage Protection” and “Output Open and Short Circuit Protection” below.)

Due to presence of the leakage inductance L_{LK}, a voltage spike occurs at the primary winding of the transformer. Although the HV9971 eliminates the effect of the leakage inductance on the LED current, the duration of this spike should be minimized for best efficiency. The time t_{LK} is the leakage spike duration, determined by:

$$t_{LK} = \frac{L_{LK} \bullet I_{PK}}{V_Z - n(V_{O(MAX)} + V_F)} \quad (16)$$

Here, L_{LK} is primary winding leakage inductance; V_Z is the Zener clamp voltage. Hence, the Zener clamp voltage V_Z should be selected significantly higher than n ($V_{O(max)}$ + V_F). V_Z must also exceed the open-circuit protection threshold.

The HV9971 is powered by an internal shunt regulator, clamping VDD at $V_{DD(max)}$ = 11.5V. The IC shuts down when the voltage at VDD falls below $V_{DD(STOP)}$ ($V_{DD(STOP)nom}$ = 7V). Under steady-state operation, the IC is powered from an auxiliary bootstrap winding through a ballast resistor R_{DD}. The primary-to-auxiliary winding turn ratio n_{AUX} and the value of R_{DD} should be selected carefully to ensure operation throughout the input and output voltage range with minimum power dissipation in R_{DD}. (Note that the polarity of the auxiliary winding is opposite to the polarity of the secondary winding, such that the auxiliary winding voltage is positive during the on time.) The following formulas are providing optimal values for n_{AUX} and R_{DD}, given the output voltage range $V_{O(min)}$, $V_{O(max)}$ and the input voltage range $V_{IN(min)}$, $V_{IN(max)}$:

$$n_{AUX} = \frac{V_{IN(MIN)} \bullet V_{IN(MAX)}}{2 \bullet (V_{DD(STOP)MIN} + V_F) \bullet V_{IN(MAX)} - V_{IN(MIN)} \bullet (V_{DD(MAX)} + V_F)} \quad (17)$$

$$R_{DD} = \frac{\left(\frac{(V_{DD(STOP)MIN} + V_F)}{V_{IN(MIN)}} - \frac{(V_{DD(MAX)} + V_F)}{V_{IN(MAX)}}\right) \bullet n \bullet (V_{O(MIN)} + V_F) \bullet K_{Osc}}{I_{DDQ} + Q_{GATE} \bullet \frac{(V_{O(MIN)} + V_F)}{(V_{O(MAX)} + V_F)} \bullet F_{S(MAX)}} \quad (18)$$

$$W_{DD} = \frac{\left(\frac{V_{IN(MAX)}}{n_{AUX}} - (V_{DD(MIN)} + V_F)\right)^2 \bullet n \bullet (V_{O(MAX)} + V_F) \bullet K_{Osc}}{R_{DD} \bullet V_{IN(MAX)}} \quad (19)$$

Here, W_{DD} is power dissipation in R_{DD}, Q_{GATE} is the gate charge of the power MOSFET. Also, in formulas (17), (18), (19) tolerances of $V_{DD(STOP)}$ and V_{DD} are accounted for as well as forward voltage drop on auxiliary winding diode.

Start-Up

Upon applying the input AC power, the input current of VIN is diverted into the hold-up capacitor connected at VDD. The HV9971 consumes less than 60µA in this mode, and its GATE output is off. When a threshold of V_{DD} is reached, VIN is disconnected from VDD, and the GATE output turns on. The GATE turns off upon reaching $V_{CS(TH)}$=1.220V at CS. The frequency of the GATE pulses is determined by the oscillator circuit or by the 10kHz start-up clock, whichever frequency is higher.

The hold-up capacitor connected at VDD must store enough energy to supply power to the HV9971 until adequate bootstrap power supply becomes available. The HV9971 stops switching and makes another attempt to charge the hold-up capacitor, if the voltage at VDD falls below 7.0V.

Although the resistors R_{IN} serves a different purpose in operation, its value must be selected with care to ensure the required 60µA start-up current at $V_{IN(min)}$.

Current Sense Comparator

The peak current comparator is using an external sense resistor R_S to compare the primary winding current to the reference voltage $V_{CS(TH)NOM}$ = 1.220V. The corresponding peak current I_{PK} is given by equation (2). When the current in the primary winding exceeds I_{PK}, the comparator resets the PWM flip-flop circuit, and the output pulse is terminated. The next cycle begins upon receiving a clock signal from an internal oscillator circuit. A 300ns leading-edge blanking delay is applied to prevent false triggering of the current sense comparator.

Oscillator Circuit

Upon the end of the start-up cycle, the input current of VIN is reverted to a current mirror circuit for generating the current i_{IN} in accordance with the following equation:

$$i_{IN} = \frac{V_{IN} - 1V}{R_{IN}} \approx \frac{V_{IN}}{R_{IN}} \quad (20)$$

Accordingly, the input current i_D is derived by connecting a resistor R_D from the bootstrap winding to VD. However, since n_{AUX} >>1 normally, the voltage V_{AUX} is not negligible in comparison to voltage at the VD pin (V_D = 2.43V). Hence, the current I_D through resistor R_D can be expressed as:

$$i_D = \frac{V_D - V_{AUX}}{R_D} \quad (21)$$

From this equation, the current I_D is not directly proportional to V_{AUX}. The offset current is given by the following equation:

$$i_{OS} = \frac{V_D}{R_D} \quad (22)$$

The HV9971 cancels out this offset internally by subtracting a current of the same magnitude as i_{OS}. This correction current is programmed by connecting a resistor at the BIAS pin in accordance with:

$$R_{BIAS} = \frac{V_{BIAS}}{3.5 \bullet i_{OS}} \quad (23)$$

In (23), V_{BIAS} = V_D/2 is voltage at the BIAS pin. Combining the equations (22) and (23) gives formula for calculating R_{BIAS} simply as:

$$R_{BIAS} = \frac{R_D}{7} \quad (24)$$

The resulting current i_{OR} = (i_D - i_{OS}) represents the instantaneous voltage across the transformer bootstrap winding:

$$i_{OR} = \frac{V_D - V_{AUX}}{R_D} - \frac{V_{BIAS}}{3.5 \bullet R_{BIAS}} = - \frac{V_{AUX}}{R_D} \quad (25)$$

Sampled during the conduction time of the transformer secondary winding, this current represents the reflected output voltage ($V_O + V_F$), where V_F is the voltage drop across the output rectified diode. The value of R_D should scale with R_{IN} in accordance with:

$$R_D = \frac{R_{IN} \bullet k}{n_{AUX}} \quad (26)$$

In (26), k is the coupling coefficient between the primary and the bootstrap windings. The coupling coefficient can be determined by measuring the leakage inductance $L_{S(AUX)}$ of the auxiliary winding with respect to the primary winding and calculating it in accordance with the equation:

$$k = \sqrt{1 - \frac{L_{S(AUX)}}{L_{AUX}}} \quad (27)$$

Here, L_{AUX} is the bootstrap winding inductance. Since the value of k is normally very close to 1, then k = 1 could be used as a first approximation.

With proper selection of the resistor R_D in accordance with (26), the oscillator circuit then generates switching frequency:

$$F_S = \frac{n \bullet (V_O + V_F) \bullet K_{Osc} \bullet R_S}{L_M \bullet V_{SC(TH)}} \quad (28)$$

Output Open and Short Circuit Protection

The HV9971 provides very reliable open circuit protection. If the sampled current i_{OR} exceeds the $I_{D(OV)}$($I_{D(OV)NOM}$ = 140µA) threshold, the HV9971 is forced to go through a power-up cycle again. The corresponding output voltage threshold can be calculated as:

$$V_{O(LIM)} = \frac{R_D \bullet n_{AUX}}{n} \bullet I_{D(OV)} - V_F \quad (29)$$

Normal operation resumes when the adequate LED load is connected.

Output short circuit protection is inherent to the HV9971 since the switching frequency is directly proportional to the output voltage. Moreover, loss of output voltage is likely to cause insufficient bootstrap power at VDD, resulting in a “hiccup” operating mode and repetitive restart attempts.

Input Under-Voltage Protection

The GATE output of the HV9971 becomes inhibited when the input current at VIN falls below $I_{IN(UVLO)}$ ($I_{IN(UVLO)NOM}$ = 90µA). The GATE output is enabled again when the VIN current exceeds $I_{IN(UVLO)} + \Delta I_{IN(UVLO)}$ ($I_{IN(UVLO)NOM} + \Delta I_{IN(UVLO)NOM}$ = 104µA). The corresponding input under-voltage thresholds can be calculated as:

$$V_{IN(STOP)} = R_{IN} \bullet I_{IN(UVLO)} \quad (30)$$

$$V_{IN(START)} = R_{IN} \bullet (I_{IN(UVLO)} + \Delta I_{IN(UVLO)}) \quad (31)$$

Design Considerations for meeting OVP and UVLO requirements

UVLO requirement is simply met by proper choice of R_{IN} according to equation (30). After a R_{IN} value is defined, it’s value is affecting the value of $V_{OR(MAX)}$ according to (13, 26, 29) and therefore affecting condition for OVP. We can meet condition for OVP now by proper choice of $F_{S(MAX)}$ which is not therefore an independent design parameter. The following calculation defines $F_{S(MAX)}$ adequate for meeting OVP condition. We start with rearranging (29):

$$(V_{O(LIM)} + V_F) \bullet n = R_D \bullet n_{AUX} \bullet I_{D(OV)MIN} \quad (32)$$

Using (26), we rearrange (32) into:

$$V_{OR(LIM)} = R_{IN(MIN)} \bullet k \bullet I_{D(OV)MIN} \quad (33)$$

Where also by (13):

$$V_{OR(LIM)} = (V_{O(LIM)} + V_F) \bullet n$$

To guarantee that OV threshold never trips under normal conditions, we must meet:

$$V_{OR(MAX)} \leq V_{OR(LIM)} \quad (34)$$

We define here coefficient (design parameter) $K_{OVP} \leq 1$ to specify sufficient margin to meet (34):

$$K_{OVP} = \frac{V_{OR(MAX)}}{V_{OR(LIM)}} \quad (35)$$

K_{OVP} should accommodate worst case voltage variation across output filtering capacitor plus some margin on top of it.

Note that switching frequency output ripple cannot cause OVP as the circuit uses for OVP VOR sampled in the middle of the conduction time. But variations of V_{OR} due to line and load regulation should be accounted for. After substituting (35) in (33) and (10):

$$\frac{F_{S(MAX)} \bullet \Delta Q_{IN(MAX)} \bullet R_{IN(MIN)}}{K_{Osc(MAX)}} \bullet K_{TOL} = K_{OVP} \bullet R_{IN(MIN)} \bullet k \bullet I_{D(OV)MIN}$$

Which we resolve to:

$$F_{S(MAX)} = \frac{K_{OVP} \bullet K_{Osc(MAX)} \bullet k \bullet I_{D(OV)MIN}}{K_{TOL} \bullet \Delta Q_{IN(MAX)}} \quad (36)$$

We can see that adequate value of $F_{S(MAX)}$ is independent of R_{IN} and some variation of it comes from K_{OVP} and K_{TOL}.

R-C Snubber Design Considerations

Detection of t_{LK} given by the equation (16) is crucial for proper operation of the HV9971. Upon the turn-off of the switching MOSFET, the voltage spike caused by the transformer leakage inductance is followed by high-frequency oscillation. The oscillation occurs at the transformer windings with the period equal to $2\pi\sqrt{L_{LK}C_{OSS}}$, where C_{OSS} is the output capacitance of the MOSFET. This oscillation is damped naturally by copper and core losses of the transformer, and it subsides during conduction time of the secondary winding. However, extra damping is usually required. Insufficiently damped, the post-spike oscillation may adversely affect accuracy of the output current regulation as well as the EMI performance of the LED driver.

Damping of the post-spike oscillation is achieved by the connection of a snubber network (R_{SN}, C_{SN}) across the switching MOSFET. Selection of the R_{SN} and C_{SN} values is based on achieving sufficient damping while minimizing the power losses in the snubber network. At the same time, the oscillation should not be over-damped, as this will prevent detection of t_{LK}.

We recommend the following first cut choice of the snubber network components:

$$C_{SN} = C_{OSS} \quad (37)$$

$$R_{SN} = 1.6 \bullet \sqrt{\frac{L_{LK}}{C_{SN}}} \quad (38)$$

Note that the output capacitance C_{OSS} is a nonlinear function of the drain voltage. Most datasheets give the C_{OSS} value at the drain voltage of V_{DS} = 25V. Typically, the output capacitance characteristic as a function of V_{DS} is provided in the MOSFET datasheet as well. The equation (29) should use the C_{OSS} value at $V_{DS} = (V_{IN(MIN)} + n \bullet V_{O(MIN)})$, or at the highest V_{DS} given in the plot, whichever voltage is lower.

Also note that the R-C snubber network must be connected between the drain and the source of the MOSFET, rather than being wired to ground or across the primary winding. Otherwise, the current from C_{SN} may cause false tripping of the CS comparator.

Power dissipation in R_{SN} can be estimated by the following formula:

$$W_{RSN} = C_{SN} \bullet V^2_{IN(MAX)} \bullet F_{S(MAX)} \quad (39)$$

Layout Considerations

The signal inputs VIN and VD operate at relatively low input current ranging from hundreds down to tens of microamps. Therefore, proximity of the switching potential of the MOSFET drain can cause a displacement current in VD and VIN affecting the normal operation of the HV9971. Proper HV9971 PCB layout should avoid direct proximity of the VD and VIN inputs to the high-voltage switching potential.

The resistor R_D should be placed as close as possible to the VD input. Otherwise, a long VD trace can be susceptible to noise coupling, or it can introduce parasitic capacitance with respect to ground capable of distorting the VD input signal.

Design Example

The design procedure defines essential components for HV9971 based LED driver for worst case conditions defined by tolerances of the components and the tolerances of the electrical characteristics of HV9971 chip. The range of the input voltage assumes that low frequency ripple is included. Output voltage range assumes average output voltages across LED string, with voltage ripple specified separately.

The following example illustrates LED driver design with HV9971 for the following conditions:

1. Input: $V_{IN(MIN)}$ = 110V, $V_{IN(MAX)}$ = 375V
2. Output: $V_{O(MIN)}$ = 6V, $V_{O(MAX)}$ = 18V, V_F = 0.7V, I_O = 0.5A, $(\Delta V_O/V_O)_{MAX}$ = 0.05 – ±5% output ripple
3. K_{TOL} = 0.766 (see definition in formula (11), also assuming ±10% inductor tolerance and ±1% resistor tolerance)
4. K_{OVP} = 0.9 - this value includes ±5% output ripple plus 5% safety margin
5. $V_{IN(STOP)}$ = 101V

Design:

1. Using formula (30), calculate value of the resistor R_{IN}:

$$R_{IN} = \frac{V_{IN(STOP)}}{I_{IN(UVLO)MAX}} = \frac{V_{IN(STOP)}}{101\mu A} = 1.0M\Omega$$

2. Using formula (36), calculate $F_{S(MAX)}$:

$$F_{S(MAX)} = \frac{K_{OVP} \bullet K_{Osc(MAX)} \bullet k \bullet I_{D(OV)MIN}}{K_{TOL} \bullet \Delta Q_{IN(MAX)}} = 115.5kHz$$

3. Using formula (10), calculate $V_{OR(MAX)}$:

$$V_{OR(MAX)} = \frac{F_{S(MAX)} \bullet \Delta Q_{IN(MAX)} \bullet R_{IN(NOM)}}{K_{Osc(MAX)}} \bullet K_{TOL} = 119.7V$$

4. Using formula (13), calculate primary-to-secondary turns ratio of the flyback transformer:

$$n = \frac{V_{OR(MAX)}}{(V_{O(MAX)} + V_F)} = 6.401$$

5. Using formula (4), calculate value of the current sense resistor:

$$R_S = \frac{n \bullet V_{EFF}}{I_O} = 2.56\Omega$$

6. Using formula (2), calculate value of the maximum peak current:

$$I_{PK(MAX)} = \frac{V_{CS(TH)MAX}}{R_{S(MIN)}} = \frac{V_{CS(TH)MAX}}{0.99 \bullet R_S} = 0.485A$$

7. Using formula (14), (15) calculate nominal value of the magnetizing inductance:

$$L_M = \frac{L_{M(MAX)}}{1.1} = \frac{\Delta Q_{IN(MAX)} \bullet R_{IN(MIN)} \bullet R_{S(MIN)}}{V_{CS(TH)MAX} \bullet 1.1} = 844.9\mu H$$

8. Using formula (17), calculate turns ratio primary-to-auxiliary winding of the flyback transformer:

$$n_{AUX} = \frac{V_{IN(MIN)} \bullet V_{IN(MAX)}}{2 \bullet (V_{DD(STOP)MIN} + V_F) \bullet V_{IN(MAX)} - V_{IN(MIN)} \bullet (V_{DD(MAX)} + V_F)} = 9.89$$

9. Using formulas (26) and (24), calculate values of the resistors R_D, R_{BIAS}:

$$R_D = \frac{R_{IN}}{n_{AUX}} = 101.1k\Omega$$

$$R_{BIAS} = \frac{R_D}{7} = 14.44k\Omega$$

10. Using formula (18), calculate value of the resistor R_{DD}:

$$R_{DD} = \frac{\left(\frac{(V_{DD(STOP)MIN} + V_F)}{V_{IN(MIN)}} - \frac{(V_{DD(MAX)} + V_F)}{V_{IN(MAX)}}\right) \bullet n \bullet (V_{O(MIN)} + V_F) \bullet K_{Osc}}{I_{DDQ} + Q_{GATE} \bullet \frac{(V_{O(MIN)} + V_F)}{(V_{O(MAX)} + V_F)} \bullet F_{S(MAX)}} = 270\Omega$$

(We have assumed Q_{GATE}=15nC.)

11. Using formula (19), calculate the maximum power dissipation W_{DD} in the resistor R_{DD}:

$$W_{DD} = \frac{\left(\frac{V_{IN(MAX)}}{n_{AUX}} - (V_{DD(MIN)} + V_F)\right)^2 \bullet n \bullet (V_{O(MAX)} + V_F) \bullet K_{Osc}}{R_{DD} \bullet V_{IN(MAX)}} = 0.26W$$

12. Using formulas (37), (38) calculate the first cut values of capacitor C_{SN} and resistor R_{SN}. Assume C_{OSS}= 33pF (IRFUC20, 600V 1A MOSFET), L_{LK}= 20µH:

$$C_{SN} = C_{OSS} = 33pF$$

$$R_{SN} = 1.6 \bullet \sqrt{\frac{L_{LK}}{C_{SN}}} = 880\Omega$$

The final values of the snubber components should be defined by compromise between critical damping minimizing leakage ringing and power dissipation accuracy of current regulation, leakage ringing should not change the value of V_{OR} at 50% of the output diode conduction time by more than 1%.

13. Using formula (39), calculate the maximum power dissipation W_{RSN} in the resistor R_{SN}:

$$W_{RSN} = C_{SN} \cdot V^2_{IN(MAX)} \cdot F_{S(MAX)} = 0.476W$$

14. Evaluate amplitude of the unclamped leakage spike:

$$V_{LK(MAX)} = I_{PK(MAX)} \cdot \sqrt{\frac{L_{LK}}{C_{OSS}}} = 267V$$

15. Evaluate maximum voltage stress on the drain of the MOSFET without clamping Zener diode:

$$V_{MOS(MAX)} = V_{IN(MAX)} + V_{OR(MAX)} + V_{LK(MAX)} = 762V$$

Choose MOSFET with $V_{MOS(MAX)}$= 700V

16. Design Zener clamp:

Evaluate maximum Zener voltage to keep maximum MOSFET drain stress less than $K_{MOS} \cdot V_{(MOS)MAX}$ (here K_{MOS}= 0.95, assuming 5% margin)

$$V_{Z(MAX)} = (K_{MOS} \cdot V_{MOS(MAX)}) - V_{IN(MAX)} - V_{OR(MAX)} = 170V$$

Evaluate nominal Zener voltage assuming that maximum Zener voltage could be higher than nominal by k_Z=1.2:

$$V_{Z(NOM)} = \frac{V_{Z(MAX)}}{k_Z} = 142V$$

Using modified formula (16) to evaluate leakage spike duration:

$$t_{LK} = \frac{L_{LK} \cdot I_{PK(MAX)}}{V_Z - V_{OR(MAX)}} = 115nS$$

Evaluate maximum power dissipation on Zener diode:

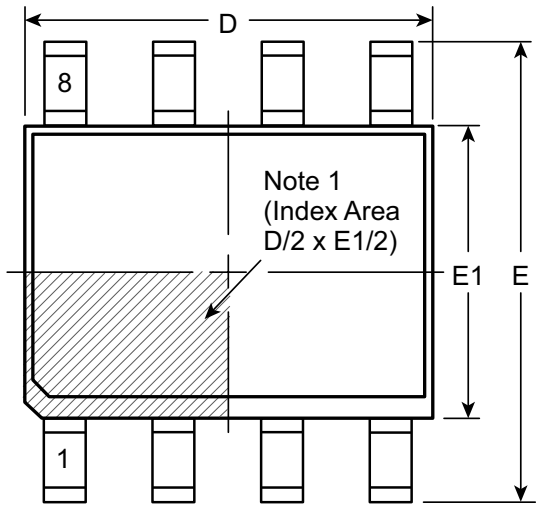
$$W_{Z(MAX)} = 0.5 \cdot t_{LK} \cdot I_{PK(MAX)} \cdot V_{Z(MAX)} \cdot F_{S(MAX)} = 0.457W$$

Pin Description

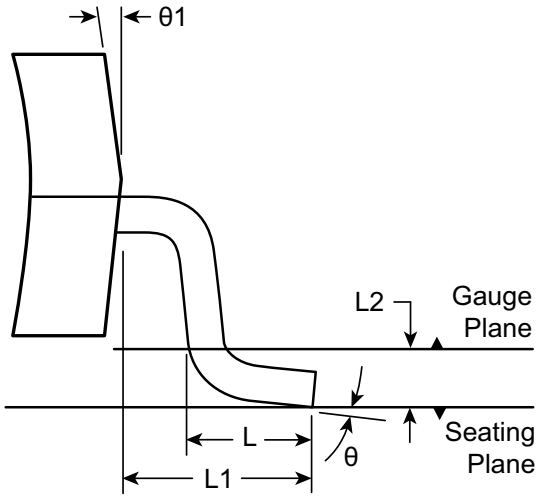
Pin #	Function	Description
1	BIAS	This pin is used for generating a correction current to account for the 2.44V offset at VD. Connect a resistor to ground to program.
2	VIN	This pin is the input voltage feed forward input. Connect a resistor from this pin to the input side of the primary winding of the transformer to program the VIN current. The same resistor is also used for start-up upon initial application of power.
3	VD	This pin is the auxiliary winding feedback input. Connect a resistor from this pin to the transformer bootstrap winding.
4	PWMD	When this pin is pulled to GND, switching of the HV9971 is disabled. When the PWM pin is released, or external TTL high level is applied to it, switching will resume.
5	CS	This pin is for sensing peak output voltage at an external current sense resistor.
6	GND	This pin is the common return for all the internal circuits.
7	GATE	This pin is the output gate driver for an external N-channel power MOSFET.
8	VDD	This is a power supply pin for all internal circuits. It must be bypassed with a low ESR capacitor to GND. The capacitor must be able to store sufficient energy for starting up the converter.

8-Lead SOIC (Narrow Body) Package Outline (LG)

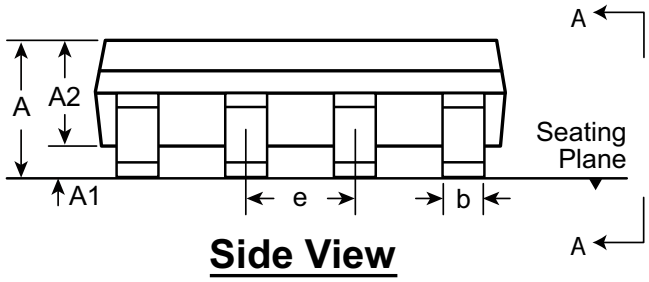
4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



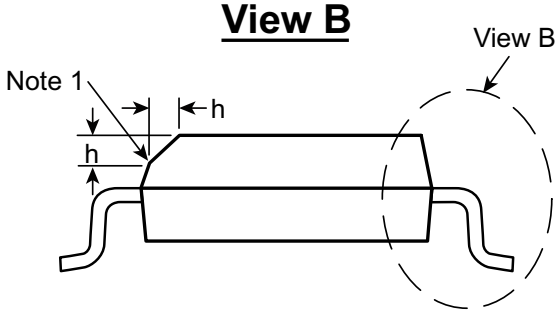
Top View



View B



Side View



View A-A

Note:

1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
***Supertex Doc. #:** DSPD-8SOLGTG, Version I041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
Tel: 408-222-8888
www.supertex.com