# ZL40200

# Precision 1:2 LVPECL Fanout Buffer

Data Sheet

April 2014

**Ordering Information**

| | | |
|---|---|---|
| ZL40200LDG1 | 16 Pin QFN | Trays |
| ZL40200LDF1 | 16 Pin QFN | Tape and Reel |

Matte Tin

Package size: 3 x 3 mm

**-40$^{o}$C to +85$^{o}$C**

## Features

### Inputs/Outputs

- Accepts differential or single-ended input
    - LVPECL, LVDS, CML, HCSL, LVCMOS
- Two precision LVPECL outputs
- Operating frequency up to 750 MHz

### Power

- Options for 2.5 V or 3.3 V power supply
- Core current consumption of 49 mA
- On-chip Low Drop Out (LDO) Regulator for superior power supply rejection

### Performance

- Ultra low additive jitter of 39 fs RMS

## Applications

- General purpose clock distribution
- Low jitter clock trees
- Logic translation
- Clock and data signal restoration
- Wired communications: OTN, SONET/SDH, GE, 10 GE, FC and 10G FC
- PCI Express generation 1/2/3 clock distribution
- Wireless communications
- High performance microprocessor clock distribution

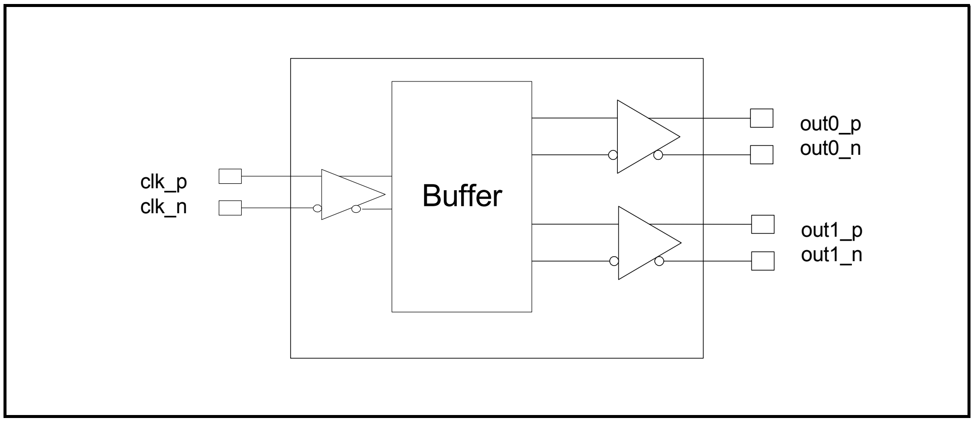


**Figure 1 - Functional Block Diagram**

Microsemi Corporation

# Table of Contents

# List of Figures

## Change Summary

Below are the changes from the February 2013 ti the April 2014 issue:

| Page | Item | Change |
|---|---|---|
| 1 | Applications | Added PCI Express clock distribution. |
| 5 | Pin Description | Added exposed pad to Pin Description. |
| 6, 7 | Figure 3 and Figure 4 | Removed 22 Ohm series resistors from Figure 3 and 4. These resistors are not required; however there is no impact to performance if the resistors are included. |
| 13 | Figure 16 | Corrected LVPECL interface circuit. |
| 18 | Figure 21 | Clarification of $V_{ID}$ and $V_{OD.}$ |

Below are the changes from the November 2012 issue to the February 2013 issue:

| Page | Item | Change |
|---|---|---|
| 7 | Figure 4 | Changed text to indicate the circuit is not recommended for VDD_driver=2.5V. |
| 7 | Figure 5 | Changed pull-up and pull-down resistors from 2kOhm to 100 Ohm. |

## 1.0 Package Description

The device is packaged in a 16 pin QFN

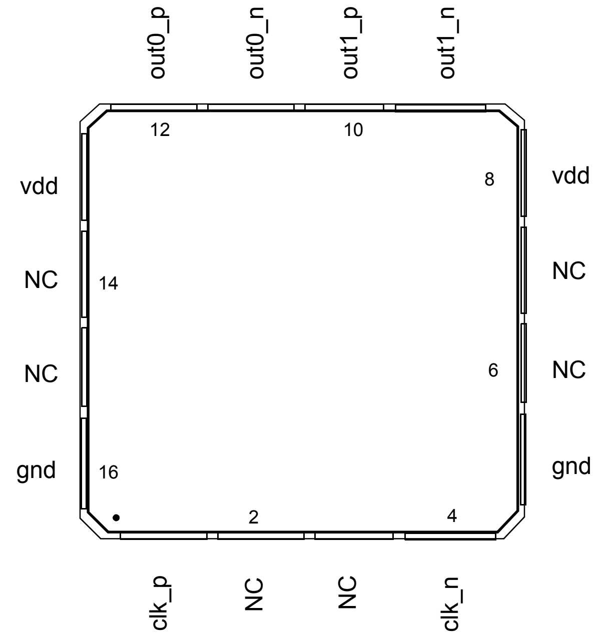


**Figure 2 - Pin Connections**

## 2.0 Pin Description

**Pin Description**

| Pin # | Name | Description |
|---|---|---|
| 1, 4 | clk_p, clk_n, | **Differential Input (Analog Input).** Differential input signals. |
| 12, 11, 10, 9 | out0_p, out0_n<br>out1_p, out1_n | **Differential Output (Analog Output).** Differential outputs. |
| 8, 13 | vdd | **Positive Supply Voltage.** 2.5$V_{DC}$ or 3.3 $V_{DC}$ nominal. |
| 5, 16 | gnd | **Ground.** 0 V. |
| 2, 3, 6, 7, 14, 15 | NC | **No Connection.** Leave unconnected. |
| Exposed Pad | | **Device GND**. |

## 3.0 Functional Description

The ZL40200 is an LVPECL clock fanout buffer with two identical output clock drivers capable of operating at frequencies up to 750MHz.

Inputs to the ZL40200 are externally terminated to allow use of precision termination components and to allow full flexibility of input termination. The ZL40200 can accept DC coupled LVPECL or LVDS and AC coupled LVPECL, LVDS, CML or HCSL input signals; single ended input signals can also be accepted. A pin compatible device with internal termination is also available.

The ZL40200 is designed to fan out low-jitter reference clocks for wired or optical communications applications while adding minimal jitter to the clock signal. An internal linear power supply regulator and bulk capacitors minimize additive jitter due to power supply noise. The device operates from 2.5V+/-5% or 3.3V+/-5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

The device block diagram is shown in Figure 1; its operation is described in the following sections.

### 3.1 Clock Inputs

The device can accept LVPECL, LVDS, CML, HCSL and single-ended inputs.

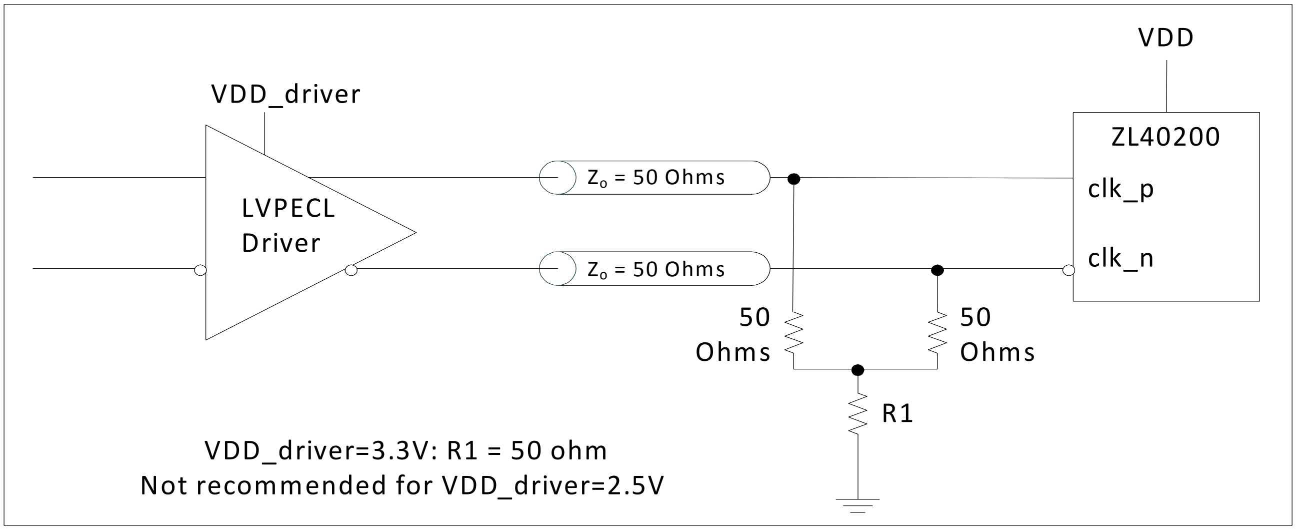


Figure 3 - LVPECL Input DC Coupled Thevenin Equivalent

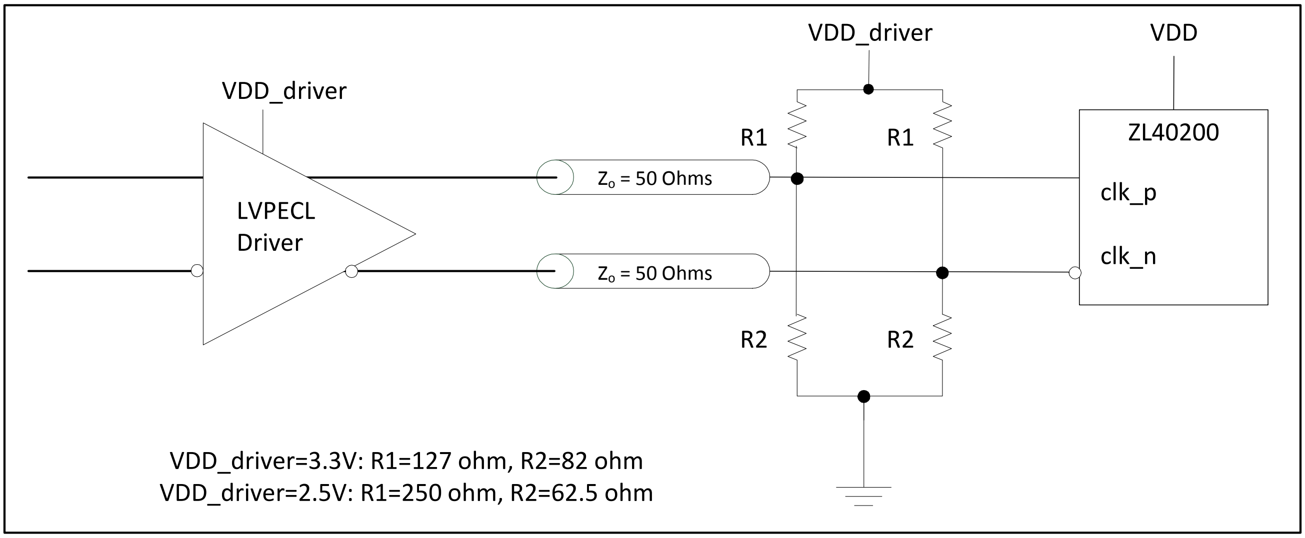


Figure 4 - LVPECL Input DC Coupled Parallel Termination

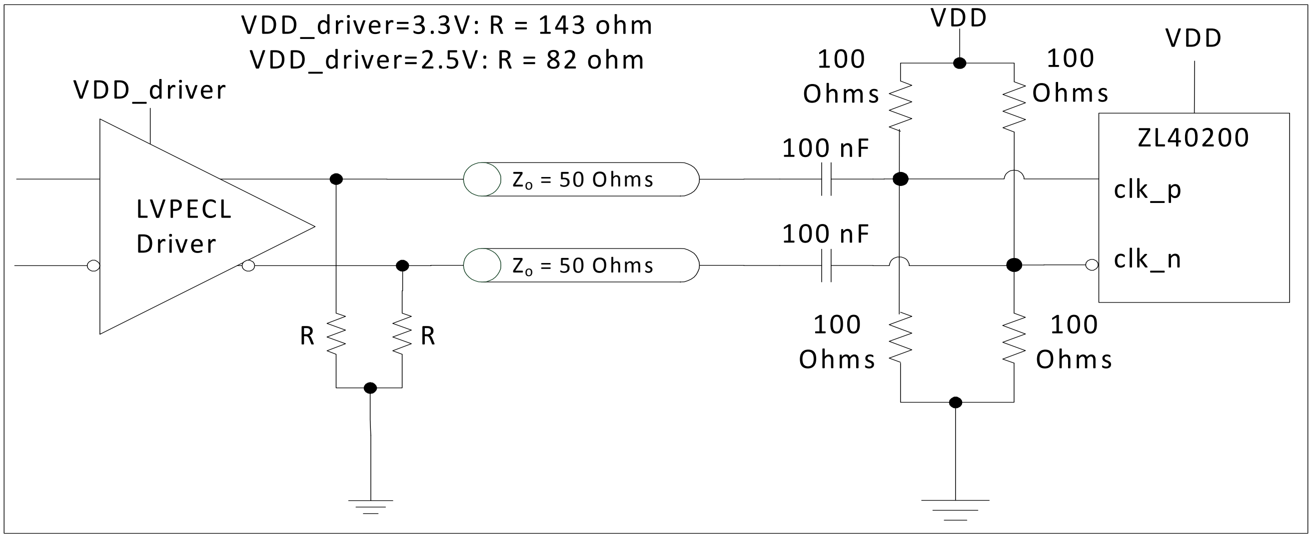


Figure 5 - LVPECL Input AC Coupled Termination

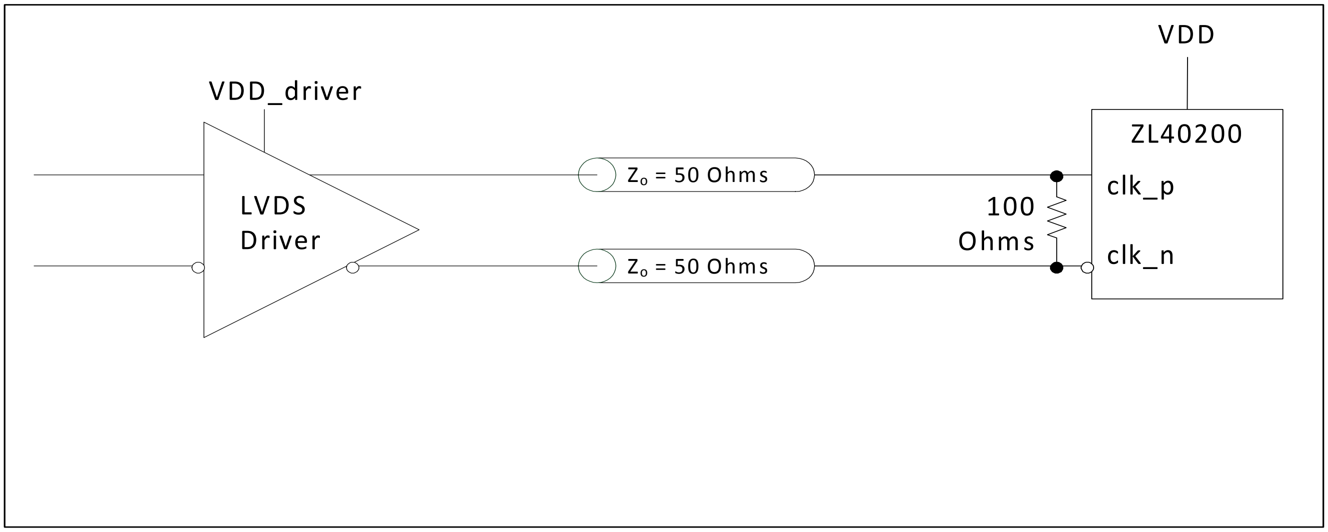


Figure 6 - LVDS Input DC Coupled

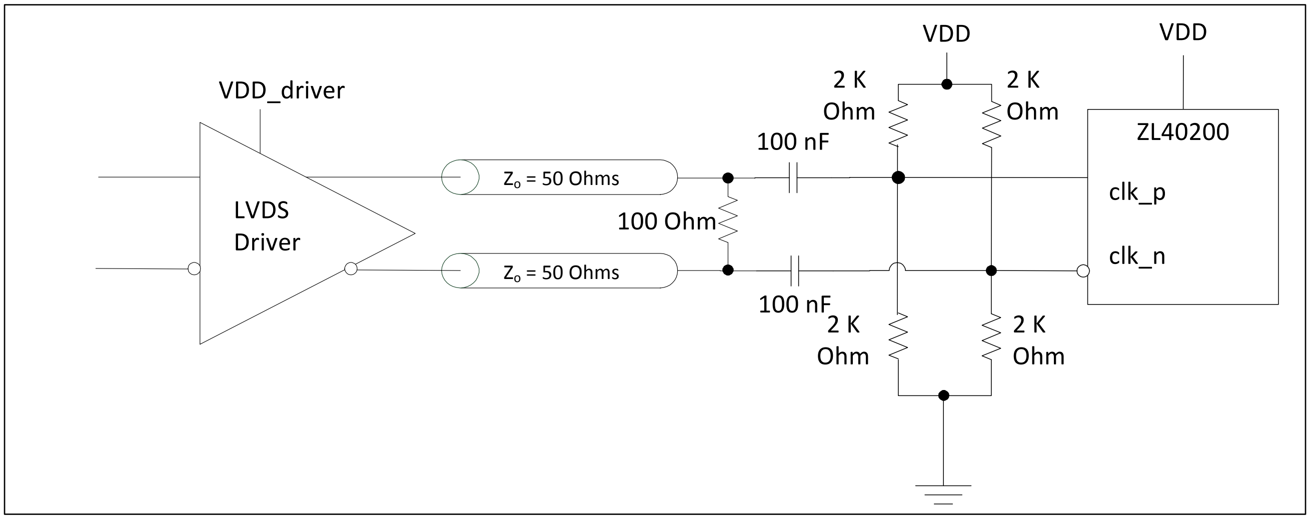


Figure 7 - LVDS Input AC Coupled

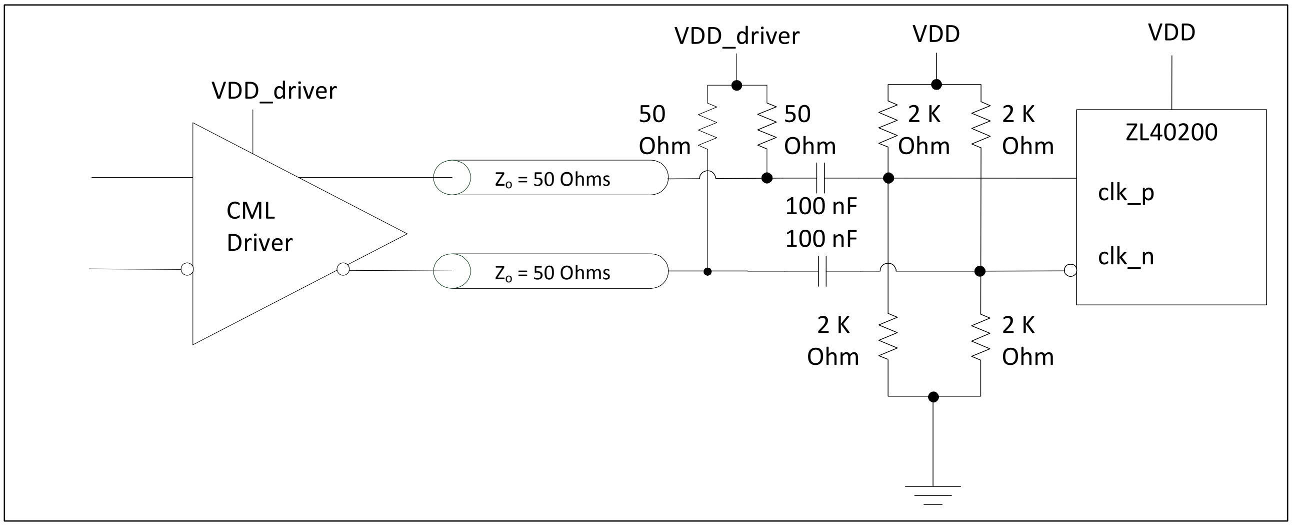


Figure 8 - CML Input AC Coupled

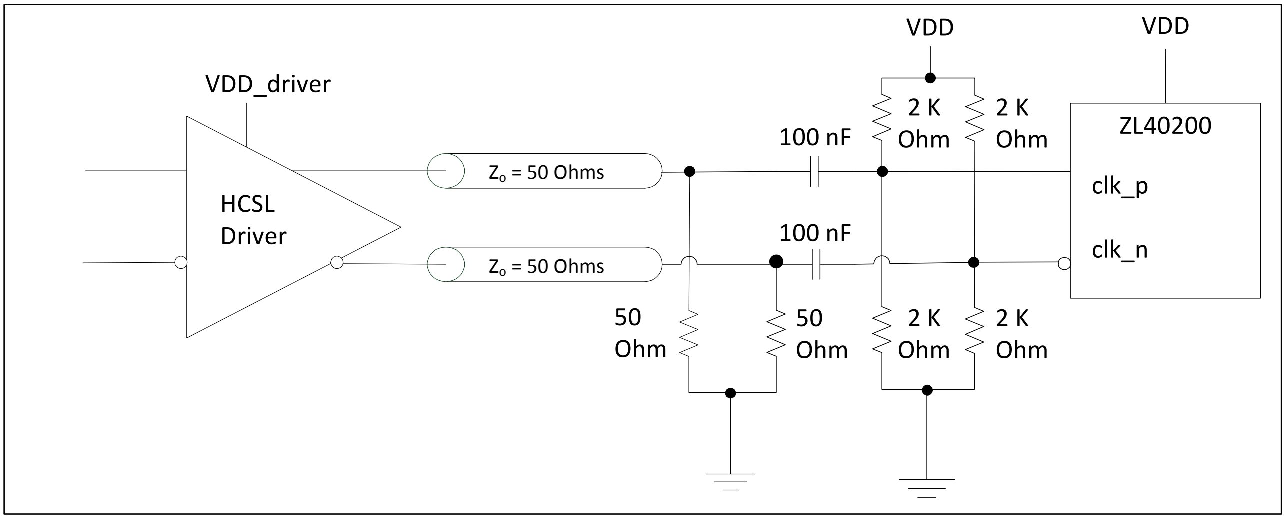


Figure 9 - HCSL Input AC Coupled

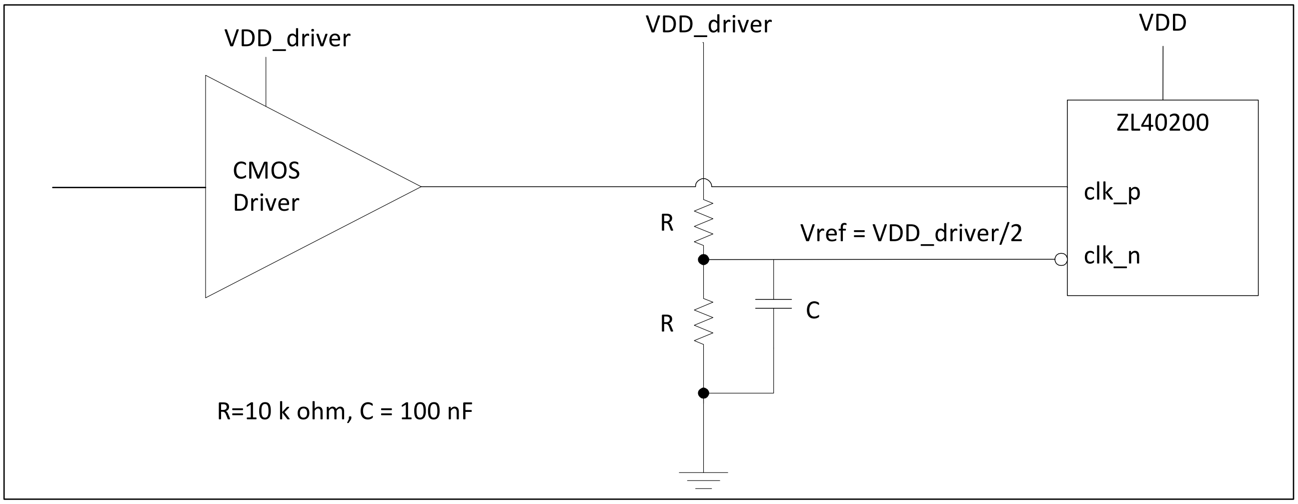


Figure 10 - CMOS Input DC Coupled Referenced to VDD/2

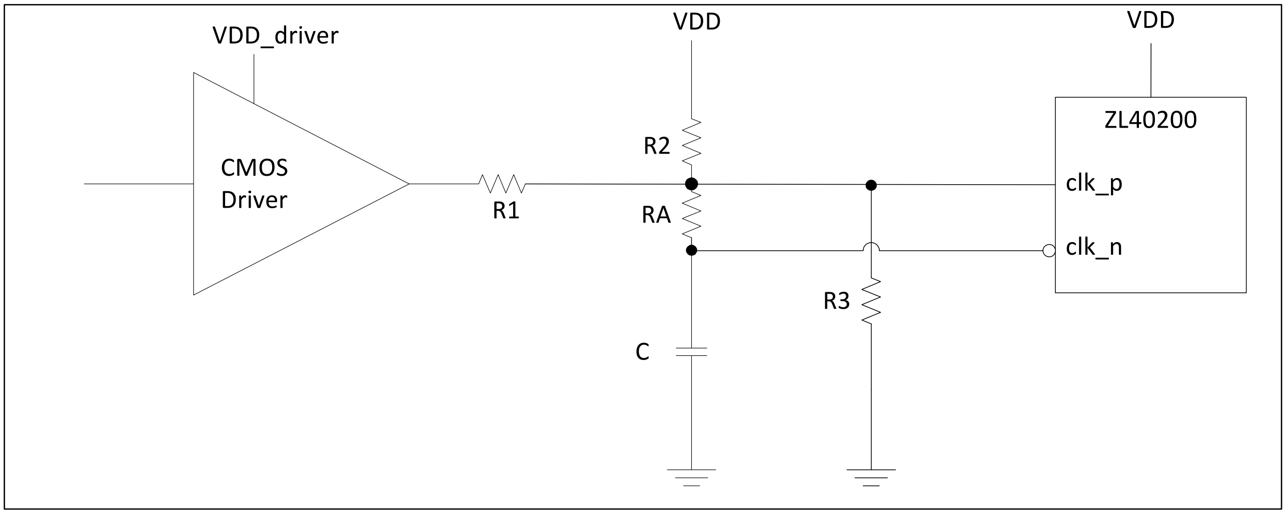


Figure 11 - CMOS Input DC Coupled Referenced to Ground

| VDD_driver | R1 (kΩ) | R2 (kΩ) | R3 (kΩ) | RA (kΩ) | C (pF) |
|---|---|---|---|---|---|
| 1.5 | 1.25 | 3.075 | open | 10 | 10 |
| 1.8 | 1 | 3.8 | open | 10 | 10 |
| 2.5 | 0.33 | 4.2 | open | 10 | 10 |
| 3.3 | 0.75 | open | 4.2 | 10 | 10 |

Table 1 - Component Values for Single Ended Input Reference to Ground

* For frequencies below 100 MHz, increase C to avoid signal integrity issues.

## 3.2 Clock Outputs

LVPECL has a very low output impedance and a differential signal swing between 1V and 1.6 V. A simplified diagram for the output stage is shown in Figure 12.The LVPECL to LVDS output termination is not shown since there is a separate device that has the same input and LVDS outputs.

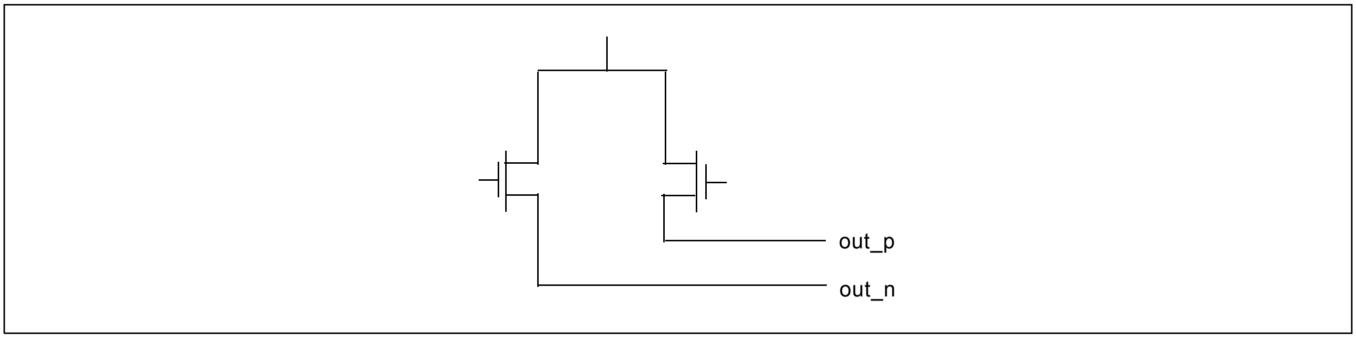


Figure 12 - Simplified Output Driver

The methods to terminate the ZL40200 LVPECL drivers are shown in the following figures.

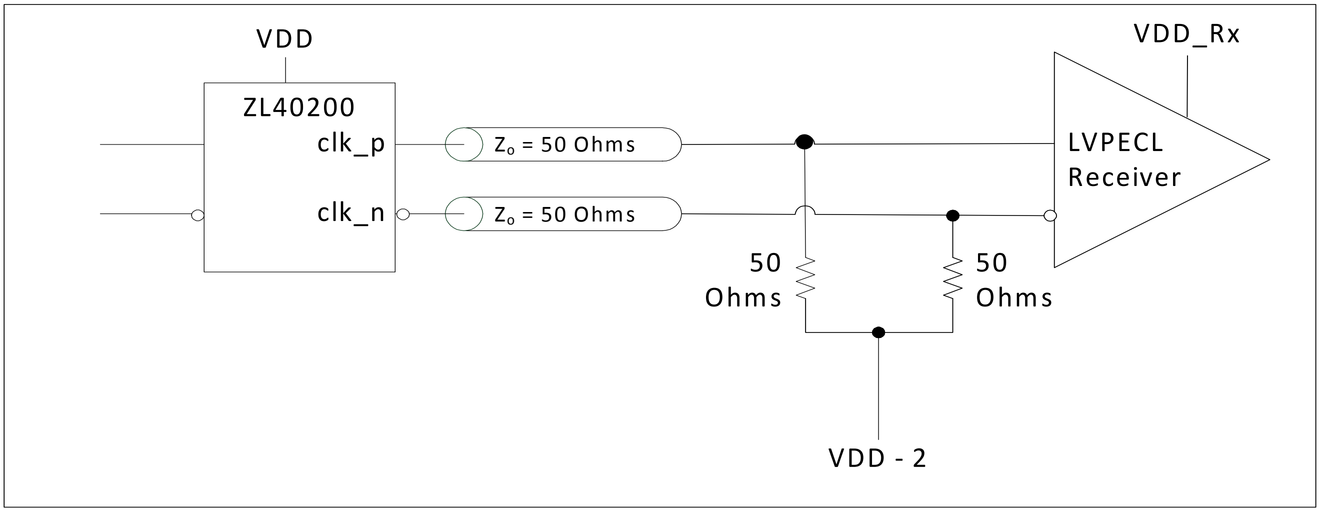


Figure 13 - LVPECL Basic Output Termination

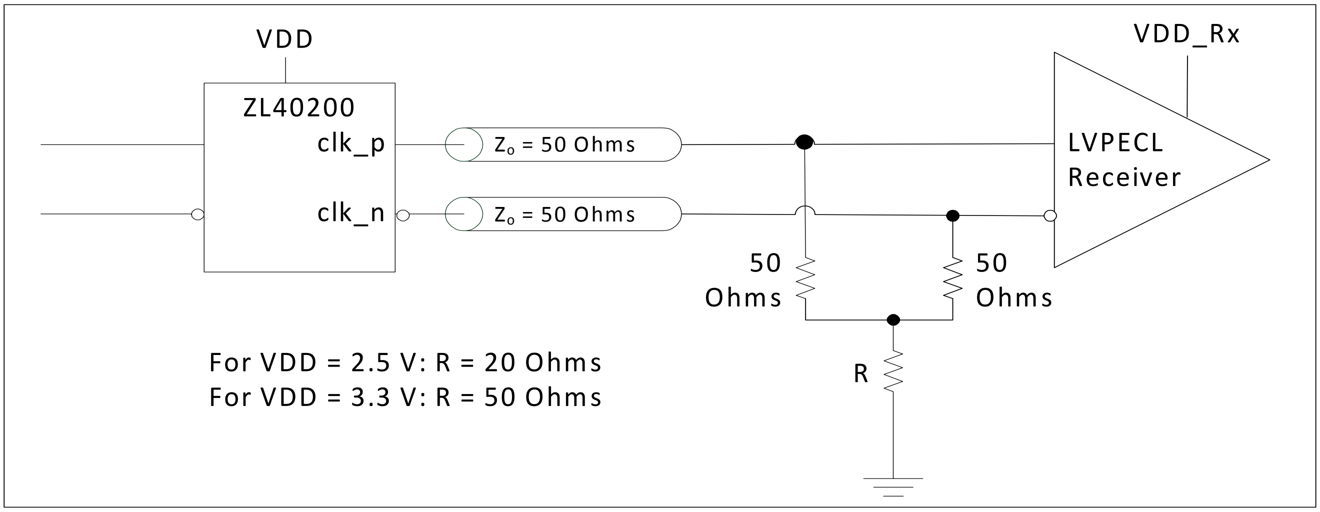


Figure 14 - LVPECL Parallel Output Termination

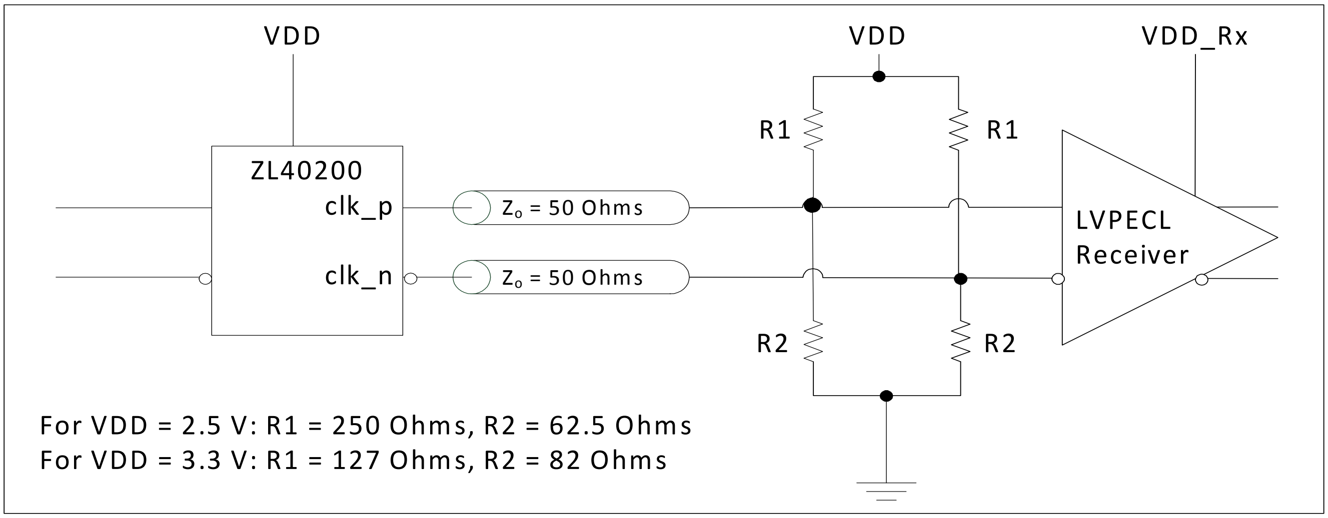


Figure 15 - LVPECL Parallel Thevenin-Equivalent Output Termination

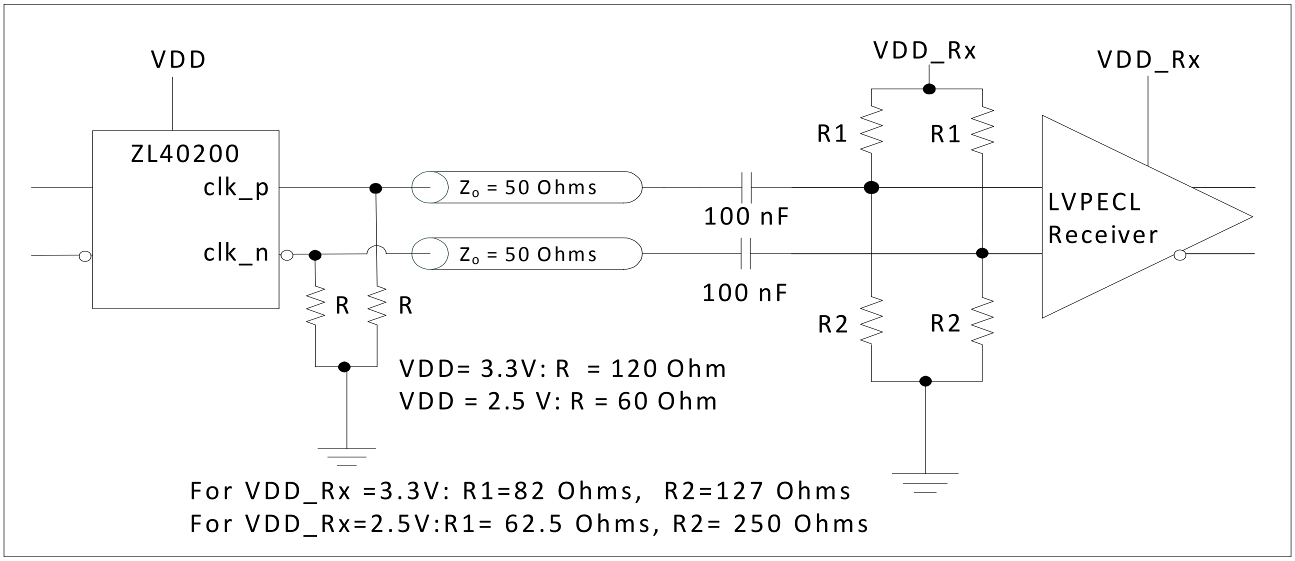


**Figure 16 - LVPECL AC Output Termination for Externally Terminated LVPECL Inputs**

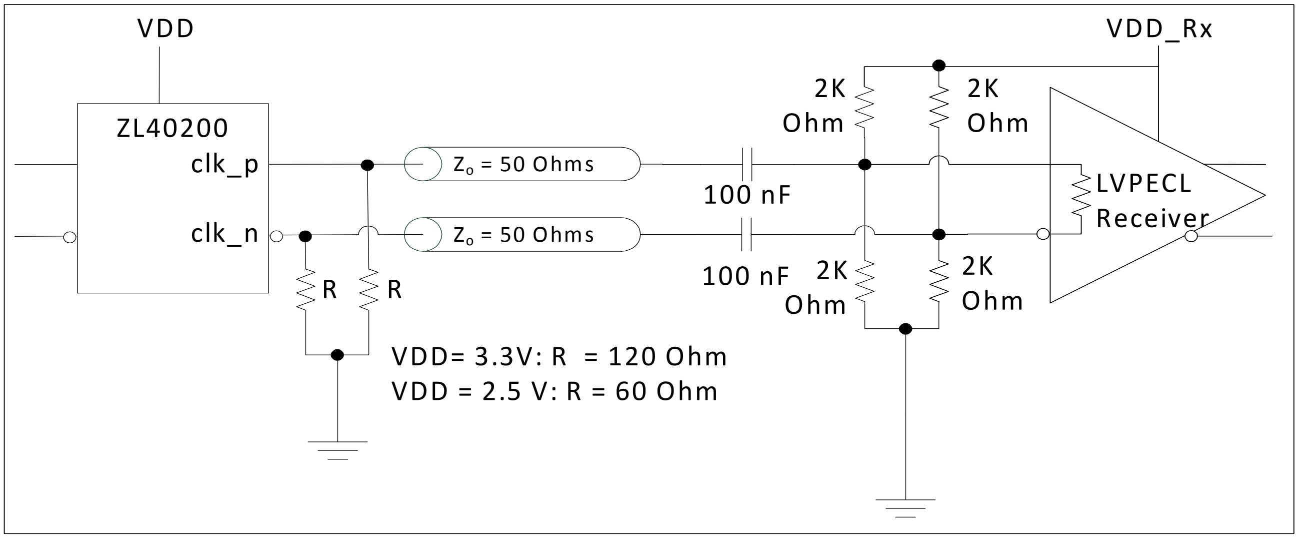


**Figure 17 - LVPECL AC Output Termination for Internally Terminated LVPECL Inputs**

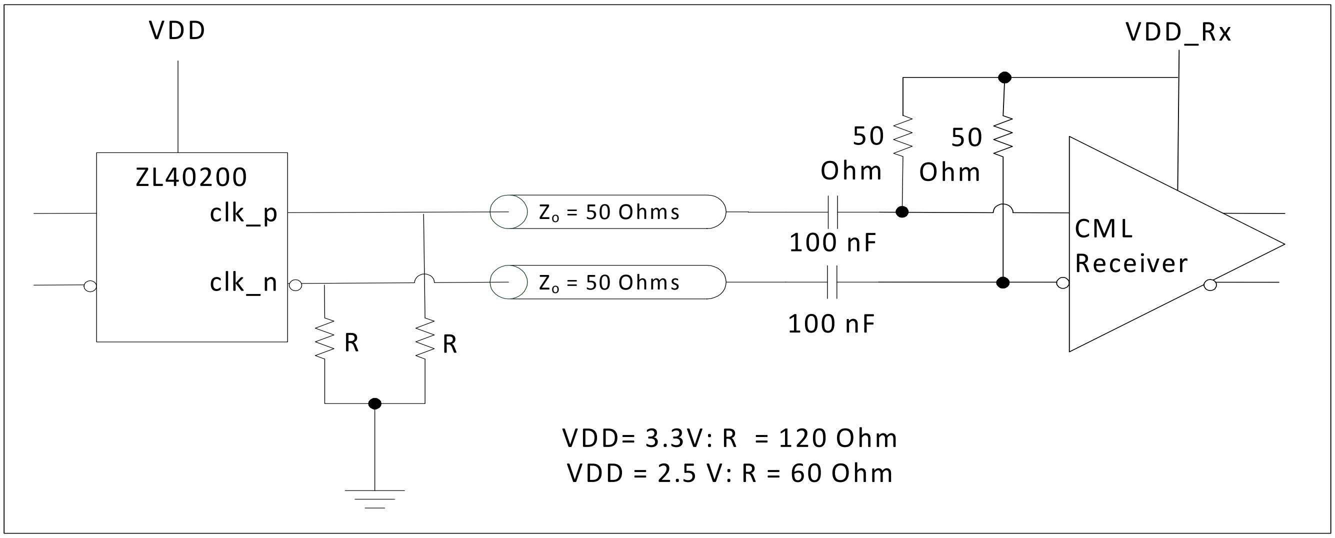


**Figure 18 - LVPECL AC-Coupled Output Termination for CML Inputs**

### 3.3 Device Additive Jitter

The ZL40200 clock fan out buffer is not intended to filter clock jitter. The jitter performance of this type of device is characterized by its additive jitter. Additive jitter is the jitter the device would add to a hypothetical jitter-free clock as it passes through the device. The additive jitter of the ZL40200 is random and as such it is not correlated to the jitter of the input clock signal.

The square of the resultant random RMS jitter at the output of the ZL40200 is equal to the sum of the squares of the various random RMS jitter sources including: input clock jitter; additive jitter of the buffer; and additive jitter due to power supply noise. There may be additional deterministic jitter sources that are not shown in Figure 19.

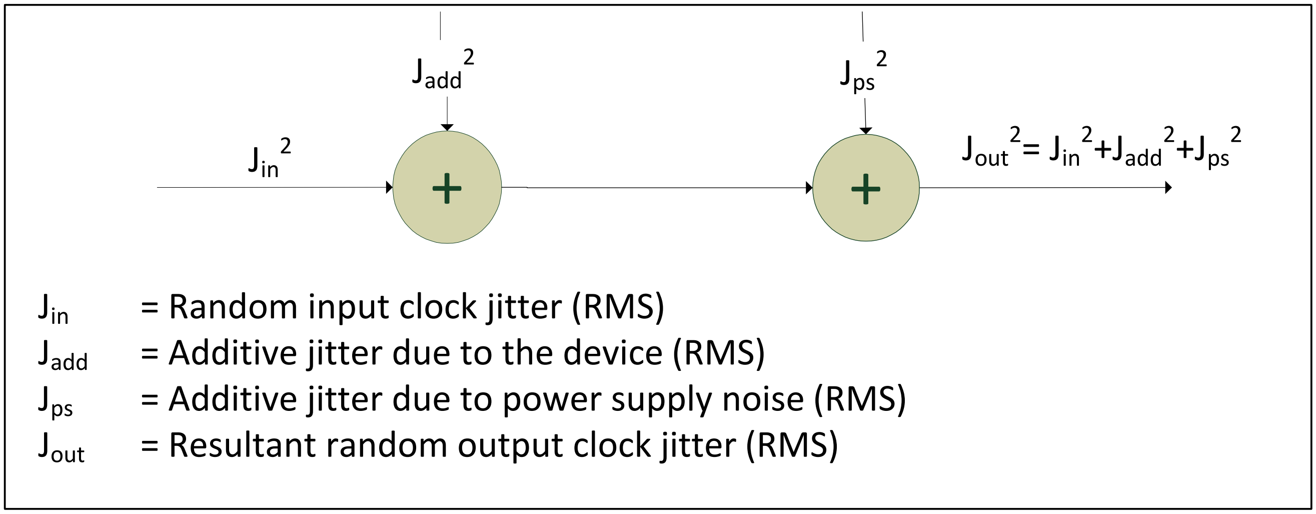


**Figure 19 - Additive Jitter**

## 3.4 Power Supply

This device operates with either a 2.5V supply or 3.3V supply.

### 3.4.1 Sensitivity to power supply noise

Power supply noise from sources such as switching power supplies and high-power digital components such as FPGAs can induce additive jitter on clock buffer outputs. The ZL40200 is equipped with a low drop out (LDO) power regulator and on-chip bulk capacitors to minimize additive jitter due to power supply noise. The LDO regulator on the ZL40200 allows this device to have superior performance even in the presence of external noise sources. The on-chip regulation, recommended power supply filtering, and good PCB layout all work together to minimize the additive jitter from power supply noise.

The performance of these clock buffers in the presence of power supply noise is detailed in ZLAN-403, “Power Supply Rejection in Clock Buffers” which is available from Applications Engineering.

### 3.4.2 Power supply filtering

For optimal jitter performance, the device should be isolated from the power planes connected to its power supply pins as shown in Figure 20.

- 10 μF capacitors should be size 0603 or size 0805 X5R or X7R ceramic, 6.3 V minimum rating
- 0.1 μF capacitors should be size 0402 X5R ceramic, 6.3 V minimum rating
- Capacitors should be placed next to the connected device power pins
- a 0.3 Ohm resistor is recommended for the filter shown in Figure 20

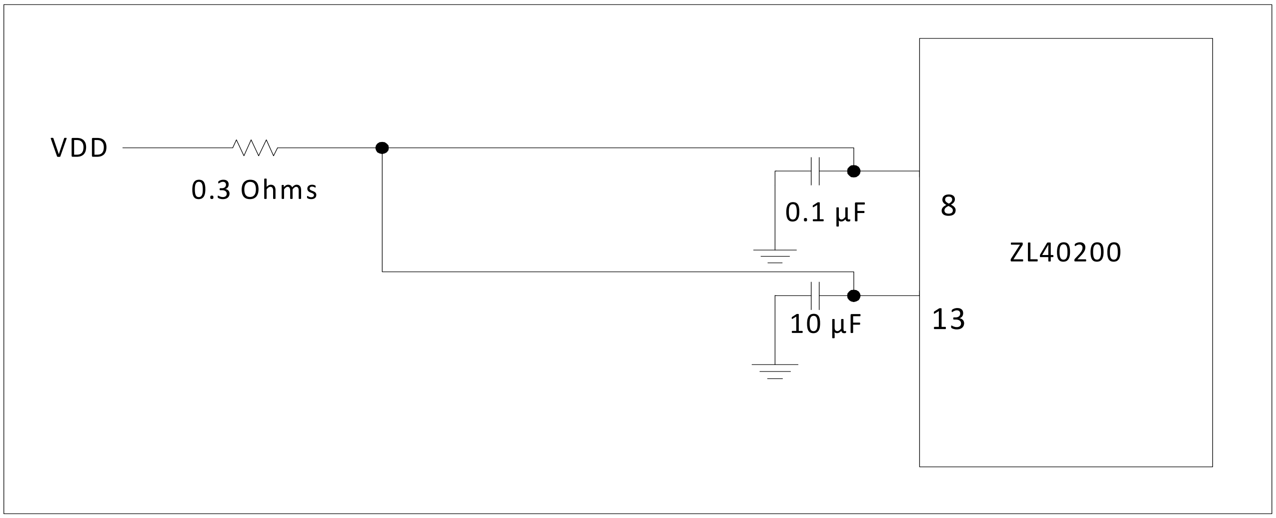


**Figure 20 - Decoupling Connections for Power Pins**

### 3.4.3 PCB layout considerations

The power nets in Figure 20 can be implemented either as a plane island or routed power topology without changing the overall jitter performance of the device.

## 4.0 AC and DC Electrical Characteristics

### Absolute Maximum Ratings*

| | Parameter | Sym. | Min. | Max. | Units |
|---|---|---|---|---|---|
| 1 | Supply voltage | $V_{DD\_R}$ | -0.5 | 4.6 | V |
| 2 | Voltage on any digital pin | $V_{PIN}$ | -0.5 | $V_{DD}$ | V |
| 3 | LVPECL output current | $I_{out}$ | | 30 | mA |
| 4 | Soldering temperature | T | | 260 | °C |
| 5 | Storage temperature | $T_{ST}$ | -55 | 125 | °C |
| 6 | Junction temperature | $T_j$ | | 125 | °C |
| 7 | Voltage on input pin | $V_{input}$ | | $V_{DD}$ | V |
| 8 | Input capacitance each pin | $C_p$ | | 500 | fF |

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
* Voltages are with respect to ground (GND) unless otherwise stated

### Recommended Operating Conditions*

| | Characteristics | Sym. | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| 1 | Supply voltage 2.5 V mode | $V_{DD25}$ | 2.375 | 2.5 | 2.625 | V |
| 2 | Supply voltage 3.3 V mode | $V_{DD33}$ | 3.135 | 3.3 | 3.465 | V |
| 3 | Operating temperature | $T_A$ | -40 | 25 | 85 | °C |

* Voltages are with respect to ground (GND) unless otherwise stated

### DC Electrical Characteristics - Current Consumption

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | Supply current LVPECL drivers - unloaded | $I_{dd\_unload}$ | | 49 | | mA | Unloaded |
| 2 | Supply current LVPECL drivers - loaded (all outputs are active) | $I_{dd\_load}$ | | 88 | | mA | Including power to $R_L = 50\Omega$ |

### DC Electrical Characteristics - Inputs and Outputs - for 3.3 V Supply

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | Differential input common mode voltage | $V_{CM}$ | 1.1 | | 2.0 | V | |
| 2 | Differential input voltage difference | $V_{ID}$ | 0.25 | | 1 | V | |
| 3 | LVPECL output high voltage | $V_{OH}$ | $V_{DD}$-1.40 | | | V | Measured at 10 MHz |
| 4 | LVPECL output low voltage | $V_{OL}$ | | | $V_{DD}$-1.62 | V | Measured at 10 MHz |

### DC Electrical Characteristics - Inputs and Outputs - for 3.3 V Supply

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 5 | LVPECL output differential voltage | $V_{OD}$ | 0.5 | | 0.9 | V | |

* The VOD parameter was measured from 125 MHz to 750 MHz.

### DC Electrical Characteristics - Inputs and Outputs - for 2.5 V Supply

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | Differential input common mode voltage | $V_{CM}$ | 1.1 | | 1.6 | V | |
| 2 | Differential input voltage difference | $V_{ID}$ | 0.25 | | 1 | V | |
| 3 | LVPECL output high voltage | $V_{OH}$ | $V_{DD}$-1.40 | | | V | |
| 4 | LVPECL output low voltage | $V_{OL}$ | | | $V_{DD}$-1.62 | V | |
| 5 | LVPECL output differential voltage* | $V_{OD}$ | 0.4 | | 0.9 | V | |

* The VOD parameter was measured from 125 MHz to 750 MHz.

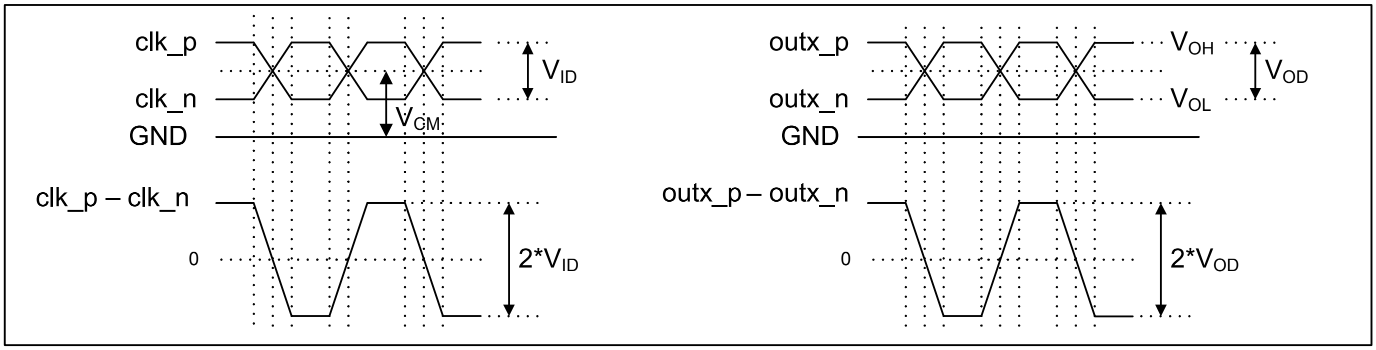


**Figure 21 - Differential Voltage Parameter**

### AC Electrical Characteristics* - Inputs and Outputs (see Figure 22) - for 3.3 V supply.

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | Maximum Operating Frequency | $1/t_p$ | | | 750 | MHz | |
| 2 | input to output clock propagation delay | $t_{pd}$ | 0 | 1 | 2 | ns | |
| 3 | output to output skew | $t_{out2out}$ | | 50 | 100 | ps | |
| 4 | part to part output skew | $t_{part2part}$ | | 80 | 300 | ps | |
| 5 | Output clock Duty Cycle degradation | $t_{PWH}/ t_{PWL}$ | -2% | 0% | 2% | Duty Cycle | |
| 6 | LVPECL Output Slew Rate | $r_{sk}$ | 0.75 | 1.2 | | V/ns | |

* Supply voltage and operating temperature are as per Recommended Operating Conditions

**AC Electrical Characteristics* - Inputs and Outputs (see Figure 22) - for 2.5 V supply.**

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | Maximum Operating Frequency | $1/t_p$ | | | 750 | MHz | |
| 2 | input to output clock propagation delay | $t_{pd}$ | 0 | 1 | 2 | ns | |
| 3 | output to output skew | $t_{out2out}$ | | 50 | 100 | ps | |
| 4 | part to part output skew | $t_{part2part}$ | | 80 | 300 | ps | |
| 5 | Output clock Duty Cycle degradation | $t_{PWH}/ t_{PWL}$ | -2 | 0 | 2 | Percent | |
| 6 | LVPECL Output Slew Rate | $r_{sk}$ | 0.75 | 1.2 | | ps | |

* Supply voltage and operating temperature are as per Recommended Operating Conditions

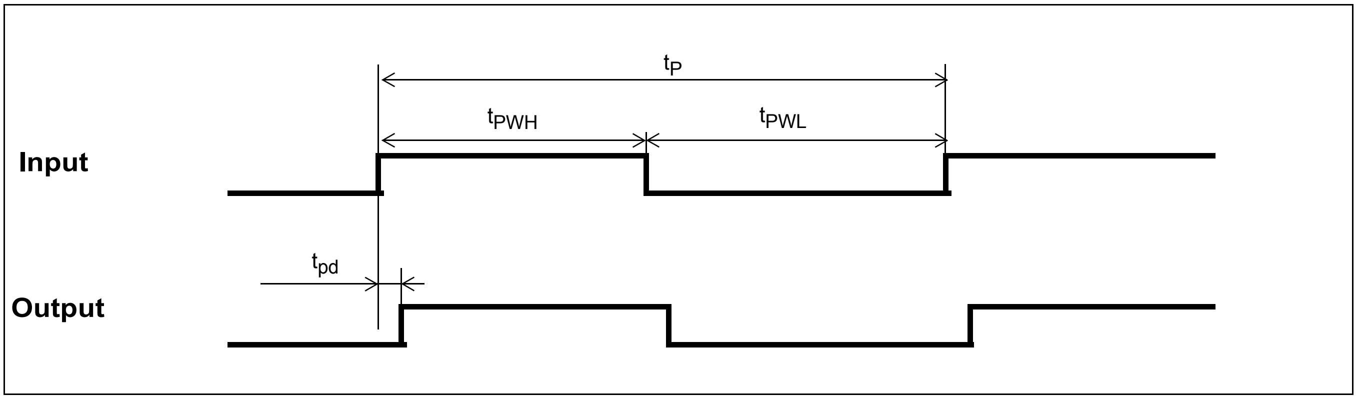


Figure 22 - Input To Output Timing

## 5.0 Performance Characterization

### Additive Jitter at 2.5 V*

| | Output Frequency (MHz) | Jitter Measurement Filter | Typical RMS (fs) | Notes |
|---|---|---|---|---|
| 1 | 125 | 12 kHz - 20 MHz | 112 | |
| 2 | 212.5 | 12 kHz - 20 MHz | 80 | |
| 3 | 311.04 | 12 kHz - 20 MHz | 70 | |
| 4 | 425 | 12 kHz - 20 MHz | 65 | |
| 5 | 500 | 12 kHz - 20 MHz | 56 | |
| 6 | 622.08 | 12 kHz - 20 MHz | 43 | |
| 7 | 750 | 12 kHz - 20 MHz | 39 | |

*The values in this table were taken with an approximate slew rate of 0.8 V/ns.

### Additive Jitter at 3.3 V*

| | Output Frequency (MHz) | Jitter Measurement Filter | Typical RMS (fs) | Notes |
|---|---|---|---|---|
| 1 | 125 | 12 kHz - 20 MHz | 112 | |
| 2 | 212.5 | 12 kHz - 20 MHz | 82 | |
| 3 | 311.04 | 12 kHz - 20 MHz | 72 | |
| 4 | 425 | 12 kHz - 20 MHz | 63 | |
| 5 | 500 | 12 kHz - 20 MHz | 52 | |
| 6 | 622.08 | 12 kHz - 20 MHz | 43 | |
| 7 | 750 | 12 kHz - 20 MHz | 39 | |

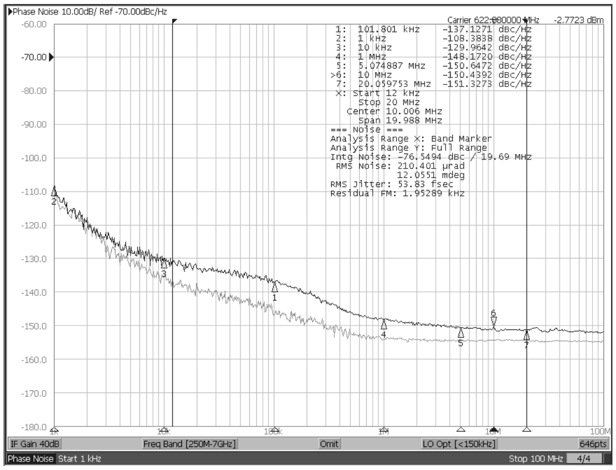
*The values in this table were taken with an approximate slew rate of 0.8 V/ns.

### Additive Jitter from a Power Supply Tone*

| Carrier Frequency (MHz) | Parameter | Typical | Units | Notes |
|---|---|---|---|---|
| 125MHz | 25 mV at 100 kHz | 159 | fs RMS | |
| 750MHz | 25 mV at 100 kHz | 82 | fs RMS | |

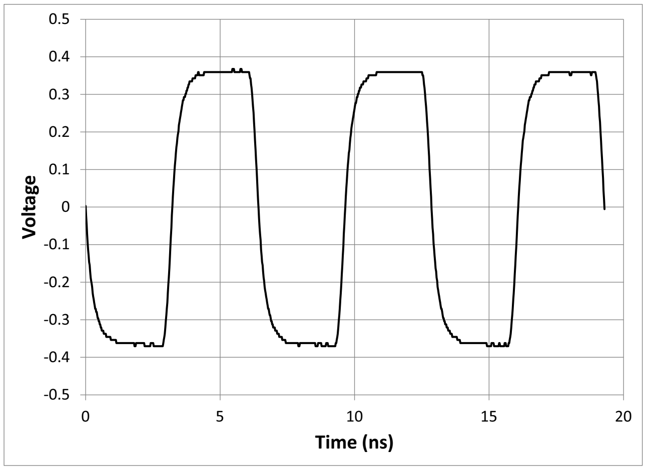
* The values in this table are the additive periodic jitter caused by an interfering tone typically caused by a switching power supply. For this test, measurements were taken over the full temperature and voltage range for $V_{DD}$ = 3.3 V. The magnitude of the interfering tone is measured at the DUT.

## 6.0 Typical Behavior

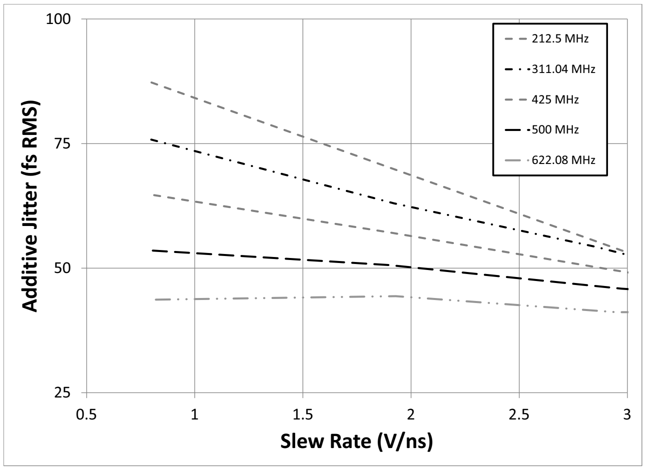


```
 1:  101.801 kHz     -137.1271 dBc/Hz
 2:  1 kHz           -108.3838 dBc/Hz
 3:  10 kHz          -129.9642 dBc/Hz
 4:  1 MHz           -148.1720 dBc/Hz
 5:  5.074887 MHz    -150.6472 dBc/Hz
>6:  10 MHz          -150.4392 dBc/Hz
 7:  20.059753 MHz   -151.3273 dBc/Hz
 X: Start 12 kHz
      Stop 20 MHz
    Center 10.006 MHz
      Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Full Range
Intg Noise: -76.5494 dBc / 19.69 MHz
 RMS Noise: 210.401 µrad
            12.0551 mdeg
RMS Jitter: 53.83 fsec
Residual FM: 1.95289 kHz
```

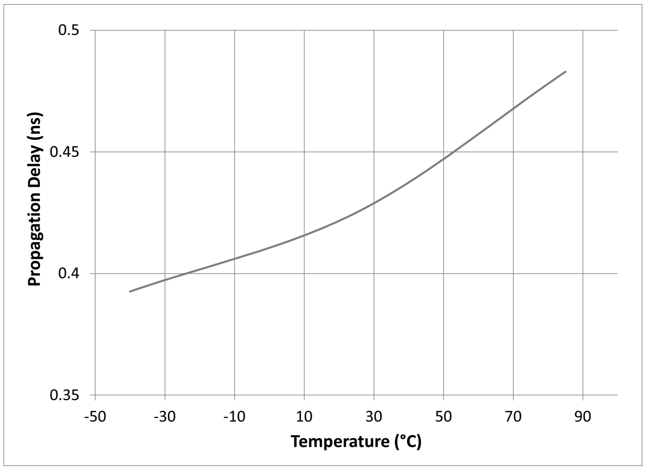
Typical Phase Noise at 622.08 MHz



Typical Waveform at 155.52 MHz

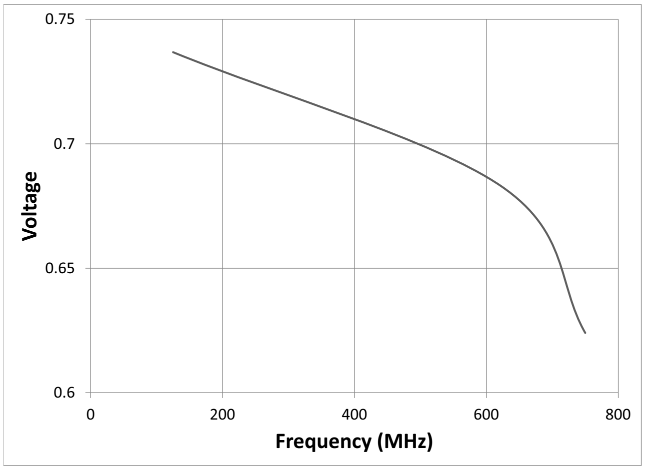


Input Slew Rate versus Additive Jitter

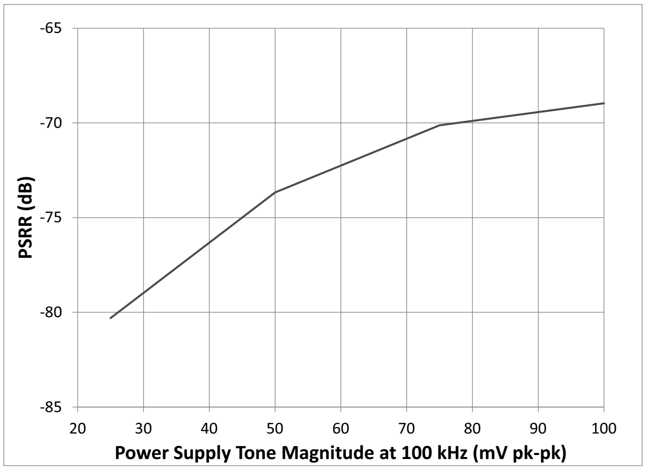


Propagation Delay versus Temperature

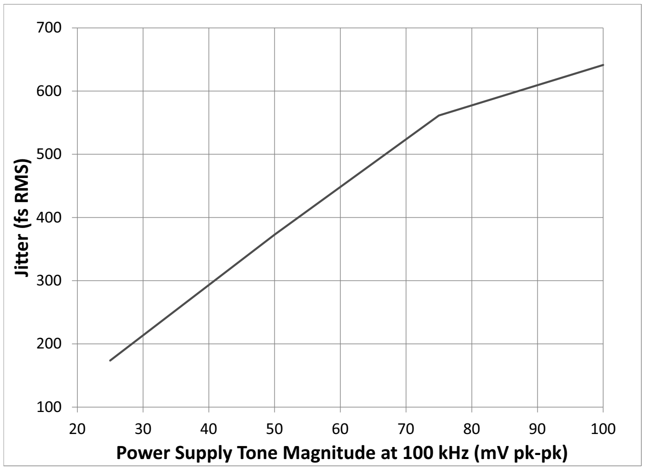
Note: This is for a single device. For more details see the characterization section.



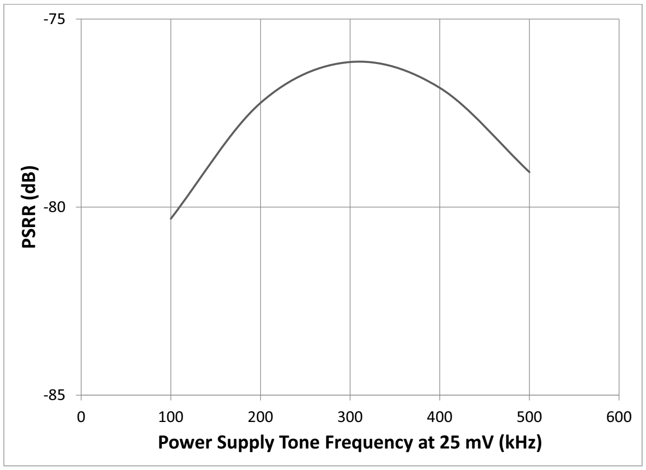
$V_{OD}$ versus Frequency



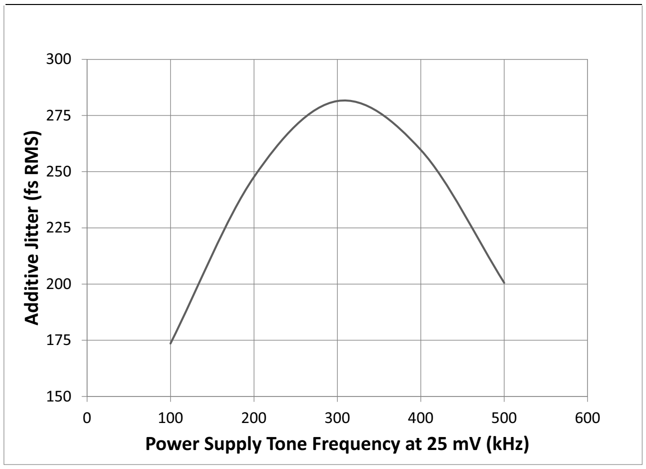
Power Supply Tone Magnitude versus PSRR (at 100 kHz) at 125 MHz



Power Supply Tone Magnitude versus Additive Jitter (at 100 kHz) at 125 MHz



Power Supply Tone Frequency (at 25 mV) versus PSRR at 125 MHz



Power Supply Tone Frequency (at 25 mV) versus Additive Jitter at 125 MHz

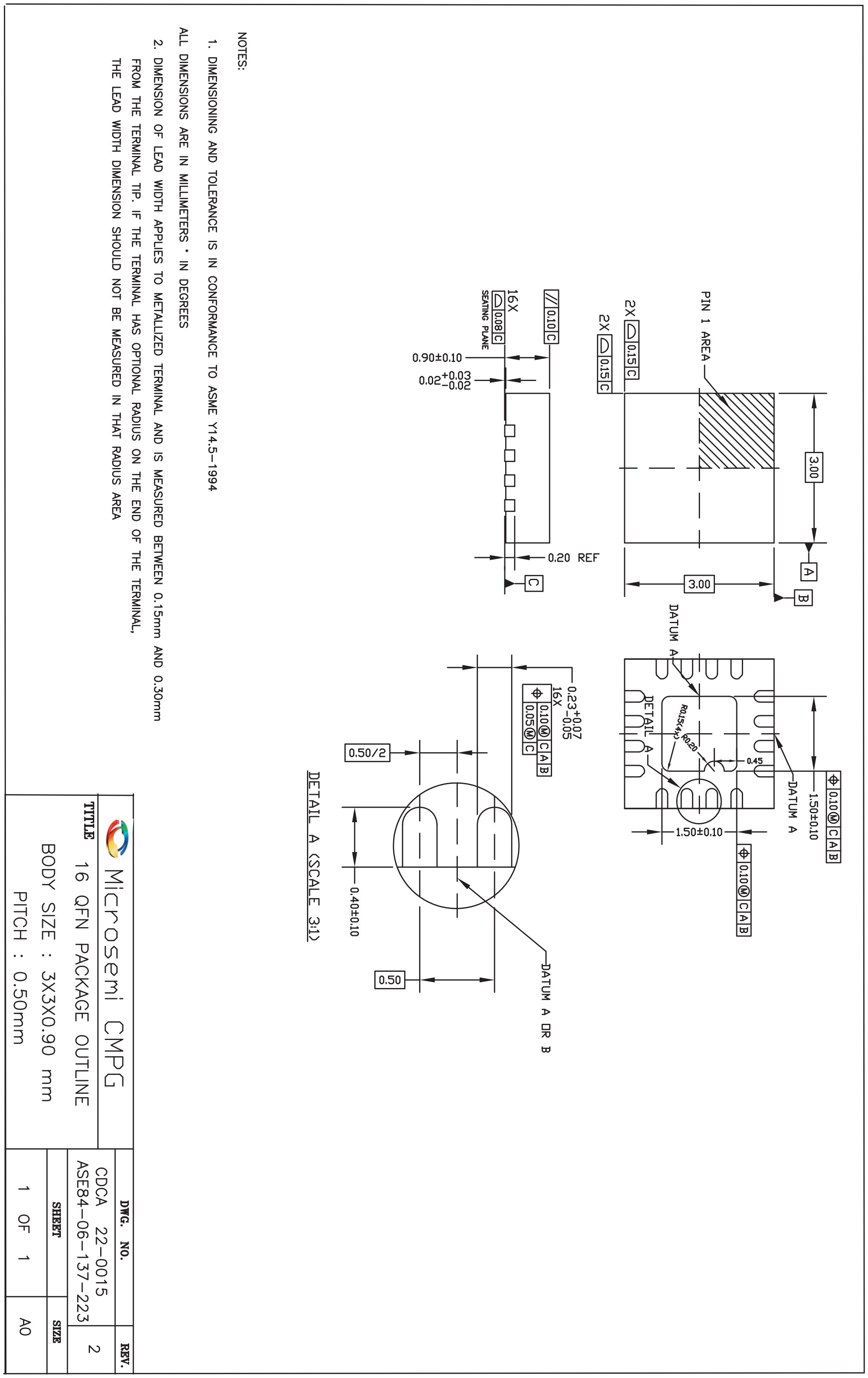
## 7.0 Package Thermal Characteristics

**Thermal Data**

| Parameter | Symbol | Test Condition | Value | Unit |
|---|---|---|---|---|
| Junction to Ambient Thermal Resistance | $\Theta_{JA}$ | Still Air<br>1 m/s<br>2 m/s | 67.9<br>61.6<br>58.1 | $^oC/W$ |
| Junction to Case Thermal Resistance | $\Theta_{JC}$ | Still Air | 44.1 | $^oC/W$ |
| Junction to Board Thermal Resistance | $\Theta_{JB}$ | Still Air | 23.2 | $^oC/W$ |
| Maximum Junction Temperature* | $T_{jmax}$ | | 125 | $^oC$ |
| Maximum Ambient Temperature | $T_A$ | | 85 | $^oC$ |

* Proper thermal management must be practiced to ensure that $T_{jmax}$ is not exceeded.

## 8.0 Mechanical Drawing



NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5-1994

ALL DIMENSIONS ARE IN MILLIMETERS ° IN DEGREES

2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

Microsemi CMPG

| | | |
|---|---|---|
| TITLE 16 QFN PACKAGE OUTLINE<br>BODY SIZE : 3X3X0.90 mm<br>PITCH : 0.50mm | DWG. NO.<br>CDCA 22-0015<br>ASE84-06-137-223 | REV.<br>2 |
| | SHEET<br>1 OF 1 | SIZE<br>A0 |

Information relating to products and services furnished herein by Microsemi Corporation or its subsidiaries (collectively “Microsemi”) is believed to be reliable. However, Microsemi assumes no liability for errors that may appear in this publication, or for liability otherwise arising from the application or use of any such information, product or service or for any infringement of patents or other intellectual property rights owned by third parties which may result from such application or use. Neither the supply of such information or purchase of product or service conveys any license, either express or implied, under patents or other intellectual property rights owned by Microsemi or licensed from third parties by Microsemi, whatsoever. Purchasers of products are also hereby notified that the use of product in certain ways or in combination with Microsemi, or non-Microsemi furnished goods or services may infringe patents or other intellectual property rights owned by Microsemi.

This publication is issued to provide information only and (unless agreed by Microsemi in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. The products, their specifications, services and other information appearing in this publication are subject to change by Microsemi without notice. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user’s responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. Manufacturing does not necessarily include testing of all functions or parameters. These products are not suitable for use in any medical and other products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to Microsemi’s conditions of sale which are available on request.

For more information about all Microsemi products
visit our website at
www.microsemi.com

TECHNICAL DOCUMENTATION – NOT FOR RESALE

Microsemi Corporate Headquarters One
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
E-mail: sales.support@microsemi.com

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense and security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world’s standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif. and has approximately 3,400 employees globally. Learn more at www.microsemi.com.

© 2014 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.