

CD4019BC Quad AND-OR Select Gate

General Description

The CD4019BC is a complementary MOS quad AND-OR select gate. Low power and high noise margin over a wide voltage range is possible through implementation of N- and P-channel enhancement mode transistors. These complementary MOS (CMOS) transistors provide the building blocks for the 4 "AND-OR select" gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_A and K_B . All inputs are protected against static discharge damage.

Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: $0.45 V_{DD}$ (typ.)
- Low power TTL compatibility: Fan out of 2 driving 74L or 1 driving 74LS

Applications

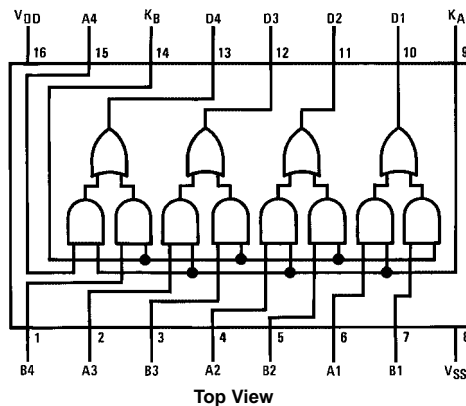
- AND-OR select gating
- Shift-right/shift-left registers
- True/complement selection
- AND/OR/EXCLUSIVE-OR selection

Ordering Code:

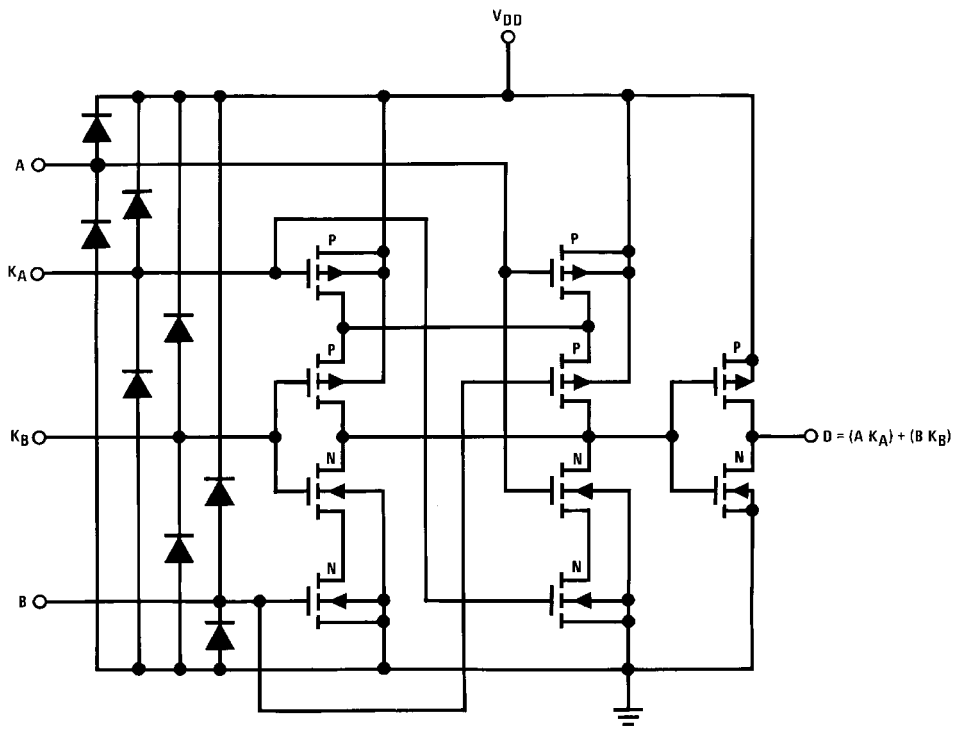
| Order Number | Package Number | Package Description |
|--------------|----------------|--|
| CD4019BCM | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| CD4019BCN | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Schematic Diagram



Schematic diagram for 1 of 4 identical stages

Absolute Maximum Ratings (Note 1)

(Note 2)

| | |
|-------------------------------------|--------------------------|
| Supply Voltage (V_{DD}) | -0.5V to +18V |
| Input Voltage (V_{IN}) | -0.5V to $V_{DD} + 0.5V$ |
| Storage Temperature Range (T_S) | -65°C to +150°C |
| Power Dissipation (P_D) | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| Lead Temperature (T_L) | |
| (Soldering, 10 seconds) | 260°C |

Recommended Operation Conditions (Note 2)

| | |
|---------------------------------------|-----------------|
| DC Supply Voltage (V_{DD}) | +3V to +15V |
| Input Voltage (V_{IN}) | 0V to $V_{DD}V$ |
| Operating Temperature Range (T_A) | -55°C to +125°C |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

DC Electrical Characteristics (Note 3)

| Symbol | Parameter | Conditions | -55°C | | +25°C | | | +125°C | | Units |
|----------|------------------------------------|---------------------------------------|-------|------|-------|------------|-------|--------|------|---------|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| I_{DD} | Quiescent Device Current | $V_{DD} = 5V$ | | 0.25 | | 0.25 | 1 | | 7.5 | μA |
| | | $V_{DD} = 10V$ | | 0.5 | | 0.5 | 2 | | 15 | |
| | | $V_{DD} = 15V$ | | 1.0 | | 1.0 | 4 | | 30 | |
| V_{OL} | LOW Level Output Voltage | $ I_{OL} < 1 \mu A$ | | | | | | | | V |
| | | $V_{DD} = 5V$ | | 0.05 | | 0 | 0.05 | | 0.05 | |
| | | $V_{DD} = 10V$ | | 0.05 | | 0 | 0.05 | | 0.05 | |
| V_{OH} | HIGH Level Output Voltage | $ I_{OL} < 1 \mu A$ | | | | | | | | V |
| | | $V_{DD} = 5V$ | 4.95 | | 4.95 | 5 | | 4.95 | | |
| | | $V_{DD} = 10V$ | 9.95 | | 9.95 | 10 | | 9.95 | | |
| V_{IL} | LOW Level Input Voltage | $V_{DD} = 5V, V_O = 0.5V$ or $4.5V$ | | 1.5 | | 2 | 1.5 | | 1.5 | V |
| | | $V_{DD} = 10V, V_O = 1.0V$ or $9.0V$ | | 3.0 | | 4 | 3.0 | | 3.0 | |
| | | $V_{DD} = 15V, V_O = 1.5V$ or $13.5V$ | | 4.0 | | 6 | 4.0 | | 4.0 | |
| V_{IH} | HIGH Level Input Voltage | $V_{DD} = 5V, V_O = 0.5V$ or $4.5V$ | 3.5 | | 3.5 | 3 | | 3.5 | | V |
| | | $V_{DD} = 10V, V_O = 1.0V$ or $9.0V$ | 7.0 | | 7.0 | 6 | | 7.0 | | |
| | | $V_{DD} = 15V, V_O = 1.5V$ or $13.5V$ | 11.0 | | 11.0 | 9 | | 11.0 | | |
| I_{OL} | LOW Level Output Current (Note 4) | $V_{DD} = 5V, V_O = 0.4V$ | 0.64 | | 0.51 | 1 | | 0.36 | | mA |
| | | $V_{DD} = 10V, V_O = 0.5V$ | 1.6 | | 1.3 | 2.5 | | 0.9 | | |
| | | $V_{DD} = 15V, V_O = 1.5V$ | 4.2 | | 3.4 | 10 | | 2.4 | | |
| I_{OH} | HIGH Level Output Current (Note 4) | $V_{DD} = 5V, V_O = 4.6V$ | -0.25 | | -0.2 | -0.4 | | -0.14 | | mA |
| | | $V_{DD} = 10V, V_O = 9.5V$ | -0.62 | | -0.5 | -1.0 | | -0.35 | | |
| | | $V_{DD} = 15V, V_O = 13.5V$ | -1.8 | | -1.5 | -3.0 | | -1.1 | | |
| I_{IN} | Input Current | $V_{DD} = 15V, V_{IN} = 0V$ | | -0.1 | | -10^{-5} | -0.10 | | -1.0 | μA |
| | | $V_{DD} = 15V, V_{IN} = 15V$ | | 0.1 | | 10^{-5} | 0.10 | | 1.0 | |

Note 3: $V_{SS} = 0V$ unless otherwise specified.

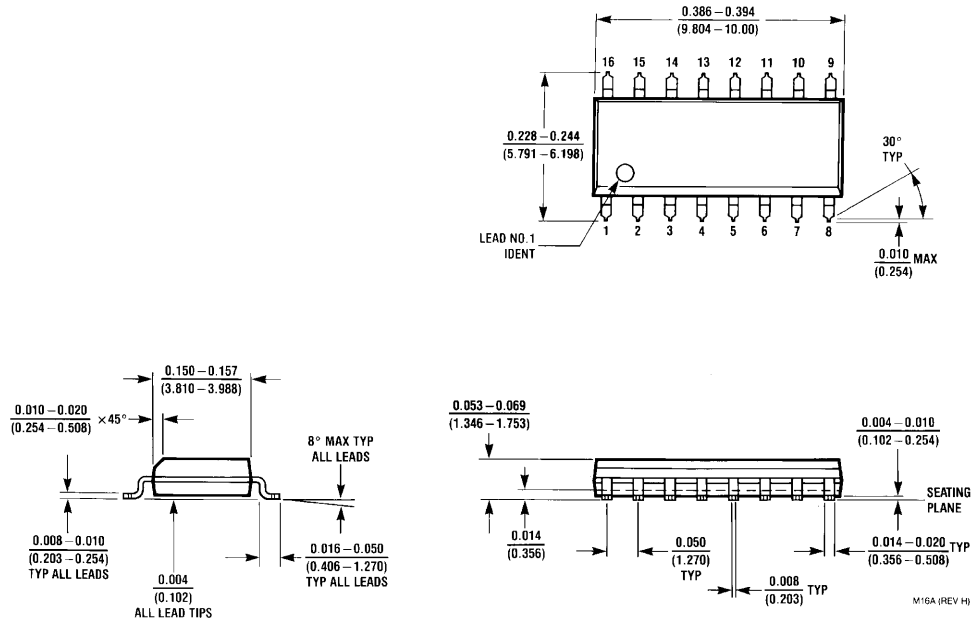
Note 4: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics (Note 5) $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}$, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------|---------------------------------------|------------------------|-----|-----|-----|-------|
| t_{PHL} | Propagation Delay, Input to Output | $V_{DD} = 5\text{V}$ | | 100 | 300 | ns |
| t_{PLH} | | $V_{DD} = 10\text{V}$ | | 50 | 120 | |
| | | $V_{DD} = 15\text{V}$ | | 45 | 100 | |
| t_{THL} | HIGH-to-LOW Level Transition Time | $V_{DD} = 5\text{V}$ | | 100 | 200 | ns |
| | | $V_{DD} = 10\text{V}$ | | 50 | 100 | |
| | | $V_{DD} = 15\text{V}$ | | 40 | 80 | |
| t_{TLH} | LOW-to-HIGH Level Transition Time | $V_{DD} = 5\text{V}$ | | 150 | 300 | ns |
| | | $V_{DD} = 10\text{V}$ | | 70 | 140 | |
| | | $V_{DD} = 15\text{V}$ | | 50 | 100 | |
| C_{IN} | Input Capacitance | All A and B Inputs | | 5 | 7.5 | pF |
| | | K_A and K_B Inputs | | 10 | 15 | |

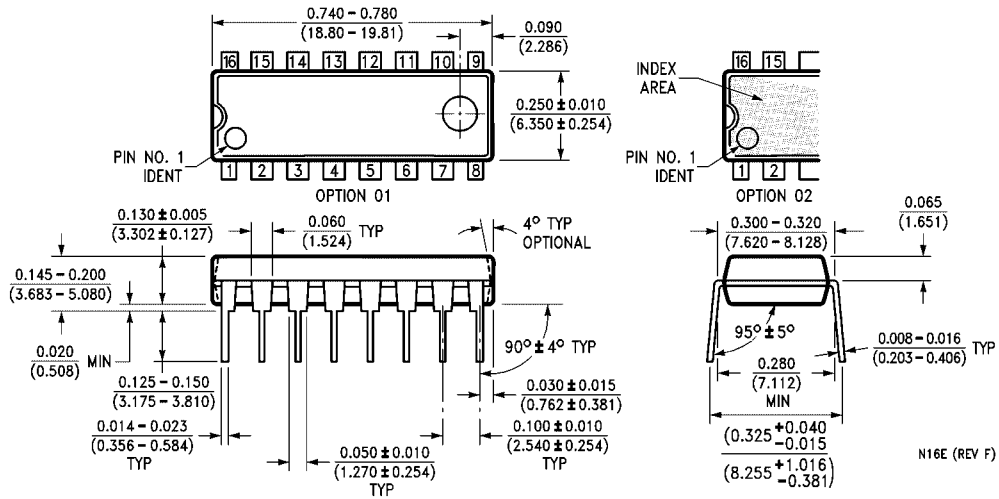
Note 5: AC Parameters are guaranteed by DC correlated testing.

Physical Dimensions inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E**

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