LCD MODULE SPECIFICATION
FOR CUSTOMER'S APPROVAL

APPROVED BY: (FOR CUSTOMER ONLY)

1. BASIC SPECIFICATION

1.1 Mechanical specifications

Items	Nominal Dimension	Unit
Dot Matrix	320 x 240	dots
Module Size (W x H x T)	154.6 x 114.8 x 9.85	mm.
Viewing Area (W x H)	121.4 x 92.62	mm.
Active Area (W x H)	115.17 x 86.37	mm.
Dot Size (W x H)	0.33 x 0.33	mm.
Dot Pitch (W x H)	0.36 x 0.36	mm.
Driving method	1/240	Duty
	1/16	Bias
Driving IC Package	TAB+PCB	

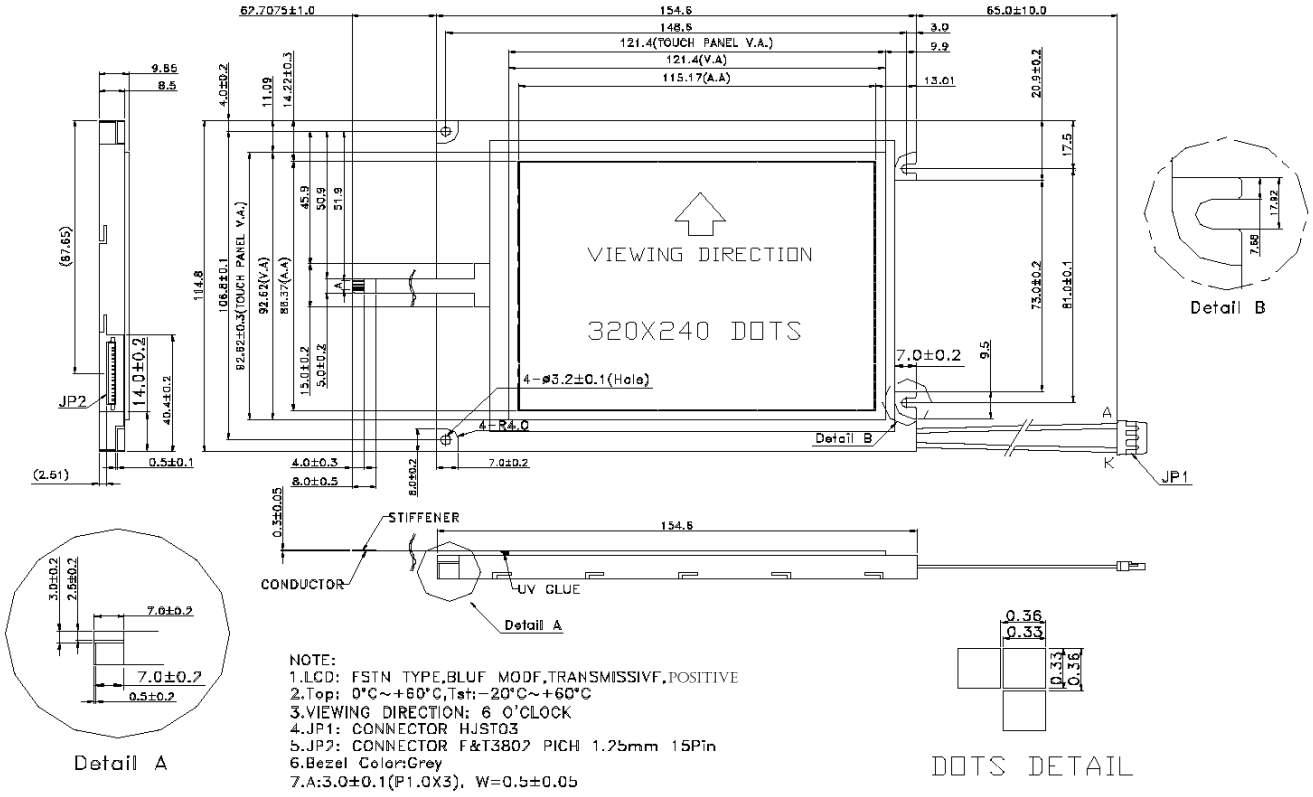
* Expose the driver IC under blaze (luminosity over than 1 cd) when using the LCM may cause IC operating failure.

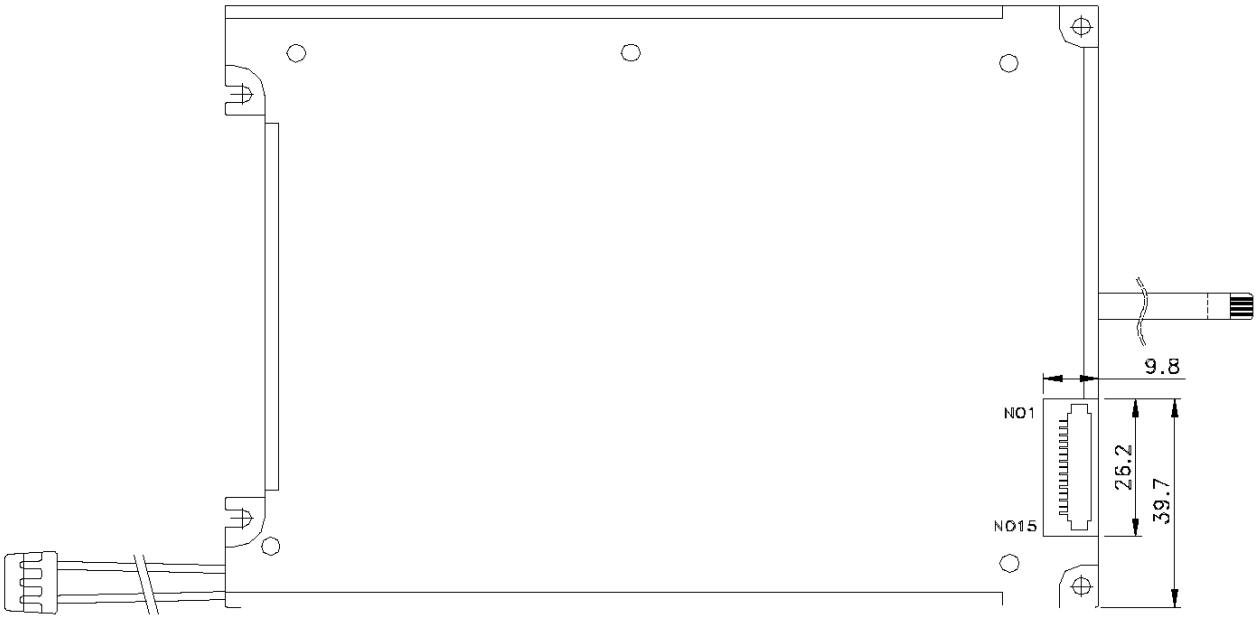
1.2 Display specification

Display	Descriptions	Note
LCD Type	FSTN	
LCD Mode	POSITIVE	
Polarizer Mode	Transmissive	
Polarizer UV-Cutting	With	
Polarizer Surface	Normal	
Background Color	Dark_Blue	
Backlight Type	CCFL	
Backlight Color	White	
Viewing Direction	6 O'clock Direction	

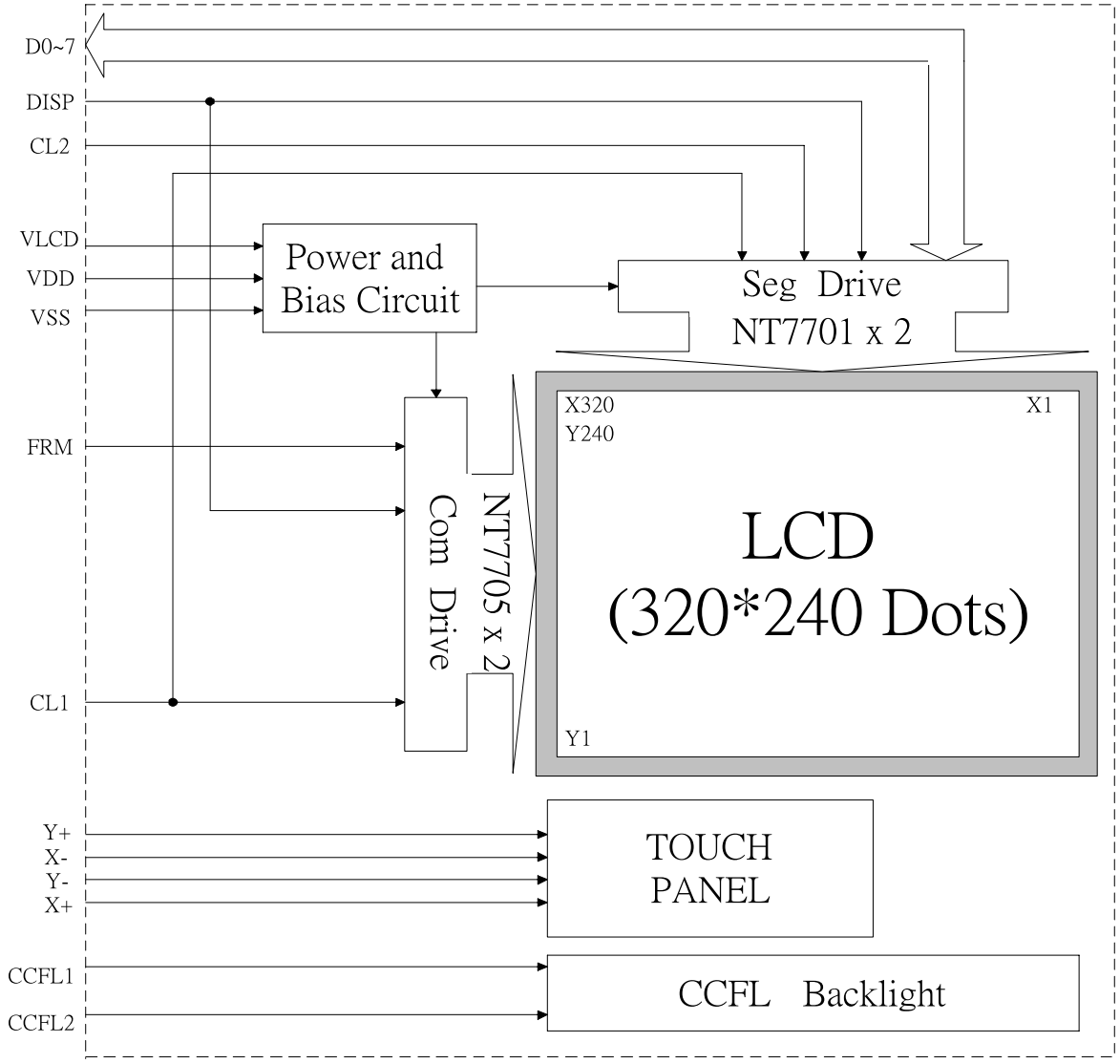
* Color tone is slightly changed by temperature and driving voltage.

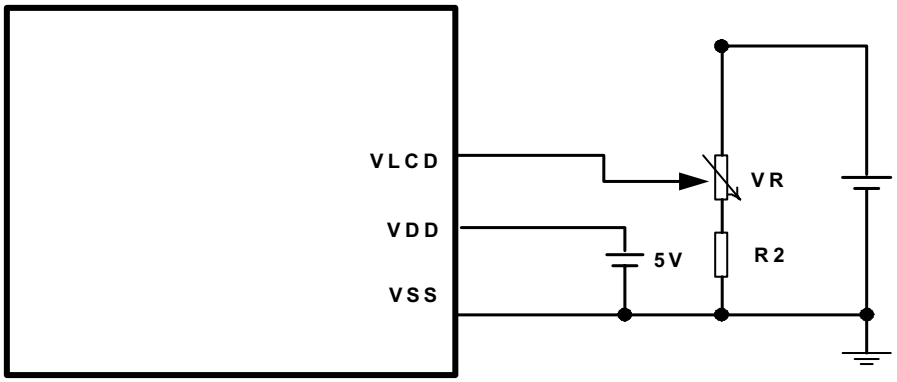
1.3 Outline dimension





1.4 Block diagram:





1.5 Interface pin :

Pin No.	Pin Symbol	I/O	Description
1	FRM	I	Start signal of frame.
2	CL1	I	Latch strobe signal.
3	CL2	I	Shift clock signal.
4	DISP	I	Display control signal.
5	VDD	-	Power supply voltage(+5.0V)
6	VSS	-	Ground (0V)
7	VLCD	-	Power supply for LCD driver.
8~15	D[7:0]	I/O	Bi-directional data bus.

Touch panel Interface Pin :

Pin No	Pin Symbol	I/O	Description
1	Y+	-	Touch screen.
2	X-	-	Touch screen.
3	Y-	-	Touch screen.
4	X+	-	Touch screen.

CCFL Backlight Interface Pin :

1	CCFL1	-	CCFL AC voltage Power supply input
2	NC		No connect
3	CCFL2	-	CCFL AC voltage Power supply input

2. ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit
Supply voltage for logics	VDD	-0.3	5.0	V
Supply voltage for driving LCD	VOUT,V5	-0.3	+30.0	V
Input voltage	VIN	-0.3	VDD+0.3	V
Operating temperature range	T_{OP}	0	+60	℃
Storage temperature range	T_{STR}	-20	+60	℃

2.2 DC Characteristics

Items	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply voltage (Logic)	VDD	2.5	5.0	5.5	V	
Supply voltage(LCD)	VOP	-		-	V	*NOTE1
Input high level voltage	V_{IH}	0.8xVDD	-	-	V	
Input low level voltage	V_{IL}	-	-	0.2xVDD	V	
Output high level voltage	V_{OH}	VDD-0.4	-	-	V	
Output low level voltage	V_{OL}	-	-	+0.4	V	
Power supply current (Vdd)	Idd			15	mA	*NOTE2

＊ The above spec. may be changed by Rev. No.

＊NOTE1 : Min. and Max. Voltage is specified as the voltage within the condition of operational Temperature range 0℃~60℃

Typ. Voltage is specified as module driving condition: Ta=25℃ , Vop at Optimum Contrast.

＊NOTE2 :

Measuring Condition :

Standard Value MAX.

Ta	=	25℃
VDD-VSS	=	5.0V
VDD-V0	=	Vop at optimum Contrast
Fose	=	14MHz
Bias	=	1/9 Bias
Duty	=	1/240 Duty
Display Patten	=	Checkered pattern

2.3 AC Characteristics

NT7701 (SEGMENT)

Segment Mode 1 (V_{SS} = V_S = 0V, V_{DD} = 4.5 - 5.5V, V_0 = 15 to 30, and T_A = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WCK}	71	-		ns	tr, tf ≤ 10ns, Note 1
Shift clock "H" pulse width	t_{WCKH}	23	-		ns	
Shift clock "L" pulse width	t_{WCKL}	23	-		ns	
Data setup time	t_{DS}	10	-		ns	
Data hole time	t_{DH}	20	-		ns	
Latch pulse "H" pulse width	t_{WLPH}	23	-		ns	
Shift clock rise to Latch pulse rise time	t_{LD}	0	-		ns	
Shift clock fall to Latch pulse fall time	t_{SL}	25	-		ns	
Latch pulse rise to Shift clock rise time	t_{LS}	25	-		ns	
Latch pulse fall to Shift clock rise time	t_{LH}	25	-		ns	
Input signal rise time	t_r		-	50	ns	Note 2
Input signal fall time	t_f		-	50	ns	Note 2
Enable setup time	t_S	21	-		ns	
$\overline{\text{DISPOFF}}$ Removal time	t_{SD}	100	-		ns	
$\overline{\text{DISPOFF}}$ enable pulse width	t_{WDL}	1.2	-		µs	
Output delay time (1)	t_D		-	40	ns	CL = 15pF
Output delay time (2)	t_{pd1}, t_{pd2}		-	1.2	µs	CL = 15pF
Output delay time (3)	t_{pd3}		-	1.2	µs	CL = 15pF

Note

1. Take the cascade connection into consideration.
2. (T_{ck} - t_{WCKH} - t_{wckl})/2 is the maximum in the case of high speed operation.

NT7705 (COMMON)

Common Mode (V_{SS} = V_S = 0V, V_{DD} = 2.5 - 5.5V, V_0 = 15 to 40V and T_A = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WLP}	250	-	-	ns	tr, tf ≤ 20ns
Shift clock "H" pulse width	t_{WLPH}	15	-	-	ns	V_{DD} = +5.0V ± 10%
		30	-	-	ns	V_{DD} = +2.5 - +4.5V
Data setup time	t_{SU}	30	-	-	ns	
Data hole time	t_H	50	-	-	ns	
Input signal rise time	t_r		-	50	ns	
Input signal fall time	t_f		-	50	ns	
$\overline{\text{DISPOFF}}$ Removal time	t_{SD}	100	-	-	ns	
$\overline{\text{DISPOFF}}$ enable pulse width	t_{WDL}	1.2	-	-	µs	
Output delay time (1)	t_{DL}	-	-	200	ns	C_L = 15pF
Output delay time (2)	t_{pd1}, t_{pd2}	-	-	1.2	µs	C_L = 15pF
Output delay time (3)	t_{pd3}	-	-	1.2	µs	C_L = 15pF

3. OPTICAL CHARACTERISTICS

3.1 Characteristics

Driving condition

Item	Duty	Bias	Note
Value	1/240	1/16	1

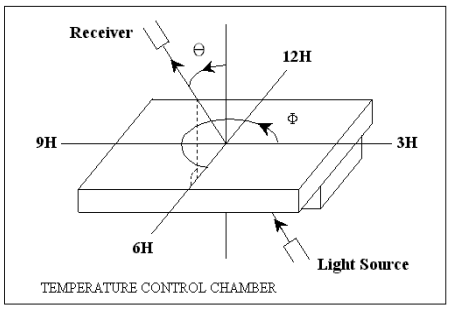
Electrical and Optical Characteristics

No.	Item		symbol / temp.		Min.	Typ.	Max.	Unit	Note
1	LCD Driving Vop		0 ℃		-	26.01	-	V	1
			25 ℃		-	25.85	-		
			60 ℃		-	24.85	-		
2	Response Time		Tr	25 ℃	-	420	840	ms	2
			Tf	25 ℃	-	140	280		
3	Viewing Angle	Front-Rear	ϴ1	Φ = 270°	-10	-	30	degree	3
		Left-Right	ϴ2		-30	-	30		
4	Contrast Ratio		Cr	25 ℃	-	3	-	-	4

3.2 Definition of optical characteristics

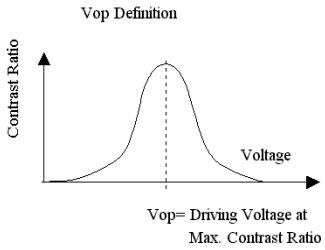
Measurement condition :

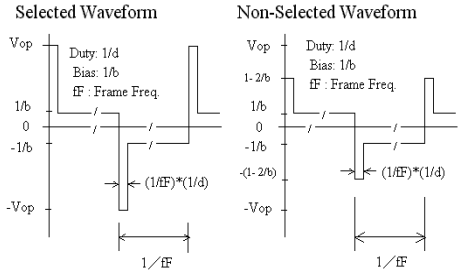
Transmissive and Transflective type



PHOTAL LCD-5000

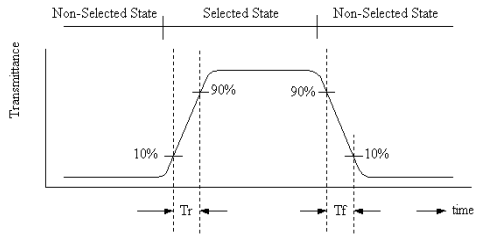
[Note 1] Definition of LCD Driving Vop and Waveform :





[Note 2] Definition of Response Time

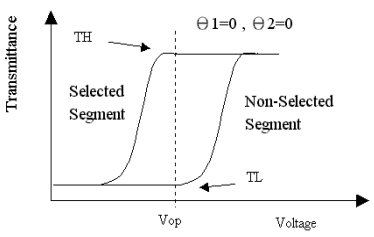
for Negative type :



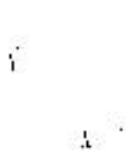
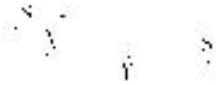
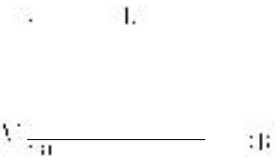
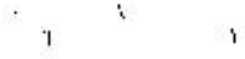
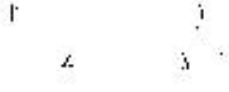
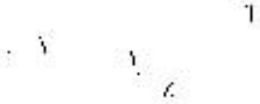
[Note 3] Definition of Viewing Angle :

[Note 4] Definition of Contrast Ratio :

for Negative type



$$\text{Contrast Ratio} = \frac{TH}{TL}$$

NO.	CLASS	ITEM	JUDGEMENT
8.4.4	MINOR	CRACK	 Y > S REJ.
8.4.5	MINOR	CRACK	 or Y > S REJ.
8.4.6	MAJOR	GLASS SCRATCH	 Y > (1/2) T REJ.
8.4.7	MAJOR	SCRIBE DEFECT	 a> L/3 , A>1.5mm. REJ. B : ACCORDING TO DIMENSION
8.4.8	MINOR	CRACK (ON THE TERMINAL AREA)	 Φ= (x+y)/2 > 2.5 mm REJ.
8.4.9	MINOR	CRACK (ON THE TERMINAL SURFACE)	 Y > (1/3) T REJ.
8.4.10	MINOR	CRACK	 Y > T REJ.