Fema Part Number

GM25664C-31-O3CW	
Description	3.1" Passive Matrix White Color OLED Display
	256x64 Characters
	Extended Operating Temperature -40 to 85 °C
	Wide Viewing Angle

1. Basic Specifications

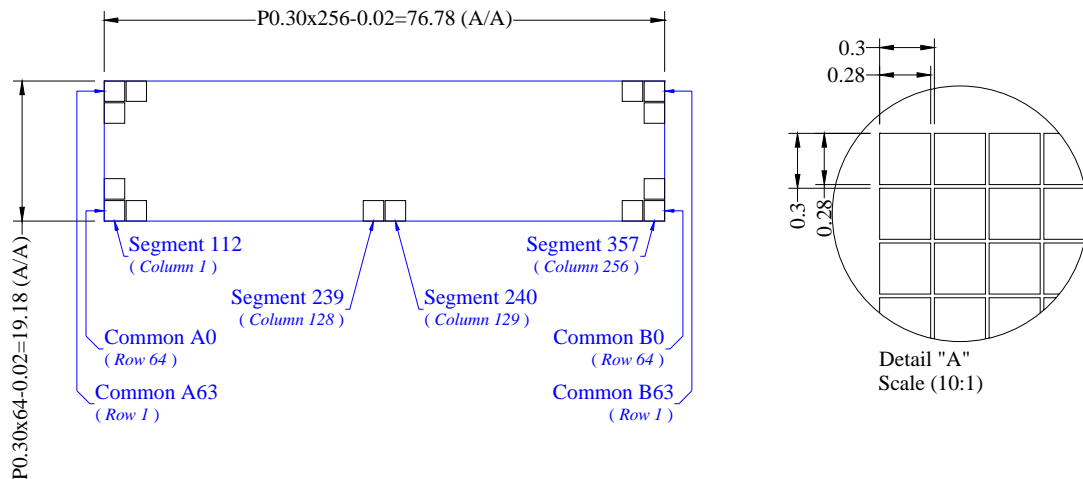## 1.1 Display Specifications

1) Display Mode: Passive Matrix
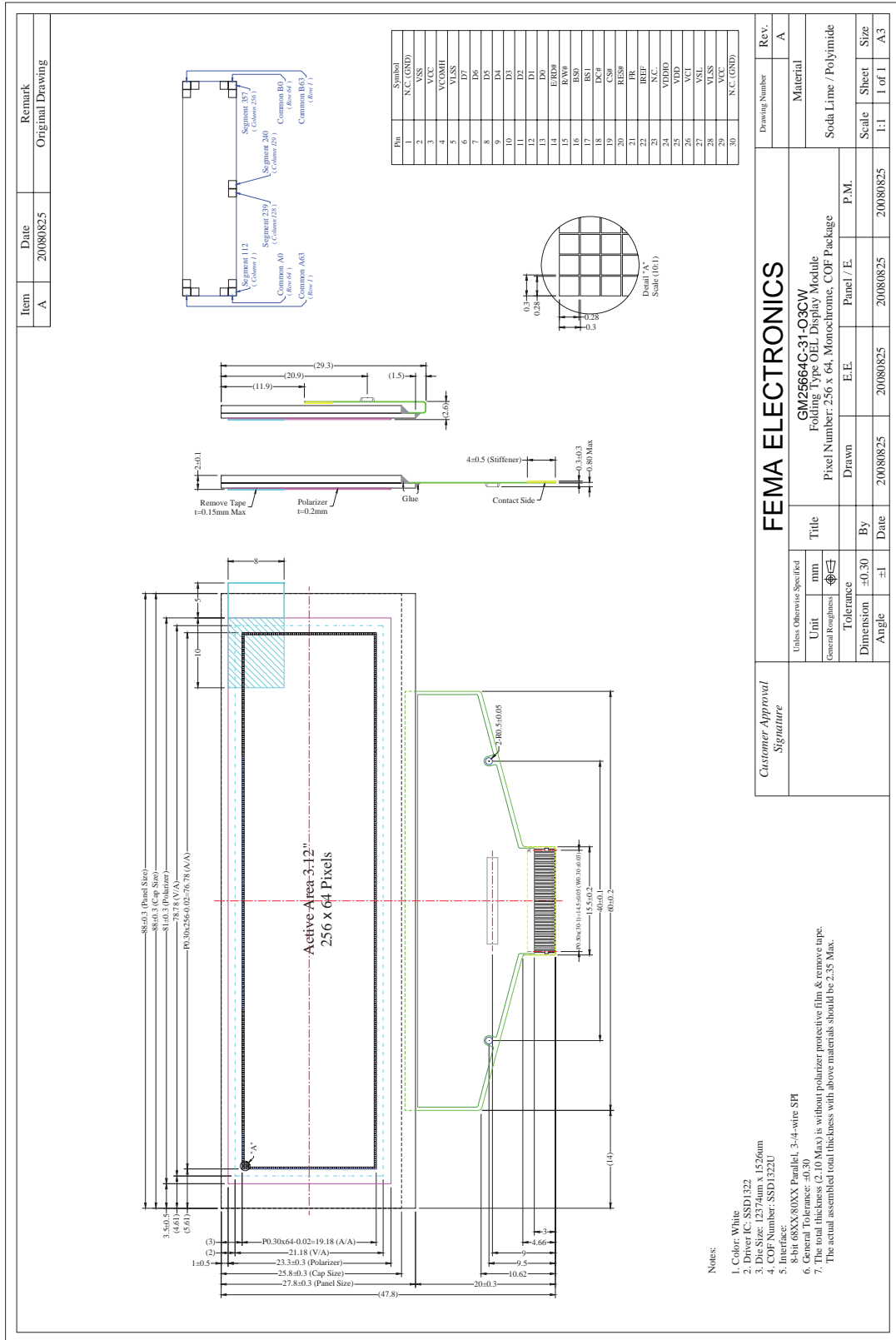2) Display Color: Monochrome (White)
3) Drive Duty: 1/64 Duty

1.2 Mechanical Specifications

1) Outline Drawing: According to the annexed outline drawing
2) Number of Pixels: 256×64
3) Panel Size: $88.00 \times 27.80 \times 2.00$ (mm)
4) Active Area: 76.78×19.18 (mm)
5) Pixel Pitch: 0.30×0.30 (mm)
6) Pixel Size: 0.28×0.28 (mm)
7) Weight: 9.95 (g)

1.3 Active Area & Pixel Construction

P0.30x256-0.02=76.78 (A/A)

P0.30x64-0.02=19.18 (A/A)

Segment 112
(Column 1)

Segment 357
(Column 256)

Segment 239
(Column 128)

Segment 240
(Column 129)

Common A0
(Row 64)

Common B0
(Row 64)

Common A63
(Row 1)

Common B63
(Row 1)

0.3
0.28

0.3
0.28

Detail "A"
Scale (10:1)

1.4 Mechanical Drawing

*Suggested mating connector: Hirose FH12A-30S-0.5SH(55)

FEMA ELECTRONICS

Title: Folding Type OEL Display Module
GM25664C-31-O3CW
Pixel Number: 256 x 64, Monochrome, COF Package

Material: Soda Lime / Polyimide

Drawing Number: Rev. A

Scale 1:1 | Sheet 1 of 1 | Size A3

	Drawn	E.E.	Panel / E	P.M.
By				
Date	20080825	20080825	20080825	20080825

Customer Approval Signature

Unless Otherwise Specified

Unit	mm	
General Roughness		
Tolerance	Dimension	±0.30
	Angle	±1

Notes:
1. Color: White
2. Driver IC: SSD1322
3. Die Size: 12374um x 1526um
4. COF Number: SSD1322U
5. Interface:
   8-bit 68XX/80XX Parallel, 3-/4-wire SPI
6. General Tolerance: ±0.30
7. The total thickness (2.10 Max) is without polarizer protective film & remove tape.
   The actual assembled total thickness should be 2.35 Max.

Item	Date	Remark
A	20080825	Original Drawing

Pin	Symbol
1	N.C.(GND)
2	VSS
3	VCC
4	VCOMH
5	VLSS
6	D7
7	D6
8	D5
9	D4
10	D3
11	D2
12	D1
13	D0
14	E/RD#
15	R/W#
16	BS0
17	BS1
18	DC#
19	CS#
20	RES#
21	FR
22	IREF
23	N.C.
24	VDDIO
25	VDD
26	VCI
27	VSL
28	VLSS
29	VCC
30	N.C.(GND)

Active Area 3.12"
256 x 64 Pixels

1.5 Pin Definition

| Pin Number	Symbol	Type	Function
Power Supply			
26	VCI	P	*Power Supply for Operation* This is a voltage supply pin. It must be connected to external source & always be equal to or higher than VDD & VDDIO.
25	VDD	P	*Power Supply for Core Logic Circuit* This is a voltage supply pin. It can be supplied externally (within the range of 2.4~2.6V) or regulated internally from VCI. A capacitor should be connected between this pin & VSS under all circumstances.
24	VDDIO	P	*Power Supply for I/O Pin* This pin is a power supply pin of I/O buffer. It should be connected to VDD or external source. All I/O signal should have VIH reference to VDDIO. When I/O signal pins (BS0~BS1, D0~D7, control signals…) pull high, they should be connected to VDDIO.
2	VSS	P	*Ground of Logic Circuit* This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.
3, 29	VCC	P	*Power Supply for OEL Panel* These are the most positive voltage supply pin of the chip. They must be connected to external source.
5, 28	VLSS	P	*Ground of Analog Circuit* These are the analog ground pins. They should be connected to VSS externally.
Driver			
22	IREF	I	*Current Reference for Brightness Adjustment* This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than 10uA.
4	VCOMH	P	*Voltage Output High Level for COM Signal* This pin is the input pin for the voltage output high level for COM signals. A tantalum capacitor should be connected between this pin and VSS.
27	VSL	P	*Voltage Output Low Level for SEG Signal* This is segment voltage reference pin. When external VSL is not used, this pin should be left open. When external VSL is used, this pin should connect with resistor and diode to ground.
Testing Pads			
21	FR	O	*Frame Frequency Triggering Signal* This pin will send out a signal that could be used to identify the driver status. Nothing should be connected to this pin. It should be left open individually.

1.5 Pin Definition (Continued)

Pin Number	Symbol	I/O	Function
Interface			
16 17	BS0 BS1	I	*Communicating Protocol Select* These pins are MCU interface selection input. See the following table: |	BS0	BS1
---	---	---
3-wire SPI	1	0
4-wire SPI	0	0
8-bit 68XX Parallel	1	1
8-bit 80XX Parallel	0	1	
20	RES#	I	*Power Reset for Controller and Driver* This pin is reset signal input. When the pin is low, initialization of the chip is executed.
19	CS#	I	*Chip Select* This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.
18	D/C#	I	*Data/Command Control* This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
14	E/RD#	I	*Read/Write Enable or Read* This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial mode is selected, this pin must be connected to VSS.
15	R/W#	I	*Read/Write Select or Write* This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial mode is selected, this pin must be connected to VSS.
6~13	D7~D0	I/O	*Host Data Input/Output Bus* These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. Unused pins must be connected to VSS except for D2 in serial mode.

1.5 Pin Definition (Continued)

Pin Number	Symbol	I/O	Function
Reserve			
23	N.C.	-	*Reserved Pin* The N.C. pin between function pins are reserved for compatible and flexible design.
1, 30	N.C. (GND)	-	*Reserved Pin (Supporting Pin)* The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.

1.6 Block Diagram

Active Area 3.12"
256 x 64 Pixels

SSD1322
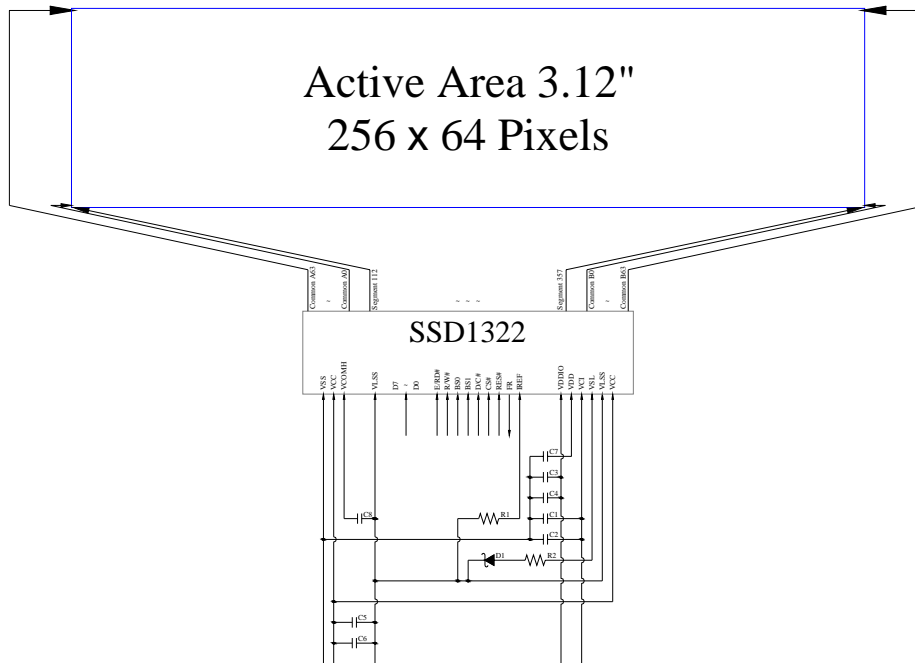
MCU Interface Selection: BS0 and BS1
Pins connected to MCU interface: D7~D0, E/RD#, R/W#, D/C#, CS#, and RES#

C1, C3, C5: 0.1μF
C2, C4:   4.7μF
C6:   10μF
C7:   1μF
C8:   4.7uF / 25V Tantalum Capacitor
R1:   680kΩ, R1 = (Voltage at IREF – VSS) / IREF
R2:   50Ω, 1/4W
D1:   ≤1.4V, 0.5W

2. *Absolute Maximum Ratings*

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Operation	V_{CI}	-0.3	4	V	1, 2
Supply Voltage for Logic	V_{DD}	-0.5	2.75	V	1, 2
Supply Voltage for I/O Pins	V_{DDIO}	-0.5	V_{CI}	V	1, 2
Supply Voltage for Display	V_{CC}	-0.5	16	V	1, 2
Operating Current for V_{CC}	I_{CC}	-	55	mA	1, 2
Operating Temperature	T_{OP}	-30	85	°C	-
Storage Temperature	T_{STG}	-40	90	°C	-

Note 1: All the above voltages are on the basis of "VSS = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

3. *Optics & Electrical Characteristics*

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	With Polarizer (Note 3)	60	80	-	cd/m^2
C.I.E. (White)	(x) (y)	Without Polarizer	0.28 0.29	0.32 0.33	0.36 0.37	
Dark Room Contrast	CR		-	>2000:1	-	
View Angle			>160	-	-	degree

* Optical measurement taken at V_{CI} = 2.8V, V_{CC} = 12V.
Software configuration follows Section 4.4 Initialization.

3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Operation	V_{CI}		2.4	2.8	3.5	V
Supply Voltage for Logic	V_{DD}		2.4	2.5	2.6	V
Supply Voltage for I/O Pins	V_{DDIO}		1.65	1.8	V_{CI}	V
Supply Voltage for Display	V_{CC}	Note 3	11.5	12	12.5	V
High Level Input	V_{IH}		$0.8 \times V_{DDIO}$	-	V_{DDIO}	V
Low Level Input	V_{IL}		0	-	$0.2 \times V_{DDIO}$	V
High Level Output	V_{OH}	I_{out} = 100μA, 3.3MHz	$0.9 \times V_{DDIO}$	-	V_{DDIO}	V
Low Level Output	V_{OL}	I_{out} = 100μA, 3.3MHz	0	-	$0.1 \times V_{DDIO}$	V
Operating Current for V_{CI}	I_{CI}		-	1.8	2.25	mA
Operating Current for V_{CC}	I_{CC}	Note 4	-	26.3	32.9	mA
		Note 5	-	41.1	51.4	mA
Sleep Mode Current for V_{CI}	$I_{CI, SLEEP}$		-	1	5	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	1	5	μA

Note 3: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.
Note 4: V_{CI} = 2.8V, V_{CC} = 12V, 50% Display Area Turn on.
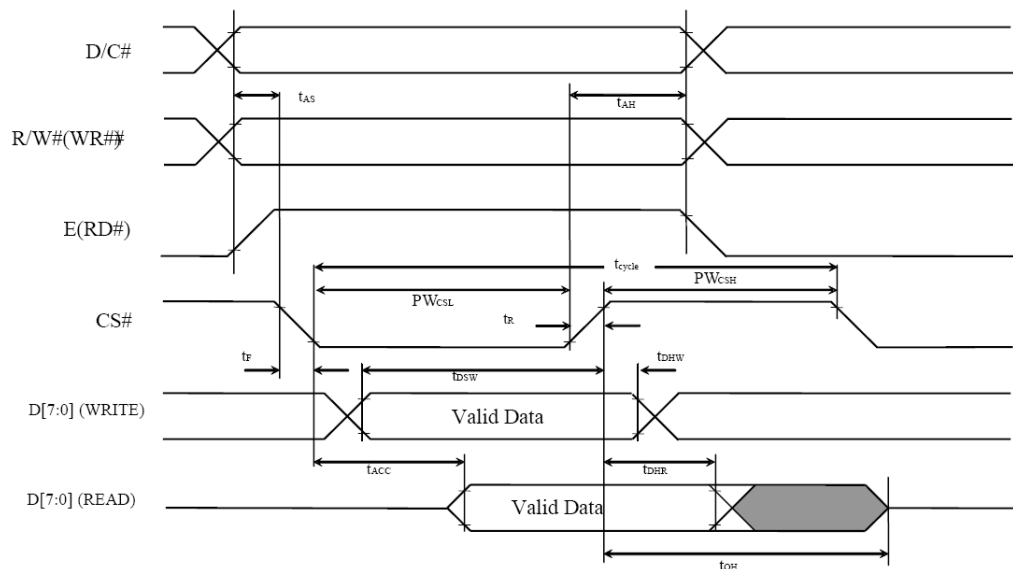Note 5: V_{CI} = 2.8V, V_{CC} = 12V, 100% Display Area Turn on.

* Software configuration follows Section 4.4 Initialization.

3.3 AC Characteristics

3.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse Width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* ($V_{DD} - V_{SS}$ = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)

3.3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	150	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_{R}	Rise Time	-	15	ns
t_{F}	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)
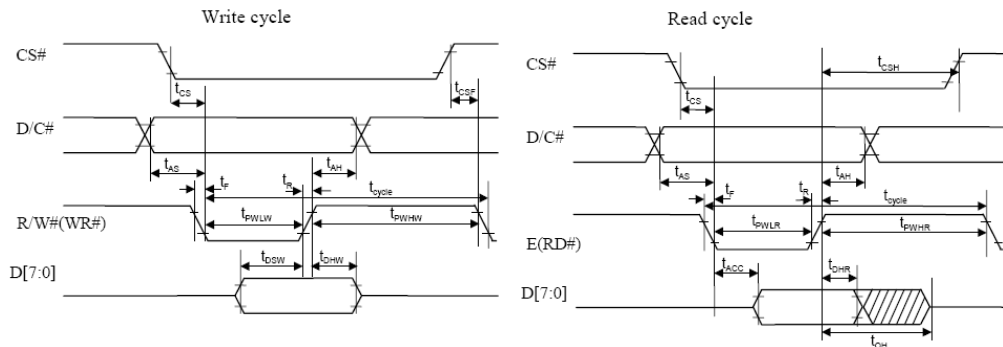
3.3.3 Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)

3.3.4 Serial Interface Timing Characteristics: (3-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* $(V_{DD} - V_{SS} = 2.4V$ to $2.6V$, $V_{DDIO} = 1.6V$, $V_{CI} = 2.8V$, $T_a = 25°C)$

4. Functional Specification

4.1. Commands

Refer to the Technical Manual for the SSD1322

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.
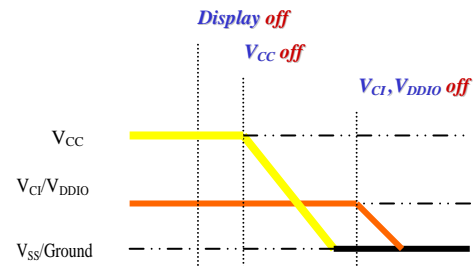
4.2.1 Power up Sequence:

1. Power up V_{CI} & V_{DDIO}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms
   (When V_{CC} is stable)
7. Send Display on command
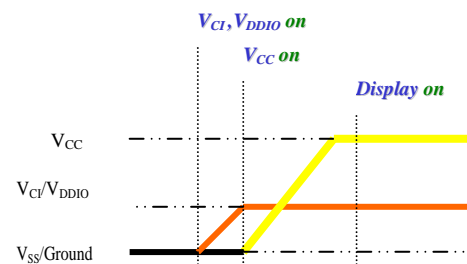
4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
   (When V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{CI} & V_{DDIO}

4.3 Reset Circuit

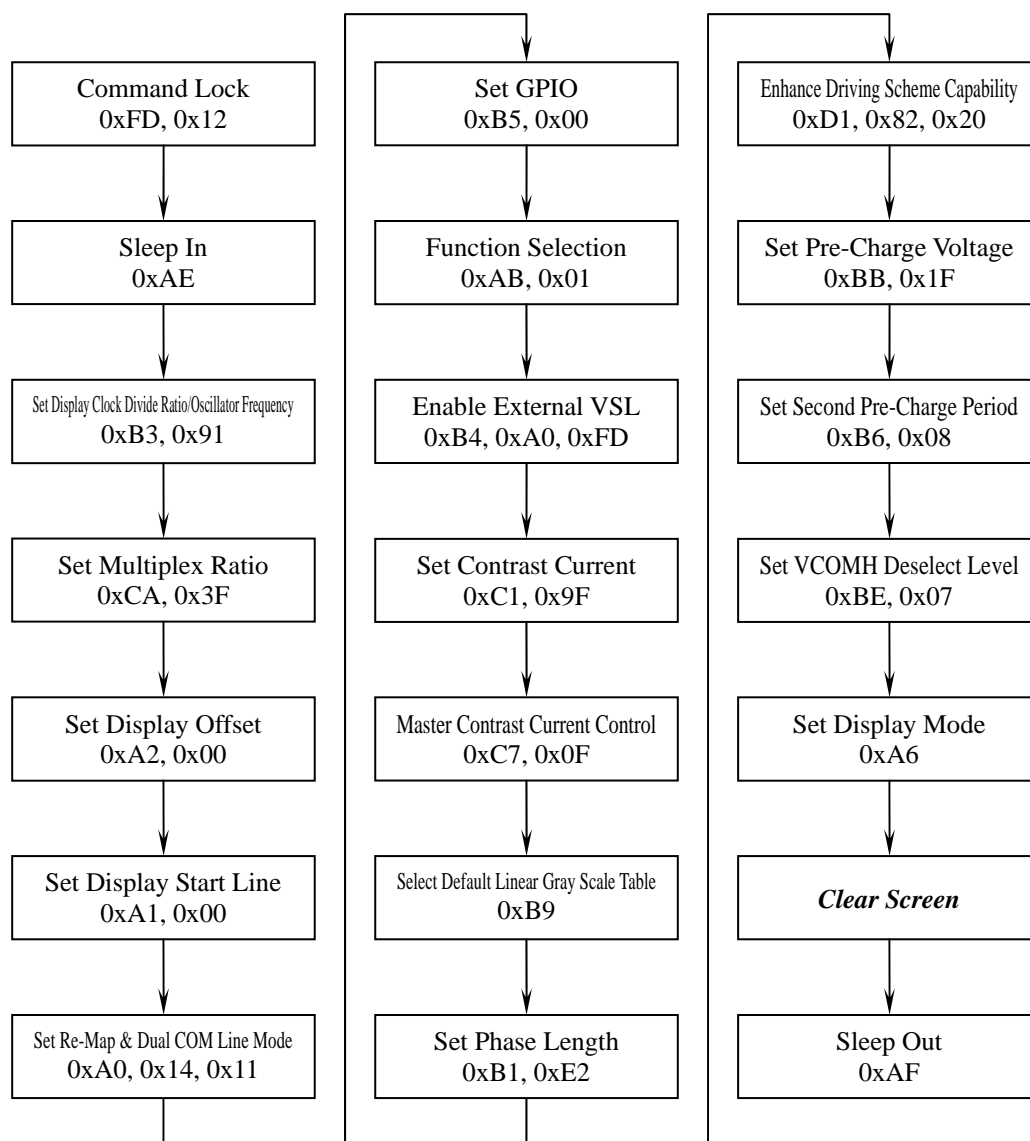When RES# input is low, the chip is initialized with the following status:
1. Display is OFF
2. 480×128 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Display start line is set at display RAM address 0
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Contrast control registers is set at 7Fh

4.4 Actual Application Example

Command usage and explanation of an actual example

<Initialization>

Command Lock 0xFD, 0x12	Set GPIO 0xB5, 0x00	Enhance Driving Scheme Capability 0xD1, 0x82, 0x20
Sleep In 0xAE	Function Selection 0xAB, 0x01	Set Pre-Charge Voltage 0xBB, 0x1F
Set Display Clock Divide Ratio/Oscillator Frequency 0xB3, 0x91	Enable External VSL 0xB4, 0xA0, 0xFD	Set Second Pre-Charge Period 0xB6, 0x08
Set Multiplex Ratio 0xCA, 0x3F	Set Contrast Current 0xC1, 0x9F	Set VCOMH Deselect Level 0xBE, 0x07
Set Display Offset 0xA2, 0x00	Master Contrast Current Control 0xC7, 0x0F	Set Display Mode 0xA6
Set Display Start Line 0xA1, 0x00	Select Default Linear Gray Scale Table 0xB9	*Clear Screen*
Set Re-Map & Dual COM Line Mode 0xA0, 0x14, 0x11	Set Phase Length 0xB1, 0xE2	Sleep Out 0xAF

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

5. *Reliability*

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	85°C, 500 hrs	The operational functions work.
Low Temperature Operation	-30°C, 500 hrs	
High Temperature Storage	90°C, 500 hrs	
Low Temperature Storage	-40°C, 500 hrs	
High Temperature/Humidity Storage	60°C, 90% RH, 500 hrs	
Thermal Shock	-40°C ⇔ 85°C, 100 cycles 30 mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

5.2 Lifetime

End of lifetime is specified as 50% of initial brightness reached.

Parameter	Min	Max	Unit	Condition	Notes
Operating Life Time	10,000	-	hr	80 cd/m^2, 50% Checkerboard	6
Storage Life Time	20,000	-	hr	Ta = 25°C, 50% RH	-

Note 6: The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

5.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.