3-Level NPC Inverter Module

NXH450N65L4Q2F2S1G

The NXH450N65L4Q2F2S1G is a power module containing a I−type neutral point clamped three−level inverter. The integrated field stop trench IGBTs and FRDs provide lower conduction losses and switching losses, enabling designers to achieve high efficiency and superior reliability.

Features

- Neutral Point Clamped Three−Level Inverter Module
- 650 V Field Stop 4 IGBTs
- Low Inductive Layout
- Solderable Pins
- Thermistor
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Solar Inverters
- Uninterruptable Power Supplies Systems

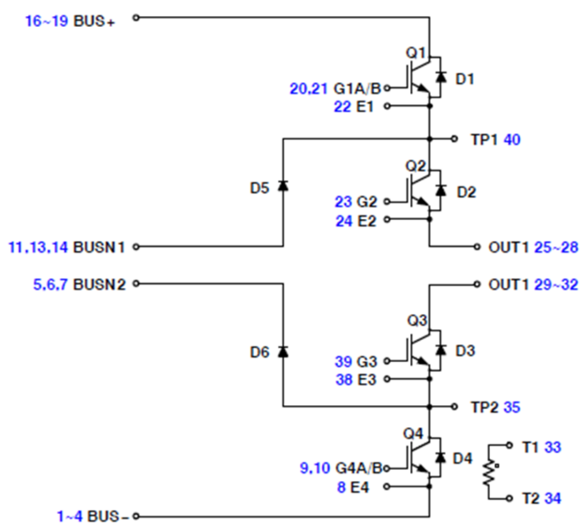

Figure 1. Schematic Diagram

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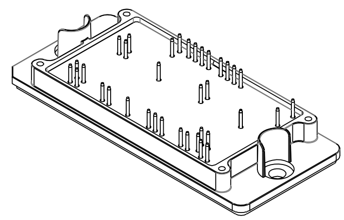
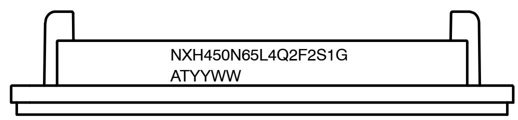


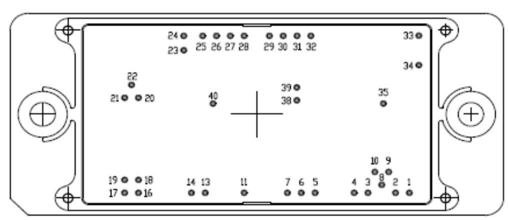
PIM40, 107.2x47
CASE 180BE

MARKING DIAGRAM



NXH450N65L4Q2F2S1G	= Specific Device Code
G	= Pb−Free Package
AT	= Assembly & Test Site Code
YYWW	= Year and Work Week Code

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 16 of this data sheet.

March, 2021 − Rev. 0

Publication Order Number:
NXH450N65L4Q2F2S1G/D

MAXIMUM RATINGS (Note 1)

Symbol	Rating	Value	Unit
OUTER IGBT (Q1−1, Q1−2, Q4−1, Q4−2)			
V_{CES}	Collector−Emitter Voltage	650	V
V_{GE}	Gate−Emitter Voltage Positive Transient Gate−Emitter Voltage (t_{pulse} = 5 s, D < 0.10)	±20 30	V
I_C	Continuous Collector Current @ T_c = 80°C (T_J = 175°C)	167	A
I_{Cpulse}	Pulsed Collector Current (T_J = 175°C)	501	A
P_{tot}	Maximum Power Dissipation (T_J = 175°C)	365	W
T_{JMAX}	Maximum Operating Junction Temperature	175	°C
INNER IGBT (Q2, Q3)			
V_{CES}	Collector−Emitter Voltage	650	V
V_{GE}	Gate−Emitter Voltage Positive Transient Gate−Emitter Voltage (t_{pulse} = 5 s, D < 0.10)	±20 30	V
I_C	Continuous Collector Current @ T_c = 80°C (T_J = 175°C)	280	A
I_{Cpulse}	Pulsed Collector Current (T_J = 175°C)	840	A
P_{tot}	Maximum Power Dissipation (T_J = 175°C)	633	W
T_{JMAX}	Maximum Operating Junction Temperature	175	°C
NEUTRAL POINT DIODE (D5, D6)			
V_{RRM}	Peak Repetitive Reverse Voltage	650	V
I_F	Continuous Forward Current @ T_c = 80°C (T_J = 175°C)	211	A
I_{FRM}	Repetitive Peak Forward Current (T_J = 175°C)	633	A
P_{tot}	Maximum Power Dissipation (T_J = 175°C)	500	W
T_{JMAX}	Maximum Operating Junction Temperature	175	°C
INVERSE DIODES (D1, D2, D3, D4)			
V_{RRM}	Peak Repetitive Reverse Voltage	650	V
I_F	Continuous Forward Current @ T_c = 80°C (T_J = 175°C)	93	A
I_{FRM}	Repetitive Peak Forward Current (t_p = 1 ms)	279	A
P_{tot}	Maximum Power Dissipation (T_J = 175°C)	231	W
T_{JMAX}	Maximum Operating Junction Temperature	175	°C
THERMAL PROPERTIES			
T_{stg}	Storage Temperature Range	−40 to 150	°C
INSULATION PROPERTIES			
V_{is}	Isolation Test Voltage, t = 1 min, 50/60 Hz	2500	V_{rms}
	Creepage Distance	12.7	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.

RECOMMENDED OPERATING RANGES

Symbol	Rating	Min	Max	Unit
T_J	Module Operating Junction Temperature	−40	T_{JMAX}	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OUTER IGBT (Q1−1, Q1−2, Q4−1, Q4−2)						
I_{CES}	Collector−Emitter Cutoff Current	V_{GE} = 0 V, V_{CE} = 650 V	–	–	300	μA
$V_{CE(sat)}$	Collector−Emitter Saturation Voltage	V_{GE} = 15 V, I_C = 225 A, T_J = 25°C	–	1.49	2.2	V
		V_{GE} = 15 V, I_C = 225 A, T_J = 175°C	–	1.68	–	
$V_{GE(TH)}$	Gate−Emitter Threshold Voltage	V_{GE} = V_{CE}, I_C = 2.75 mA	3.1	4.1	5.2	V
I_{GES}	Gate Leakage Current	V_{GE} = 20 V, V_{CE} = 0 V	–	–	600	nA
$t_{d(on)}$	Turn−On Delay Time	T_J = 25°C V_{CE} = 400 V, I_C = 200 A V_{GE} = −5 V to +15 V, R_G = 10 Ω	–	162	–	ns
t_r	Rise Time		–	49	–	
$t_{d(off)}$	Turn−off Delay Time		–	642	–	
t_f	Fall Time		–	52	–	
E_{on}	Turn−On Switching Loss per Pulse		–	4.4	–	mJ
E_{off}	Turn Off Switching Loss per Pulse		–	4.8	–	
$t_{d(on)}$	Turn−On Delay Time	T_J = 125°C V_{CE} = 400 V, I_C = 200 A V_{GE} = −5 V to +15 V, R_G = 10 Ω	–	150	–	ns
t_r	Rise Time		–	57	–	
$t_{d(off)}$	Turn−off Delay Time		–	692	–	
t_f	Fall Time		–	70	–	
E_{on}	Turn−on Switching Loss per Pulse		–	6.2	–	mJ
E_{off}	Turn Off Switching Loss per Pulse		–	5.1	–	
C_{ies}	Input Capacitance	V_{CE} = 20 V, V_{GE} = 0 V, f = 10 kHz	–	14630	–	pF
C_{oes}	Output Capacitance		–	230	–	
C_{res}	Reverse Transfer Capacitance		–	64	–	
Q_g	Total Gate Charge	V_{CE} = 480 V, I_C = 225 A, V_{GE} = ±15 V	–	452	–	nC
R_{thJH}	Thermal Resistance − Chip−to−Heatsink	Thermal grease, Thickness = 2 Mil ±2%, A = 2.8 W/mK	–	0.45	–	°C/W
R_{thJC}	Thermal Resistance − Chip−to−Case		–	0.26	–	°C/W
NEUTRAL POINT DIODE (D5, D6)						
V_F	Diode Forward Voltage	I_F = 250 A, T_J = 25°C	–	2.45	3.1	V
		I_F = 250 A, T_J = 175°C	–	1.87	–	
t_{rr}	Reverse Recovery Time	T_J = 25°C V_{CE} = 400 V, I_C = 200 A V_{GE} = −5 V to +15 V, R_G = 10 Ω	–	37	–	ns
Q_{rr}	Reverse Recovery Charge		–	1.6	–	°C
I_{RRM}	Peak Reverse Recovery Current		–	69	–	A
di/dt	Peak Rate of Fall of Recovery Current		–	3225	–	A/μs
E_{rr}	Reverse Recovery Energy		–	0.31	–	mJ
t_{rr}	Reverse Recovery Time	T_J = 125°C V_{CE} = 400 V, I_C = 200 A V_{GE} = −5 V to +15 V, R_G = 10 Ω	–	71	–	ns
Q_{rr}	Reverse Recovery Charge		–	6	–	°C
I_{RRM}	Peak Reverse Recovery Current		–	138	–	A
di/dt	Peak Rate of Fall of Recovery Current		–	2987	–	A/μs
E_{rr}	Reverse Recovery Energy		–	1.28	–	mJ
R_{thJH}	Thermal Resistance − Chip−to−Heatsink	Thermal grease, Thickness = 2 Mil ±2%, A = 2.8 W/mK	–	0.32	–	°C/W
R_{thJC}	Thermal Resistance − Chip−to−Case		–	0.19	–	°C/W
INNER IGBT (Q2, Q3)						
I_{CES}	Collector−Emitter Cutoff Current	V_{GE} = 0 V, V_{CE} = 650 V	–	–	300	μA
$V_{CE(sat)}$	Collector−Emitter Saturation Voltage	V_{GE} = 15 V, I_C = 375 A, T_J = 25°C	–	1.49	2.2	V
		V_{GE} = 15 V, I_C = 375 A, T_J = 175°C	–	1.73	–	
$V_{GE(TH)}$	Gate−Emitter Threshold Voltage	V_{GE} = V_{CE}, I_C = 3.75 mA	3.1	4.1	5.2	V
I_{GES}	Gate Leakage Current	V_{GE} = 20 V, V_{CE} = 0 V	–	–	1000	nA

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
INNER IGBT (Q2, Q3)						
$t_{d(on)}$	Turn−On Delay Time	T_J = 25°C V_{CE} = 400 V, I_C = 200 A V_{GE} = −5 V to +15 V, R_G = 15 Ω	–	188	–	ns
t_r	Rise Time		–	67	–	
$t_{d(off)}$	Turn−Off Delay Time		–	749	–	
t_f	Fall Time		–	48	–	
E_{on}	Turn−On Switching Loss per Pulse		–	4.8	–	mJ
E_{off}	Turn Off Switching Loss per Pulse		–	6.5	–	
$t_{d(on)}$	Turn−On Delay Time	T_J = 125°C V_{CE} = 400 V, I_C = 200 A V_{GE} = −5 V to +15 V, R_G = 15 Ω	–	175	–	ns
t_r	Rise Time		–	76	–	
$t_{d(off)}$	Turn−Off Delay Time		–	814	–	
t_f	Fall Time		–	50	–	
E_{on}	Turn−On Switching Loss per Pulse		–	5.68	–	mJ
E_{off}	Turn Off Switching Loss per Pulse		–	6.59	–	
C_{ies}	Input Capacitance	V_{CE} = 20 V, V_{GE} = 0 V, f = 10 kHz	–	24383	–	pF
C_{oes}	Output Capacitance		–	383	–	
C_{res}	Reverse Transfer Capacitance		–	105	–	
Q_g	Total Gate Charge	V_{CE} = 480 V, I_C = 375 A, V_{GE} = ±15 V	–	753	–	nC
R_{thJH}	Thermal Resistance − Chip−to−Heatsink	Thermal grease, Thickness = 2 Mil ±2%, A = 2.8 W/mK	–	0.31	–	°C/W
R_{thJC}	Thermal Resistance − Chip−to−Case		–	0.15	–	°C/W
INVERSE DIODES (D1, D2, D3, D4)						
V_F	Diode Forward Voltage	I_F = 100 A, T_J = 25°C	–	2.25	3.1	V
		I_F = 100 A, T_J = 175°C	–	1.69	–	
t_{rr}	Reverse Recovery Time	T_J = 25°C V_{CE} = 400 V, I_C = 200 A V_{GE} = −5 V to +15 V, R_G = 15 Ω	–	24.4	–	ns
Q_{rr}	Reverse Recovery Charge		–	0.49	–	°C
I_{RRM}	Peak Reverse Recovery Current		–	32	–	A
di/dt	Peak Rate of Fall of Recovery Current		–	2365	–	A/μs
E_{rr}	Reverse Recovery Energy		–	0.096	–	mJ
t_{rr}	Reverse Recovery Time	T_J = 125°C V_{CE} = 400 V, I_C = 200 A V_{GE} = −5 V to +15 V, R_G = 15 Ω	–	104	–	ns
Q_{rr}	Reverse Recovery Charge		–	2.54	–	°C
I_{RRM}	Peak Reverse Recovery Current		–	58	–	A
di/dt	Peak Rate of Fall of Recovery Current		–	2116	–	A/μs
E_{rr}	Reverse Recovery Energy		–	0.608	–	mJ
R_{thJH}	Thermal Resistance − Chip−to−Heatsink	Thermal grease, Thickness = 2 Mil ±2%, A = 2.8 W/mK	–	0.57	–	°C/W
R_{thJC}	Thermal Resistance − Chip−to−Case		–	0.41	–	°C/W
THERMISTOR PROPERTIES						
R_{25}	Nominal Resistance	T = 25°C	–	22	–	kΩ
R_{100}	Nominal Resistance	T = 100°C	–	1486	–	Ω
R/R	Deviation of R25		−5	–	5	%
P_D	Power Dissipation		–	200	–	mW
	Power Dissipation Constant		–	2	–	mW/K
	B−value	B (25/50), tolerance ±3%	–	3950	–	K
	B−value	B (25/100), tolerance ±3%	–	3998	–	K

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS – IGBT Q1−1, Q1−2, Q4−1, Q4−2 AND DIODE D1, D4

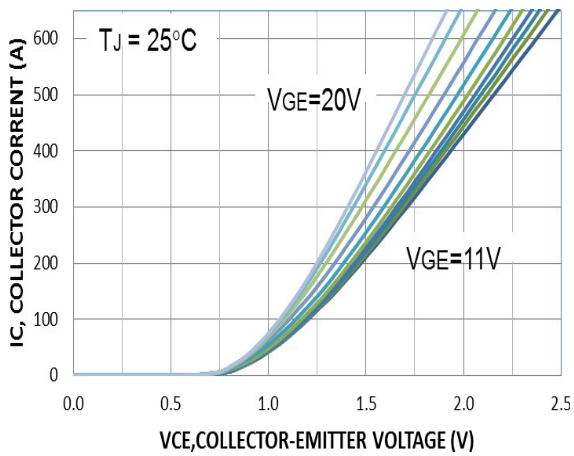


Figure 2. Typical Output Characteristics

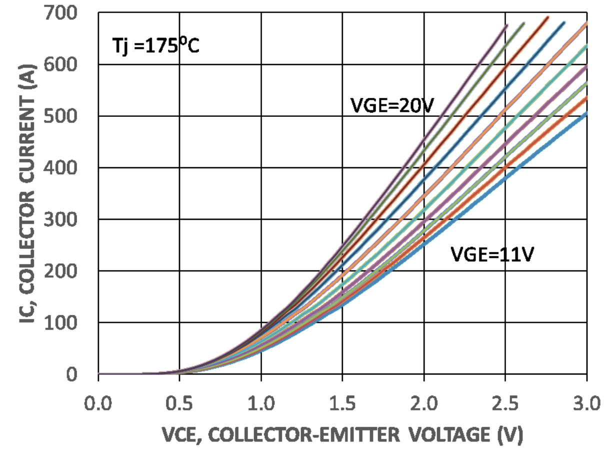


Figure 4. Typical Output Characteristics

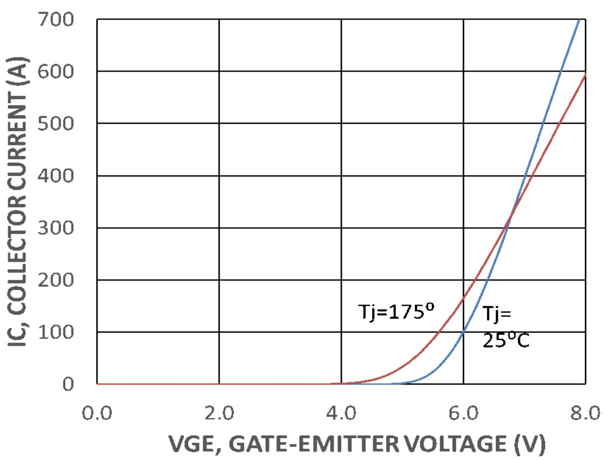


Figure 3. Typical Transfer Characteristics

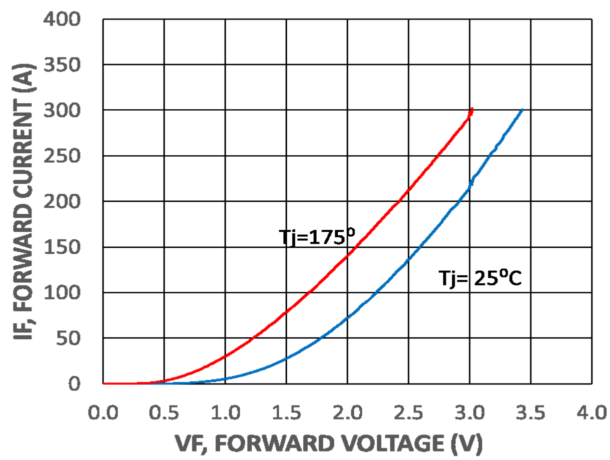


Figure 5. Typical Transfer Characteristics

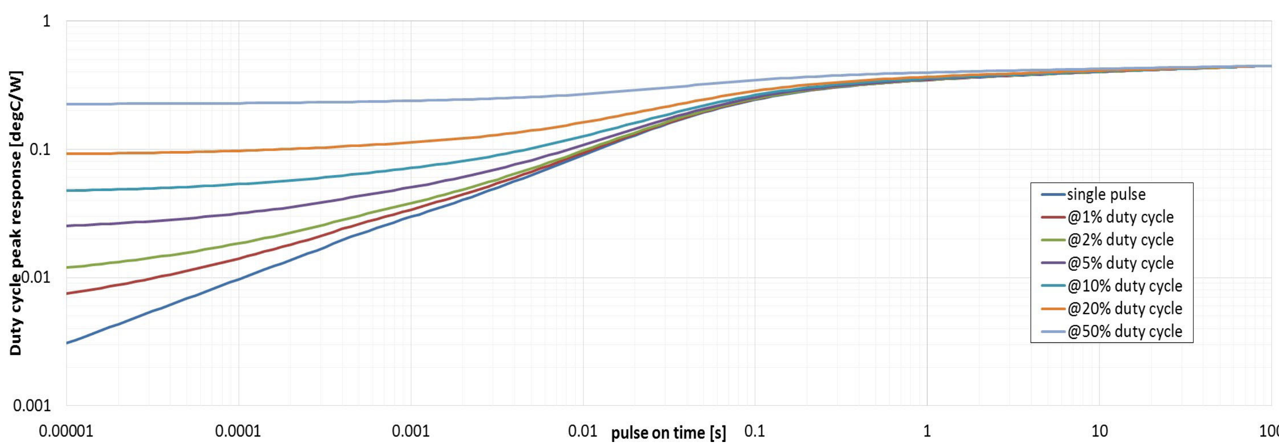


Figure 6. Transient Thermal Impedance (Q1−1, Q1−2, Q4−1, Q4−2)

TYPICAL CHARACTERISTICS – IGBT Q1−1, Q1−2, Q4−1, Q4−2 AND DIODE D1, D4 (continued)

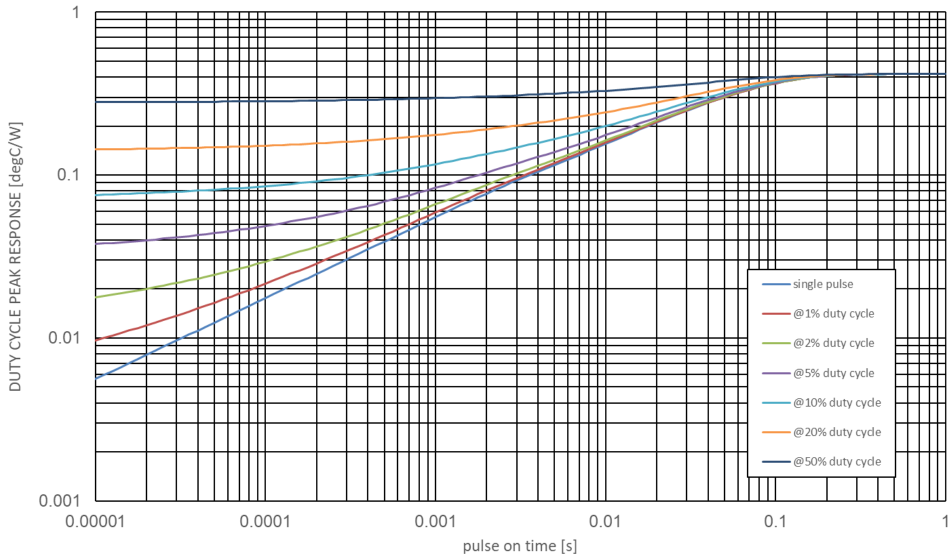


Figure 7. Transient Thermal Impedance (D1, D4)

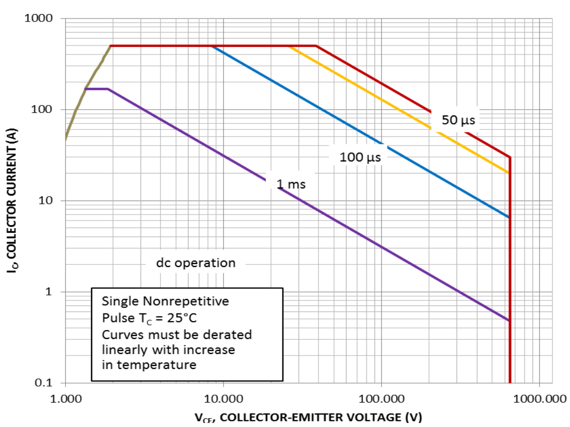


Figure 8. FBSOA (Q1−1, Q1−2, Q4−1, Q4−2)

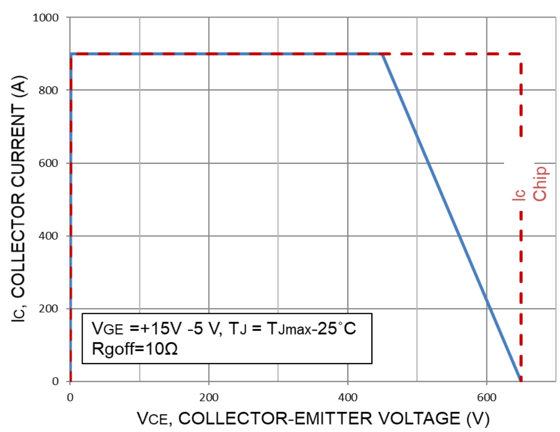


Figure 9. RBSOA (Q1, Q4)

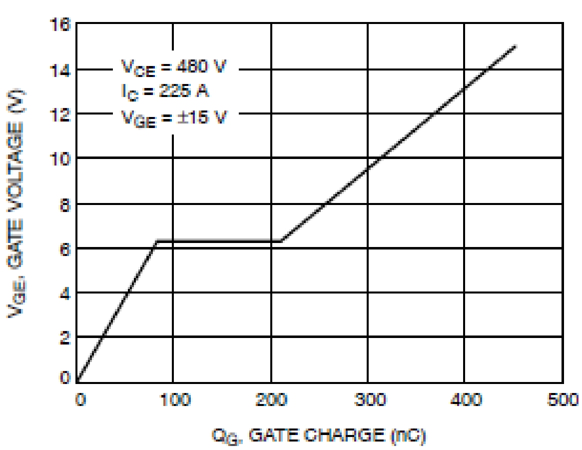


Figure 10. Gate Voltage vs. Gate Charge

TYPICAL CHARACTERISTICS – IGBT Q2, Q3 AND DIODE D2, D3

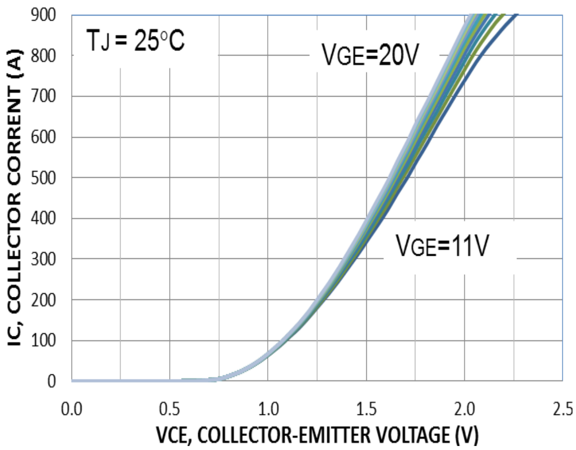


Figure 11. Typical Output Characteristics

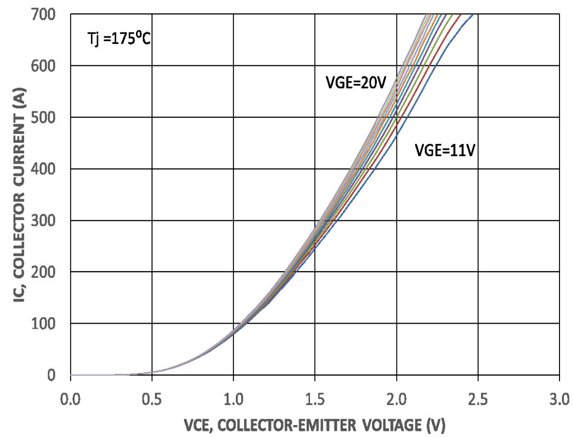


Figure 12. Typical Output Characteristics

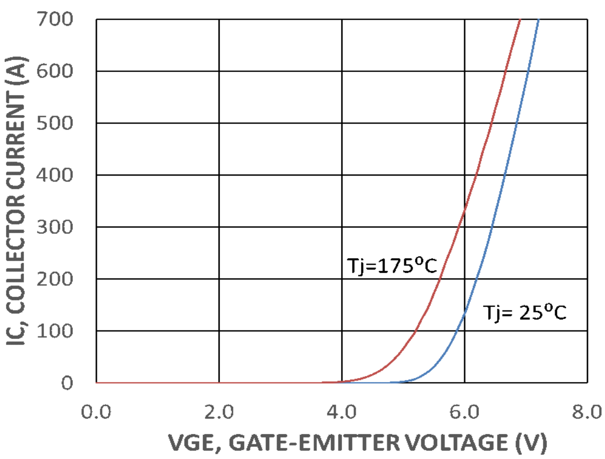


Figure 13. Typical Transfer Characteristics

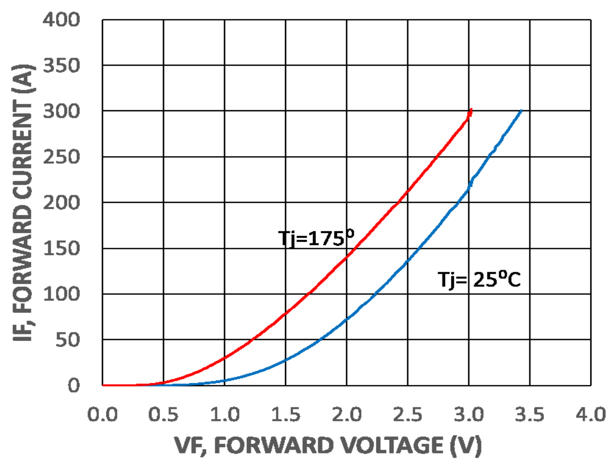


Figure 14. Typical Transfer Characteristics

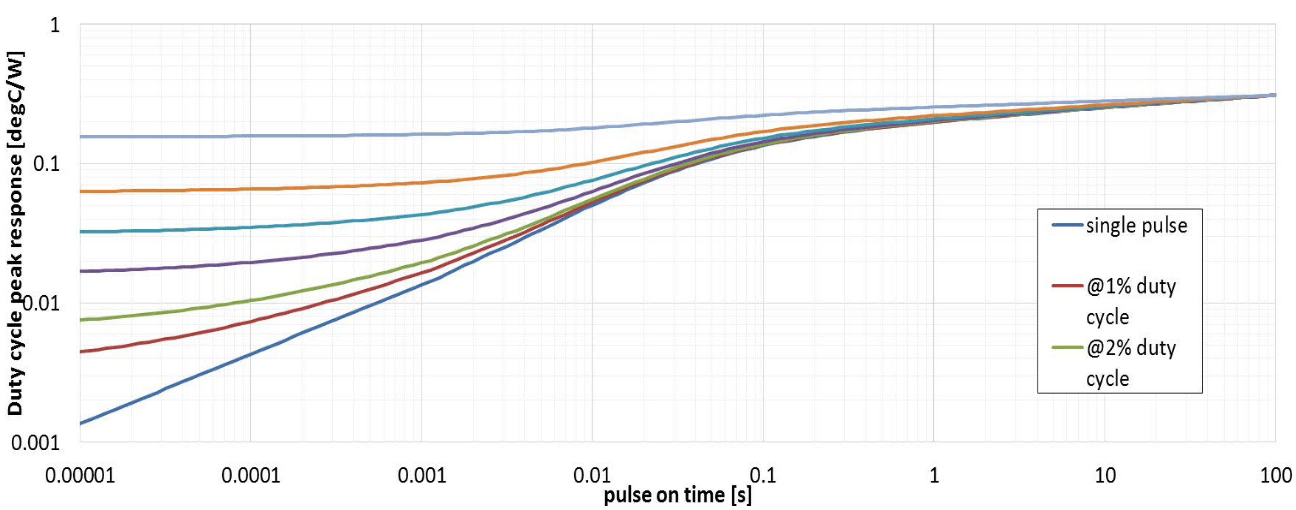


Figure 15. Transient Thermal Impedance (Q2, Q3)

TYPICAL CHARACTERISTICS – IGBT Q2, Q3 AND DIODE D2, D3 (continued)

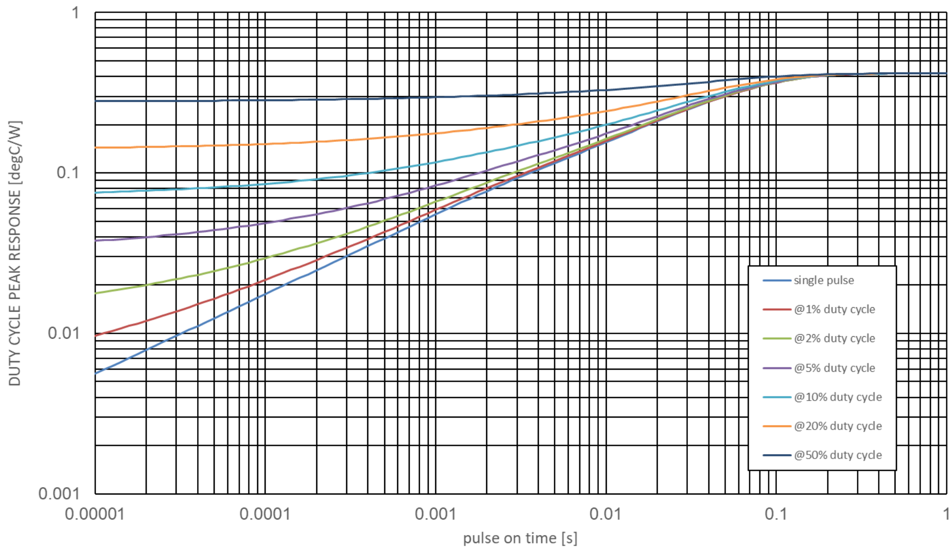


Figure 16. Transient Thermal Impedance (D2, D3)

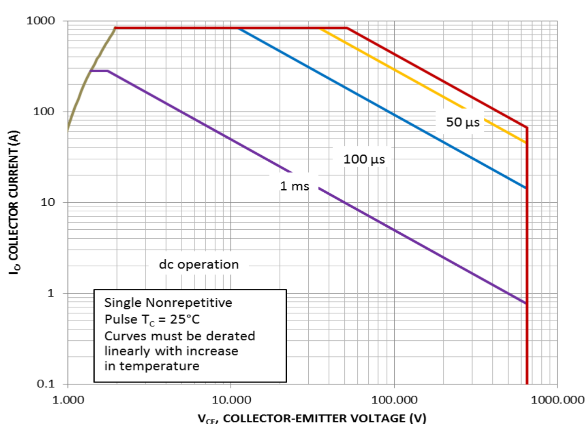


Figure 17. FBSOA (Q2, Q3)

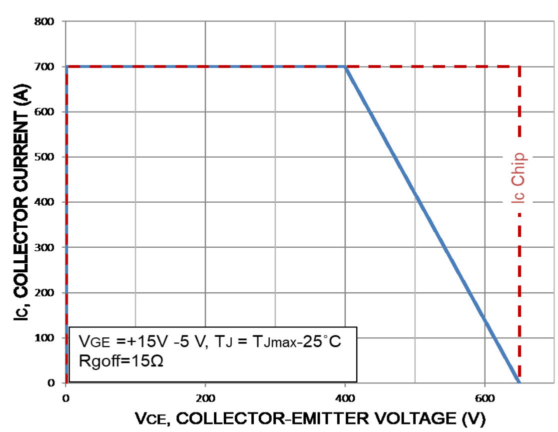


Figure 18. RBSOA (Q2, Q3)

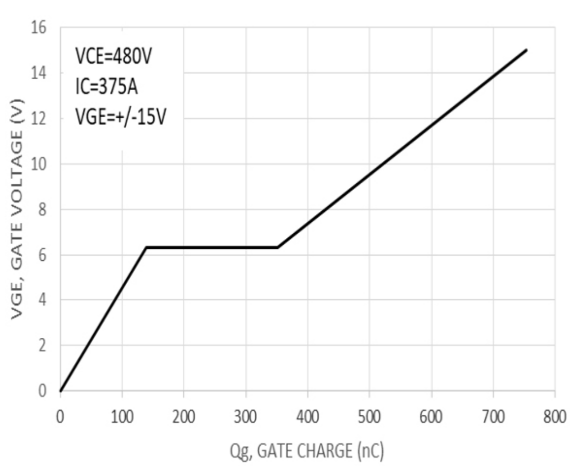


Figure 19. Gate Voltage vs. Gate Charge

TYPICAL CHARACTERISTICS – DIODE D5, D6

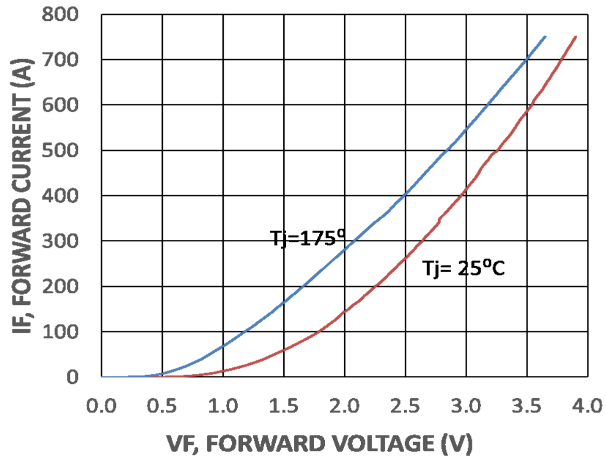


Figure 20. Diode Forward Characteristics

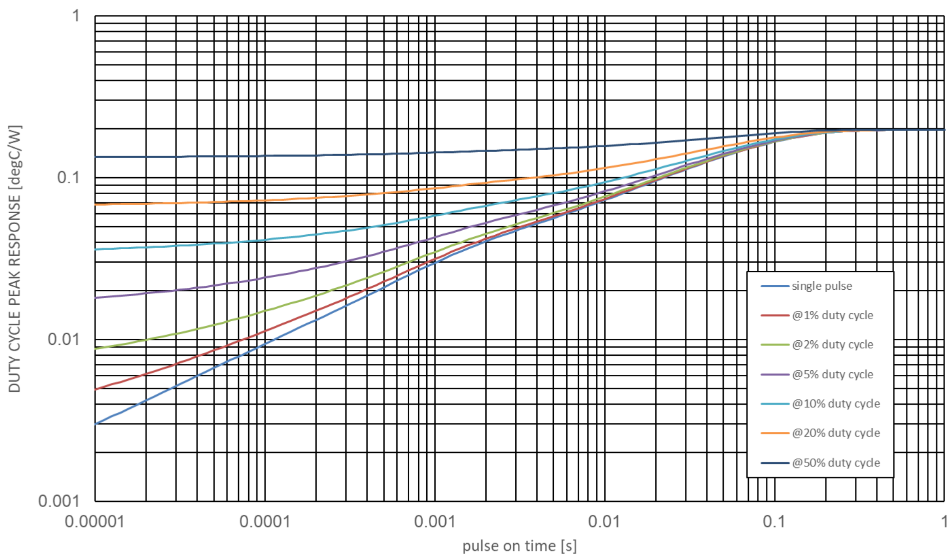


Figure 21. Transient Thermal Impedance (D5, D6)

TYPICAL CHARACTERISTICS – Q1/Q4 IGBT COMUNATES D5/D6 DIODE

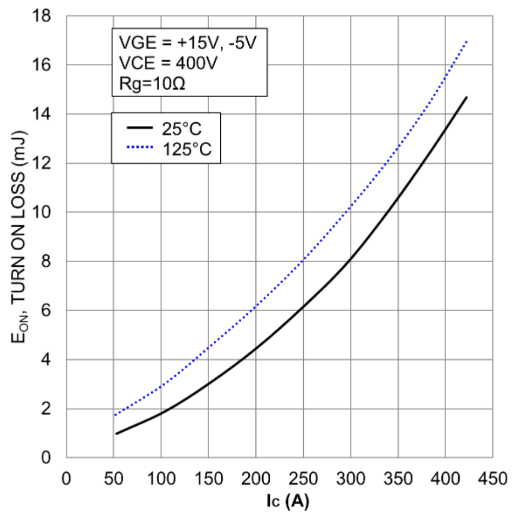


Figure 22. Typical Switching Loss Eon vs. IC

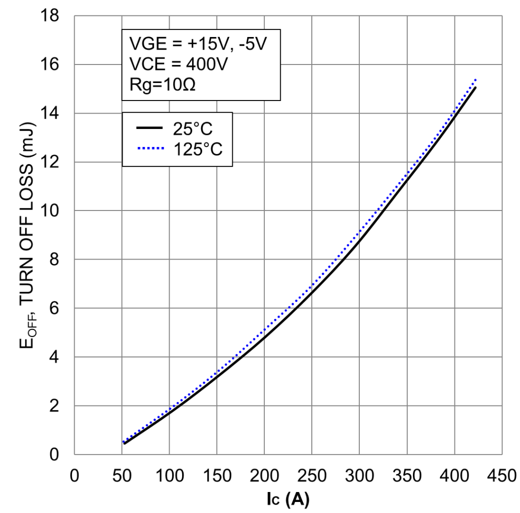


Figure 23. Typical Switching Loss Eoff vs. IC

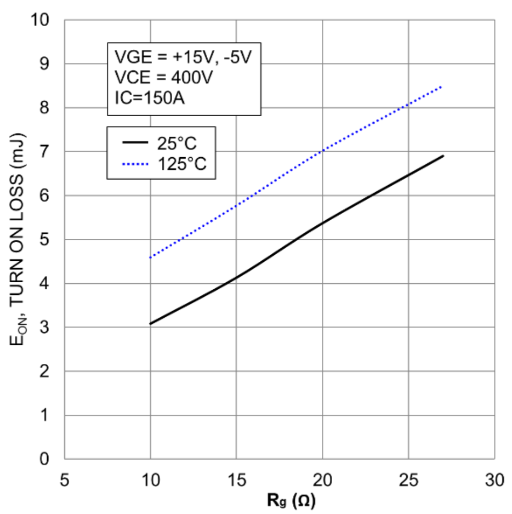


Figure 26. Typical Switching Loss Eon vs. R_G

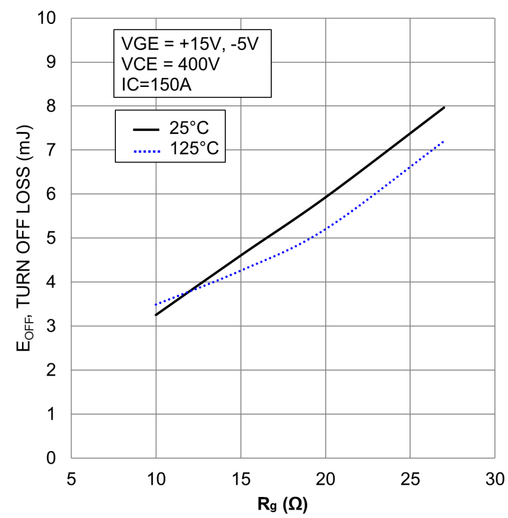


Figure 27. Typical Switching Loss Eoff vs. R_G

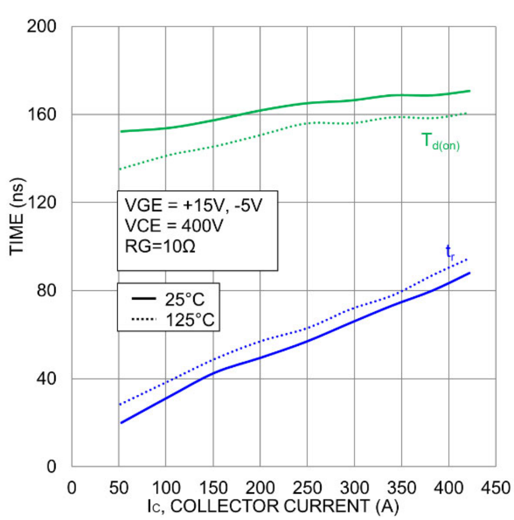


Figure 24. Typical Switching Time Tdon vs. IC

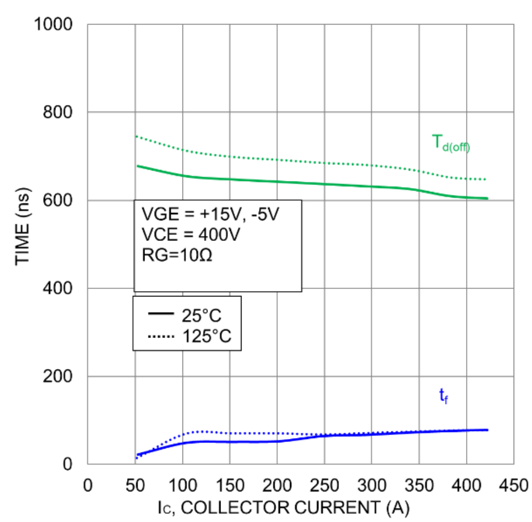


Figure 25. Typical Switching Time Tdoff vs. IC

TYPICAL CHARACTERISTICS – Q1/Q4 IGBT COMUNATES D5/D6 DIODE (continued)

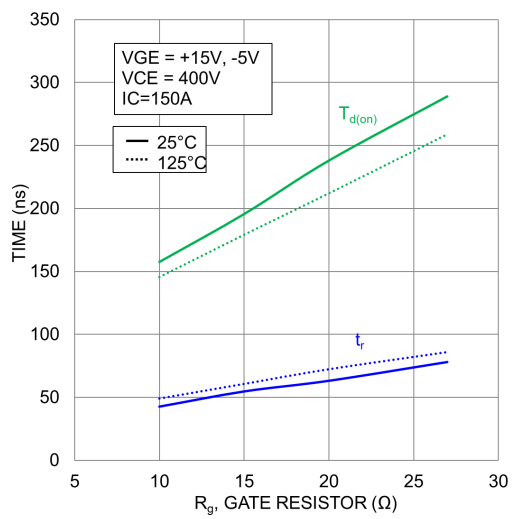


Figure 28. Typical Switching Time Tdon vs. R_G

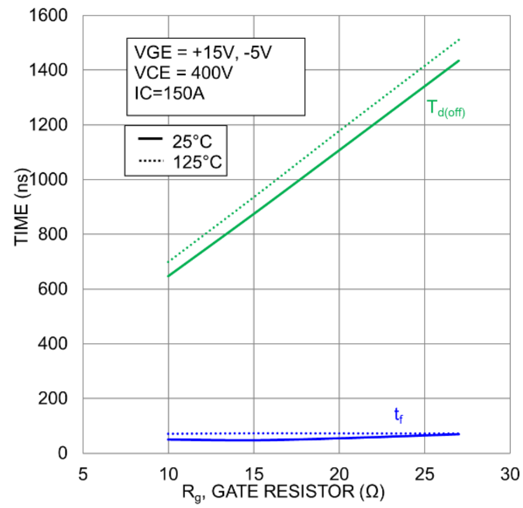


Figure 29. Typical Switching Time Tdoff vs. R_G

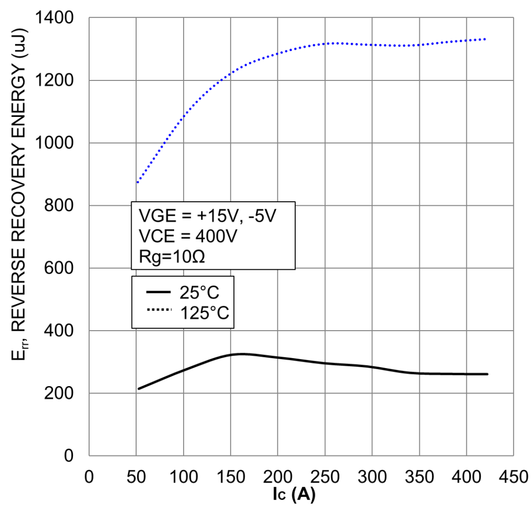


Figure 30. Typical Reverse Recovery Energy vs. IC

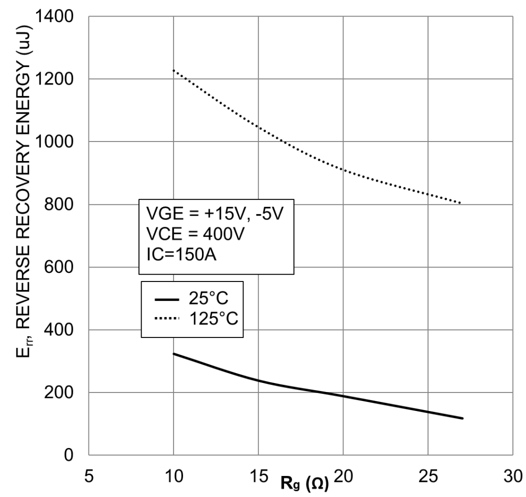


Figure 31. Typical Reverse Recovery Energy vs. R_G

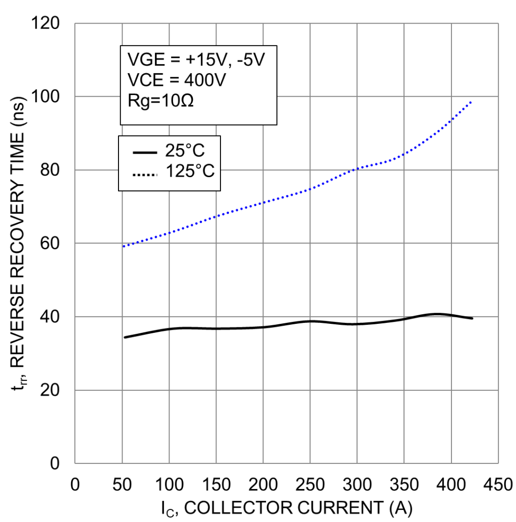


Figure 32. Typical Reverse Recovery Time vs. IC

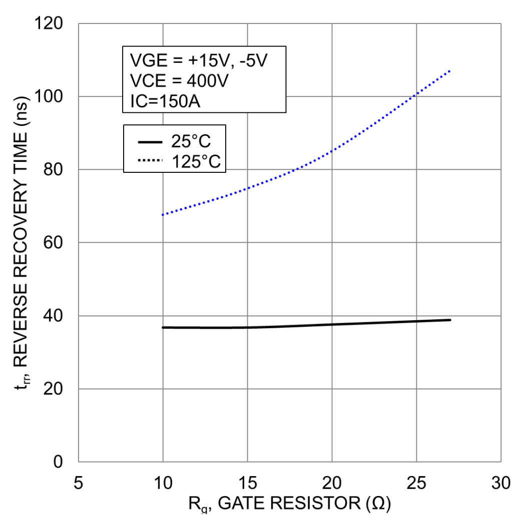


Figure 33. Typical Reverse Recovery Time vs. R_G

TYPICAL CHARACTERISTICS – Q1/Q4 IGBT COMUNATES D5/D6 DIODE (continued)

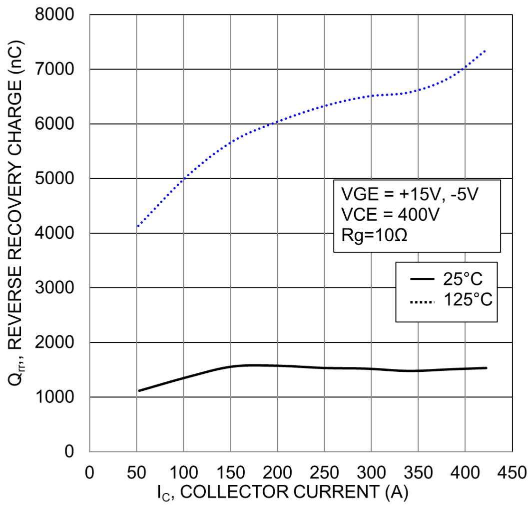


Figure 34. Typical Reverse Recovery Charge vs. IC

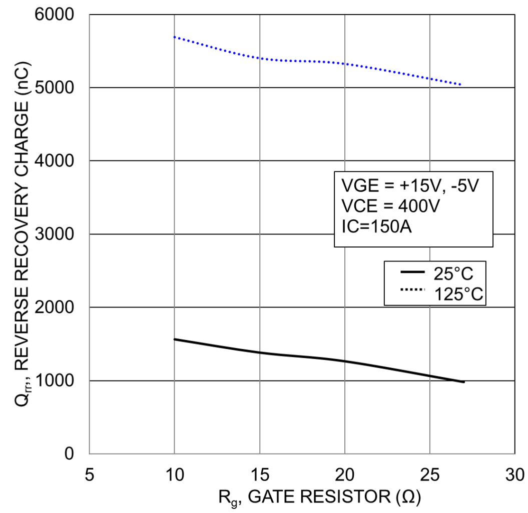


Figure 35. Typical Reverse Recovery Charge vs. R_G

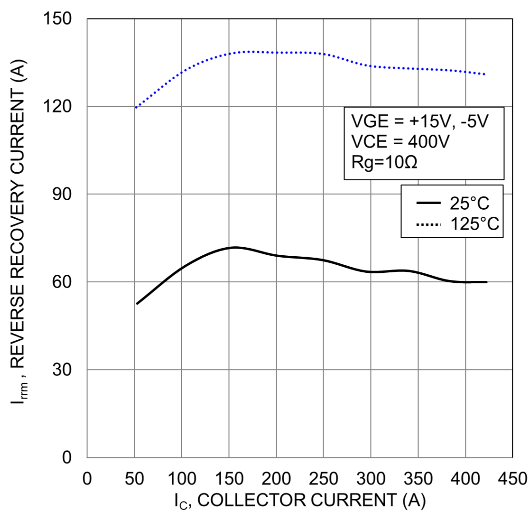


Figure 36. Typical Reverse Recovery Current vs. IC

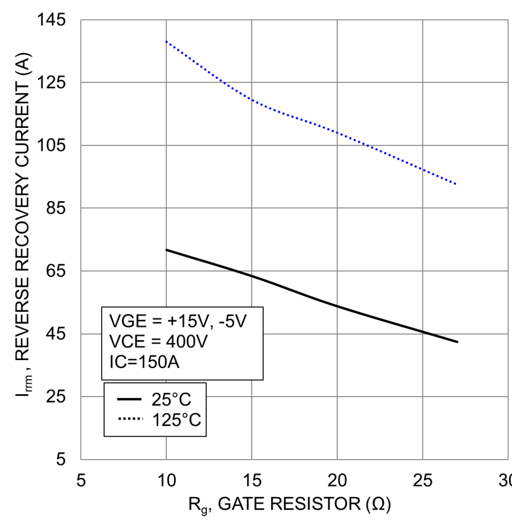


Figure 39. Typical Reverse Recovery Current vs. R_G

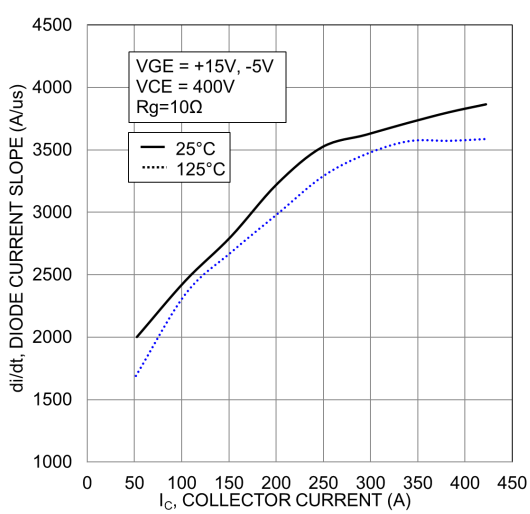


Figure 37. Typical di/dt vs. IC

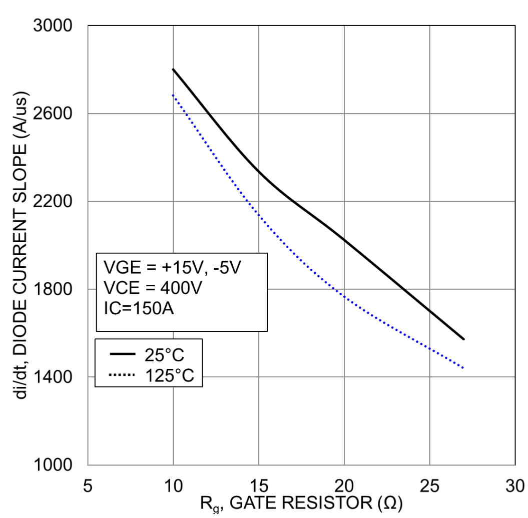


Figure 38. Typical di/dt vs. R_G

TYPICAL CHARACTERISTICS – Q2/Q3 IGBT COMUNATES D1/D4 DIODE

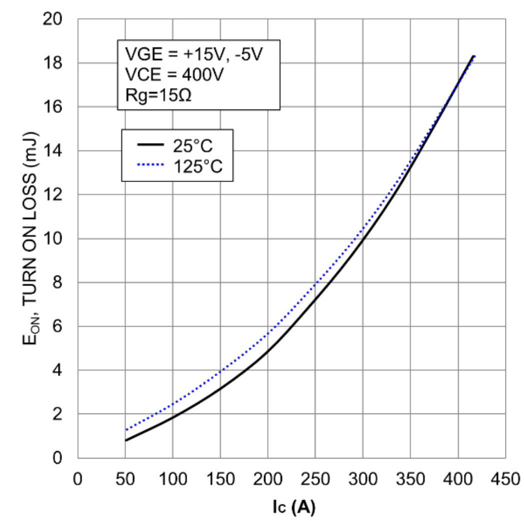


Figure 40. Typical Switching Loss Eon vs. IC

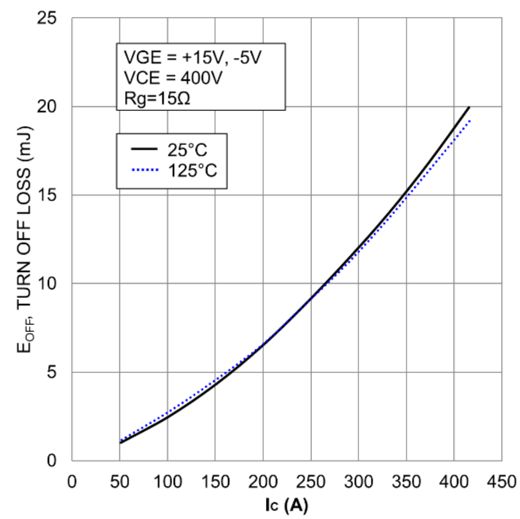


Figure 45. Typical Switching Loss Eoff vs. IC

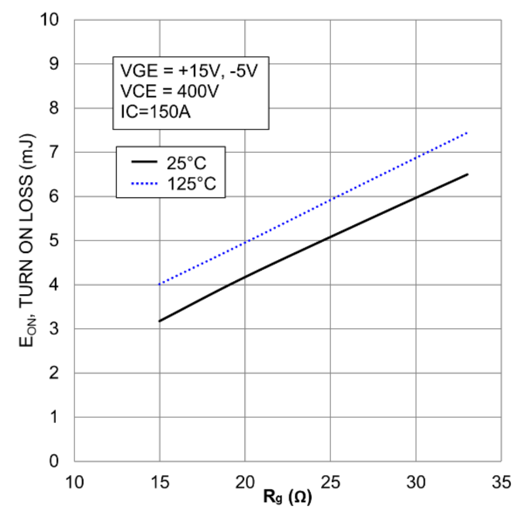


Figure 41. Typical Switching Loss Eon vs. R_G

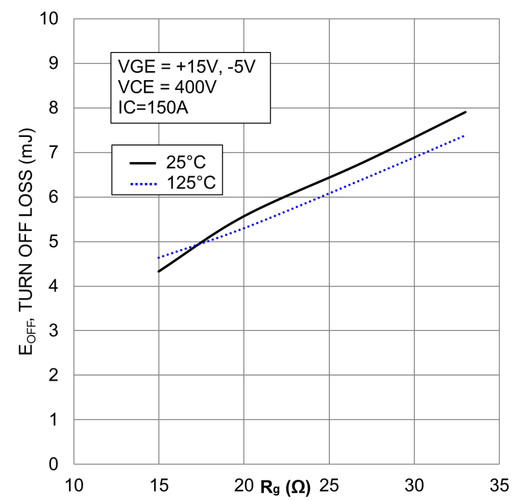


Figure 42. Typical Switching Loss Eoff vs. R_G

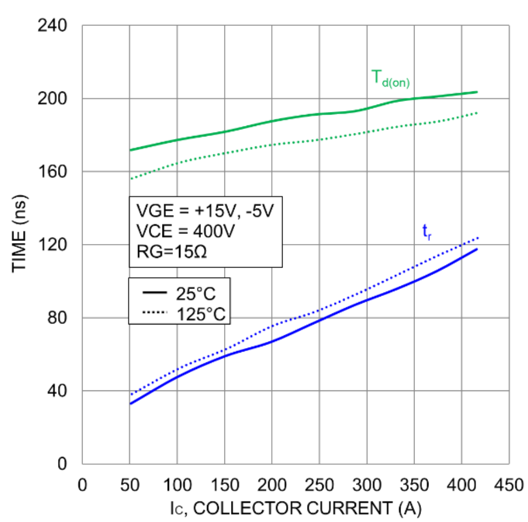


Figure 43. Typical Turn−On Switching Time vs. IC

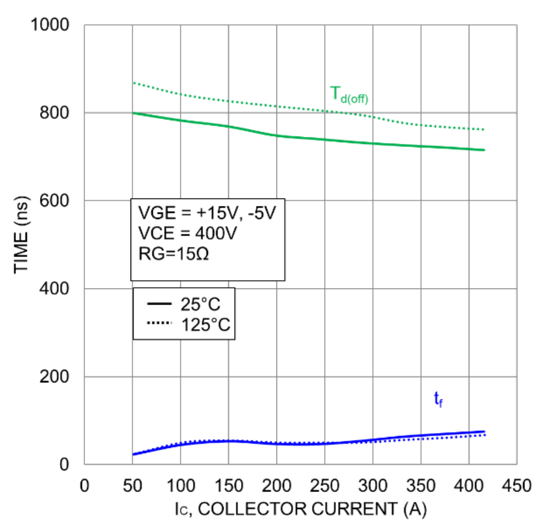


Figure 44. Typical Turn−Off Switching Time vs. IC

TYPICAL CHARACTERISTICS – Q2/Q3 IGBT COMUNATES D1/D4 DIODE (continued)

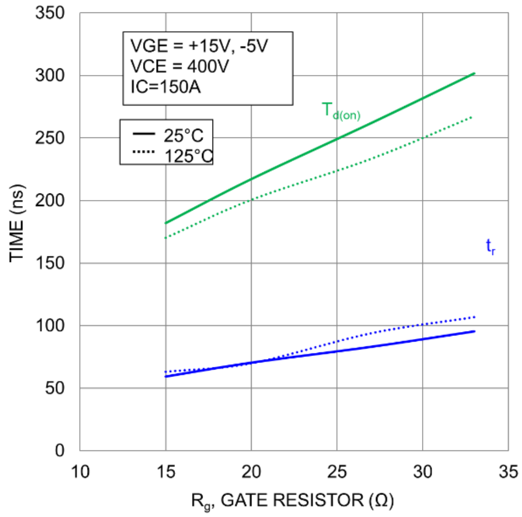


Figure 46. Typical Turn−On Switching Time vs. R_G

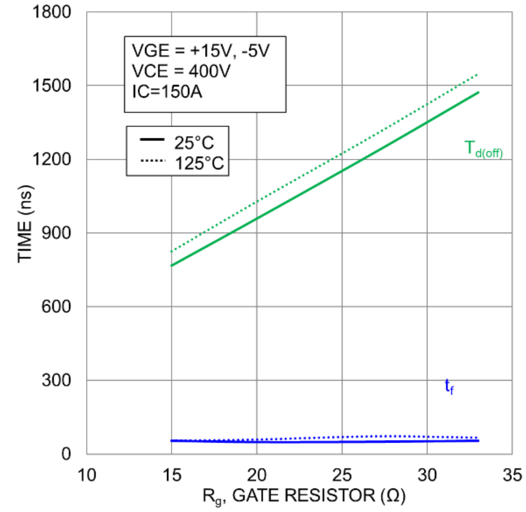


Figure 47. Typical Turn−Off Switching Time vs. R_G

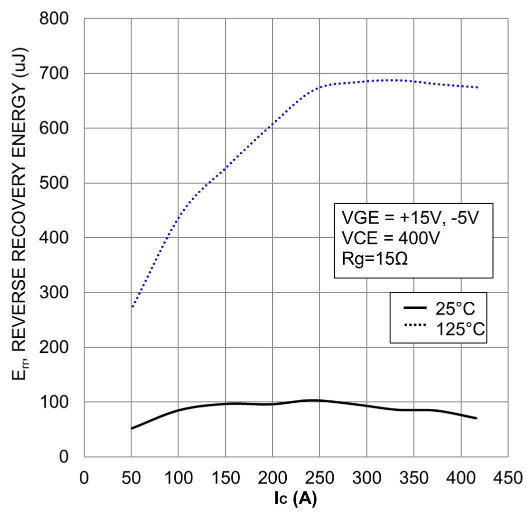


Figure 48. Typical Reverse Recovery Energy Loss vs. IC

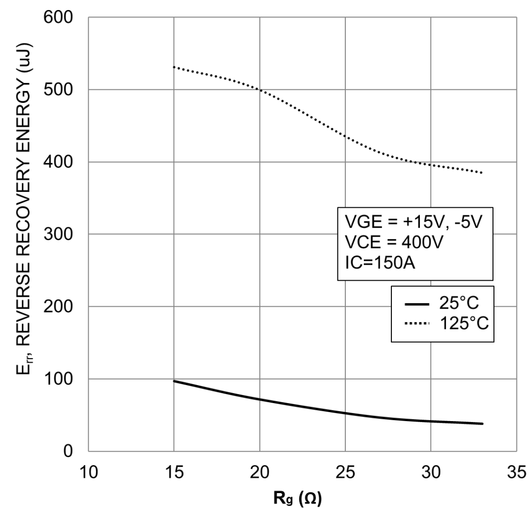


Figure 51. Typical Reverse Recovery Energy Loss vs. R_G

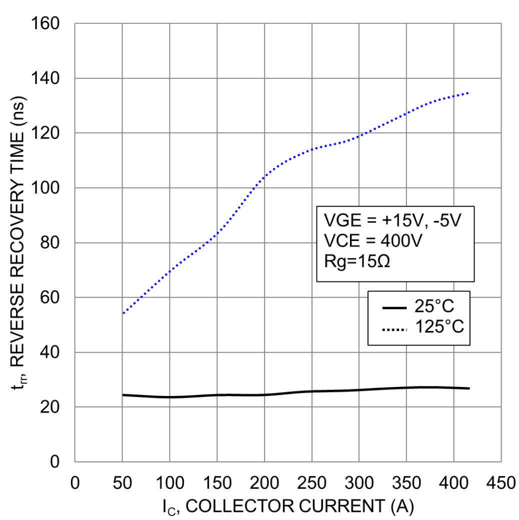


Figure 49. Typical Reverse Recovery Time vs. IC

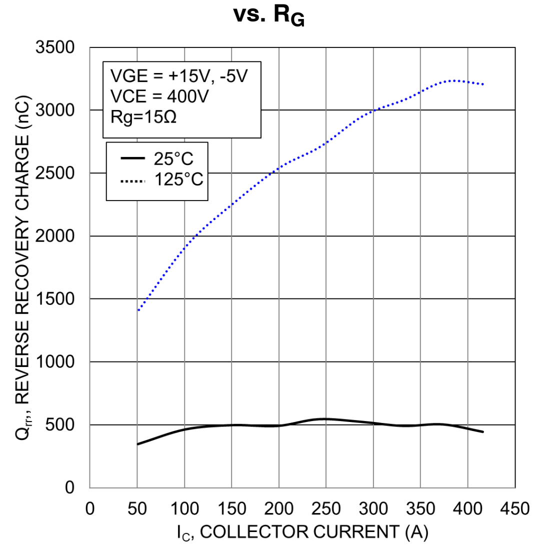


Figure 50. Typical Reverse Recovery Charge vs. IC

TYPICAL CHARACTERISTICS – Q2/Q3 IGBT COMUNATES D1/D4 DIODE (continued)

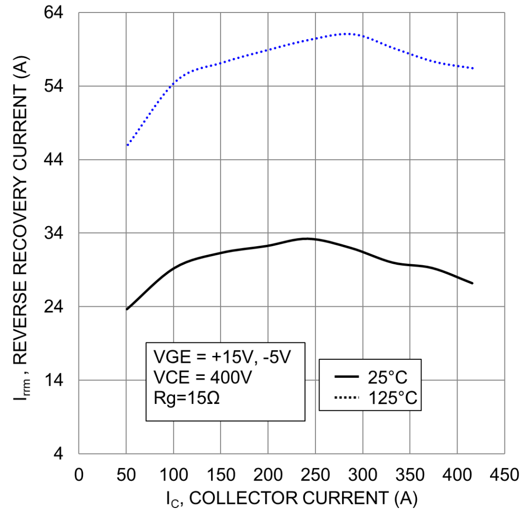


Figure 52. Typical Reverse Recovery Current vs. IC

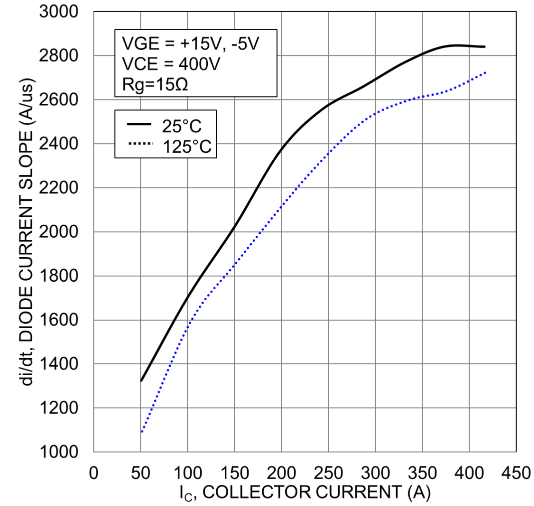


Figure 53. Typical di/dt Current Slope vs. IC

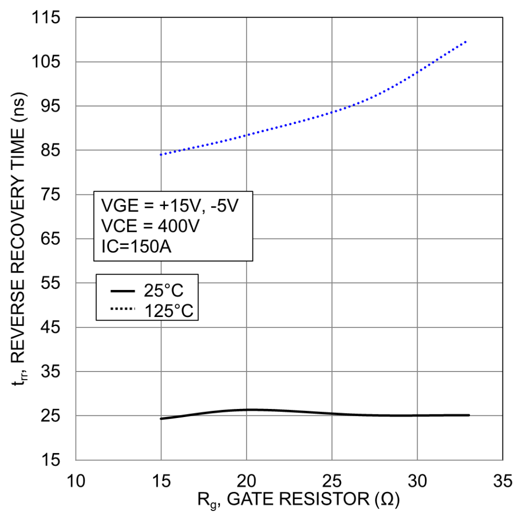


Figure 54. Typical Reverse Recovery Time vs. R_G

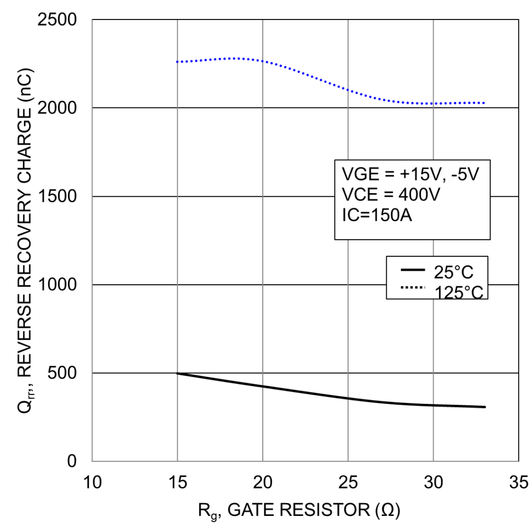


Figure 55. Typical Reverse Recovery Charge vs. R_G

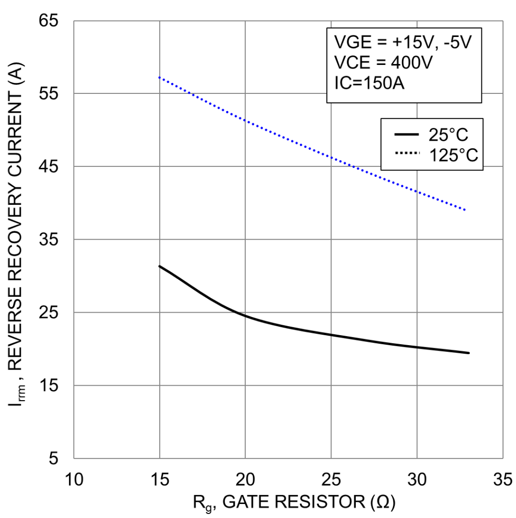


Figure 56. Typical Reverse Recovery Peak Current vs. R_G

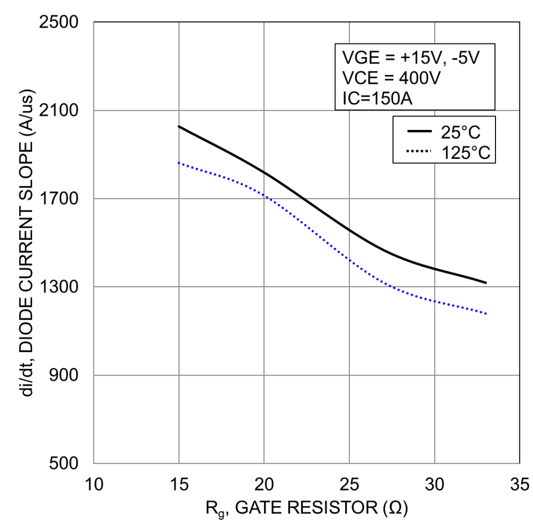


Figure 57. Typical di/dt vs. R_G

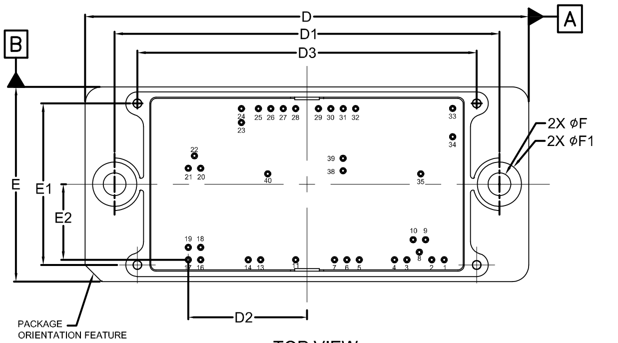
ORDERING INFORMATION

Orderable Part Number	Marking	Package	Shipping
NXH450N65L4Q2F2S1G	NXH450N65L4Q2F2S1G	PIM40, Q2PACK (Pb−Free and Halide−Free)	12 Units / Blister Tray

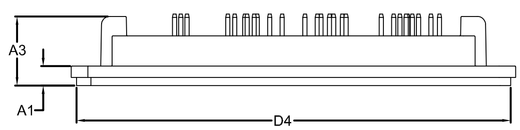
PACKAGE DIMENSIONS

PIM40, 107.2x47
CASE 180BE
ISSUE B

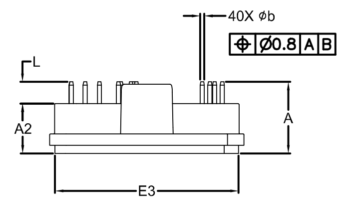
DIM	MILLIMETERS MIN.	NOM.	MAX.
A	16.63	17.23	17.83
A1	4.50	4.70	4.90
A2	11.60	12.00	12.40
A3	16.40	16.70	17.00
b	0.95	1.00	1.05
D	106.80	107.20	107.60
D1	92.90	93.00	93.10
D2	28.40	28.70	29.00
D3	81.80	82.00	82.20
D4	104.35	104.75	105.15
E	46.60	47.00	47.40
E1	38.80	39.00	39.20
E2	17.95	18.25	18.55
E3	35.22	44.40	35.82
F	5.40	5.50	5.60
F1	10.70 REF		
L	5.03	5.23	5.43



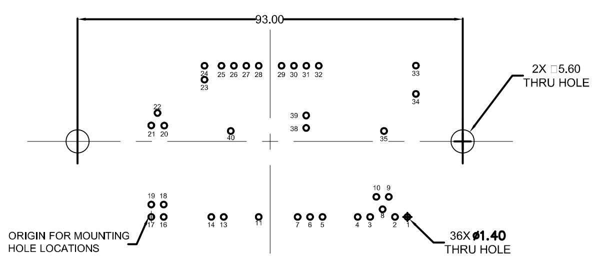
TOP VIEW



SIDE VIEW



END VIEW



RECOMMENDED MOUNTING PATTERN*

For additional information on our Pb-Free strategy and soldering details, please download the On Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTE 4

PIN	PIN POSITION X	Y	PIN	PIN POSITION X	Y
1	61.85	0.0	21	0.0	22.1
2	58.85	0.0	22	1.5	25.1
3	52.85	0.0	23	12.85	33.15
4	49.85	0.0	24	12.85	36.5
5	41.35	0.0	25	16.95	36.5
6	38.35	0.0	26	19.95	36.5
7	35.35	0.0	27	22.95	36.5
8	55.85	1.85	28	25.95	36.5
9	57.35	4.85	29	31.45	36.5
10	54.35	4.85	30	34.45	36.5
11	25.95	0.0	31	37.45	36.5
13	17.5	0.0	32	40.45	36.5
14	14.5	0.0	33	63.9	36.55
16	3.0	0.0	34	63.9	29.7
17	0.0	0.0	35	56.2	20.75
18	3.0	3.0	38	37.4	21.5
19	0.0	3.0	39	37.4	24.5
20	3.0	22.1	40	19.2	20.75

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME 7 14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS b APPLY TO THE PLATED TERMINALS AND ARE MEASURED WHERE THE PIN EXITS THE PACKAGE BODY.
4. POSITION OF THE CENTER OF THE TERMINALS IS DETERMINED FROM PIN 17. POSITIONAL TOLERANCE, AS NOTED IN THE DRAWING, APPLIES TO EACH TERMINAL.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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