

F1-2PACK SiC MOSFET Module

Product Preview

NXH010P120MNF1PTNG, NXH010P120MNF1PNG

General Description

The NXH010P120MNF1 is a power module containing an 10 mΩ/1200 V SiC MOSFET half bridge and a thermistor in an F1 package.

Features

- 10 mΩ/1200V SiC MOSFET Half Bridge
- Thermistor
- Options With Pre-Applied Thermal Interface Material (TIM) and Without Pre-Applied TIM
- Press-Fit Pins

Typical Applications

- Solar Inverter
- Uninterruptible Power Supplies
- Electric Vehicle Charging Stations
- Industrial Power

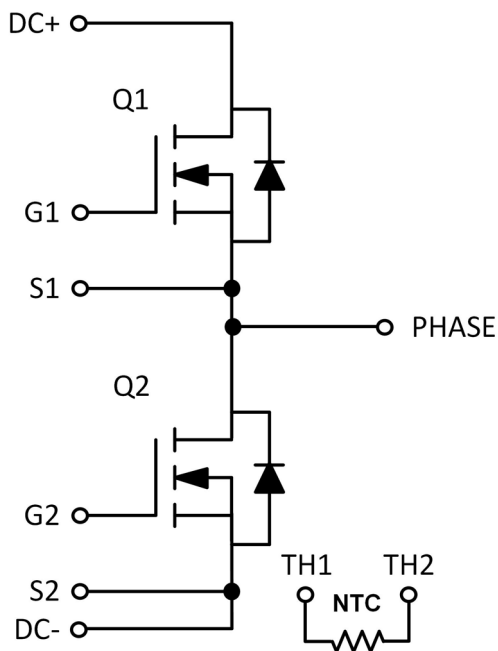


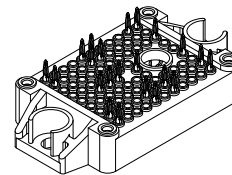
Figure 1. NXH010P120MNF1 Schematic Diagram

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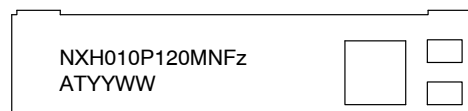
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PIM18 33.8x42.5 (PRESS FIT)
CASE 180BW

MARKING DIAGRAM



NXH010P120MNFz = Specific Device Code
z = PTNG/PNG
AT = Assembly & Test Site Code
YYWW = Year and Work Week Code

ORDERING INFORMATION

See detailed ordering and shipping information on page of this data sheet.

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PIN CONNECTIONS

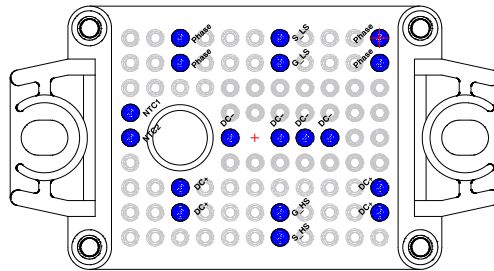


Figure 2. Pin Connections

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Description
A5	TH1	Thermistor Connection 1
A6	TH2	Thermistor Connection 2
C2	DC+	DC Positive Bus connection
C3	DC+	DC Positive Bus connection
C8	PHASE	Center point of half bridge
C9	PHASE	Center point of half bridge
E5	DC-	DC Negative Bus connection
G1	S1	Q1 Kelvin Emitter (High side switch)
G2	G1	Q1 Gate (High side switch)
G5	DC-	DC Negative Bus connection
G8	G2	Q2 Gate (Low side switch)
G9	S2	Q2 Kelvin Emitter (High side switch)
H5	DC-	DC Negative Bus connection
I5	DC-	DC Negative Bus connection
K2	DC+	DC Positive Bus connection
K3	DC+	DC Positive Bus connection
K8	PHASE	Center point of half bridge
K9	PHASE	Center point of half bridge

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Table 1. ABSOLUTE MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
SIC MOSFET			
Drain–Source Voltage	V_{DSS}	1200	V
Gate–Source Voltage	V_{GS}	+25/–15	V
Continuous Drain Current @ $T_c = 80^\circ\text{C}$ ($T_J = 175^\circ\text{C}$)	I_D	114	A
Pulsed Drain Current ($T_J = 175^\circ\text{C}$)	I_{Dpulse}	342	A
Maximum Power Dissipation ($T_J = 175^\circ\text{C}$)	P_{tot}	250	W
Short Circuit Withstand Time @ $V_{GE} = -5\text{V}/20\text{ V}$, $V_{CE} = 600\text{ V}$, $T_J \leq 150^\circ\text{C}$	T_{sc}	2	μs
Minimum Operating Junction Temperature	T_{JMIN}	–40	$^\circ\text{C}$
Maximum Operating Junction Temperature	T_{JMAX}	175	$^\circ\text{C}$
THERMAL PROPERTIES			
Storage Temperature range	T_{stg}	–40 to 150	$^\circ\text{C}$
INSULATION PROPERTIES			
Isolation test voltage, $t = 1\text{ sec}$, 60 Hz	V_{is}	4000	V_{RMS}
Creepage distance		12.7	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.

RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Module Operating Junction Temperature	T_J	–40	150	$^\circ\text{C}$

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SIC MOSFET CHARACTERISTICS						
Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_D = 400\ \mu\text{A}$	$V_{(BR)DSS}$	1200	–	–	V
Zero Gate Voltage Drain Current	$V_{GS} = 0\text{ V}$, $V_{DS} = 1200\text{ V}$	I_{DSS}	–	–	200	μA
Drain–Source On Resistance	$V_{GS} = 20\text{ V}$, $I_D = 100\text{ A}$, $T_J = 25^\circ\text{C}$	$R_{DS(ON)}$	–	10.5	14	$\text{m}\Omega$
	$V_{GS} = 20\text{ V}$, $I_D = 100\text{ A}$, $T_J = 125^\circ\text{C}$		–	14.1	–	
	$V_{GS} = 20\text{ V}$, $I_D = 100\text{ A}$, $T_J = 150^\circ\text{C}$		–	14.5	–	
Gate–Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 40\text{ mA}$	$V_{GS(TH)}$	1.8	2.90	4.3	V
Gate Leakage Current	$V_{GS} = -10/20\text{ V}$, $V_{DS} = 0\text{ V}$	I_{GSS}	–1000	–	1000	nA
Forward Transconductance	$V_{DS} = 10\text{ V}$, $I_D = 100\text{ A}$	g_{FS}		31		S
Internal Gate Resistance		R_G		TBD		Ω
Input Capacitance	$V_{DS} = 800\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	C_{ISS}	–	4707	–	pF
Reverse Transfer Capacitance		C_{RSS}	–	39	–	
Output Capacitance		C_{OSS}	–	548	–	
C_{OSS} Stored Energy	$V_{DS} = 0\text{ V to } 800\text{ V}$, $V_{GS} = 0\text{ V}$	E_{OSS}	–	TBD	–	μJ

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ELECTRICAL CHARACTERISTICS (continued)

T_A = 25°C unless otherwise noted

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SiC MOSFET CHARACTERISTICS						
Total Gate Charge	V _{DS} = 800 V, V _{GS} = 20 V, I _D = 100 A	Q _{G(TOTAL)}	–	454	–	nC
Gate–Source Charge		Q _{GS}	–	129	–	nC
Gate–Drain Charge		Q _{GD}	–	131	–	nC
Turn–on Delay Time	T _J = 25°C V _{DS} = 800 V, I _D = 100 A V _{GS} = –5V/18V, R _G = 3.9 Ω	t _{d(on)}	–	TBD	–	ns
Rise Time		t _r	–	TBD	–	
Turn–off Delay Time		t _{d(off)}	–	TBD	–	
Fall Time		t _f	–	TBD	–	
Turn–on Switching Loss per Pulse		E _{ON}	–	2.05	–	mJ
Turn off Switching Loss per Pulse		E _{OFF}	–	1.1	–	
Turn–on Delay Time	T _J = 150°C V _{DS} = 800 V, I _D = 100 A V _{GS} = –5V/18V, R _G = 3.9 Ω	t _{d(on)}	–	TBD	–	ns
Rise Time		t _r	–	TBD	–	
Turn–off Delay Time		t _{d(off)}	–	TBD	–	
Fall Time		t _f	–	TBD	–	
Turn–on Switching Loss per Pulse		E _{ON}	–	1.95	–	mJ
Turn off Switching Loss per Pulse		E _{OFF}	–	1.3	–	
Diode Forward Voltage	I _D = 100 A, T _J = 25°C	V _{SD}	–	3.94	6	V
	I _D = 100 A, T _J = 150°C		–	3.42	–	
Reverse Recovery Time	T _J = 25°C V _{DS} = 800 V, I _D = 100 A V _{GS} = –5V/18V, R _G = 3.9 Ω	t _{rr}	–	TBD	–	ns
Reverse Recovery Charge		Q _{rr}	–	TBD	–	nC
Peak Reverse Recovery Current		I _{RRM}	–	TBD	–	A
Peak Rate of Fall of Recovery Current		di/dt	–	TBD	–	A/μs
Reverse Recovery Energy		E _{rr}	–	TBD	–	μJ
Reverse Recovery Time		T _J = 25°C V _{DS} = 800 V, I _D = 100 A V _{GS} = –5V/18V, R _G = 3.9 Ω	t _{rr}	–	TBD	–
Reverse Recovery Charge	Q _{rr}		–	TBD	–	μC
Peak Reverse Recovery Current	I _{RRM}		–	TBD	–	A
Peak Rate of Fall of Recovery Current	di/dt		–	TBD	–	A/μs
Reverse Recovery Energy	E _{rr}		–	TBD	–	μJ
Thermal Resistance – chip–to–case	M1,M2		R _{thJC}	–	0.23	–
Thermal Resistance – chip–to–heatsink	Thermal Resistance – chip–to–heatsink, Thermal grease, Thickness = 2 Mil _2%, A = 2.8 W/mK	R _{thJH}	–	0.38	–	°C/W

THERMISTOR CHARACTERISTICS

Nominal resistance	T = 25°C	R ₂₅	–	5	–	kΩ
Nominal resistance	T = 100°C	R ₁₀₀	–	457	–	Ω
Deviation of R25		ΔR/R	–3	–	3	%
Power dissipation		P _D	–	50	–	mW
Power dissipation constant			–	5	–	mW/K
B–value	B(25/50), tolerance ±3%		–	3375	–	K
B–value	B(25/100), tolerance ±3%		–	3455	–	K

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ORDERING INFORMATION

Orderable Part Number	Specific Device Marking	Package Type	Shipping [†]
NXH010P120MNF1PNG	NXH010P120MNF1PNG	F1-2PACK: Case 180BW Press-fit Pins (Pb-Free and Halide-Free)	28 Units / Blister Tray
NXH010P120MNF1PTNG	NXH010P120MNF1PTNG	F1-2PACK: Case 180BW Press-fit Pins with pre-applied thermal interface material (TIM) (Pb-Free and Halide-Free)	28 Units / Blister Tray

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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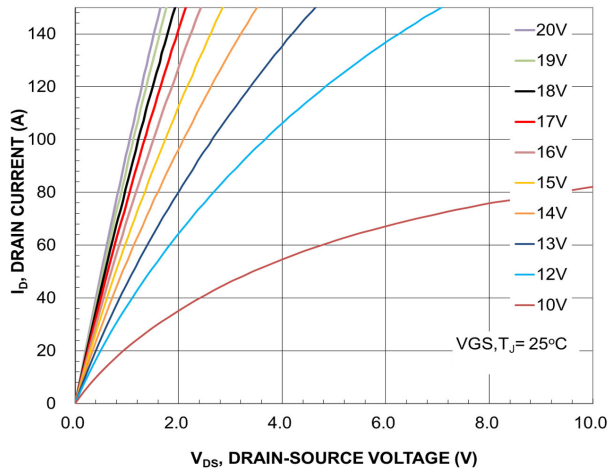


Figure 3. MOSFET Typical Output Characteristics

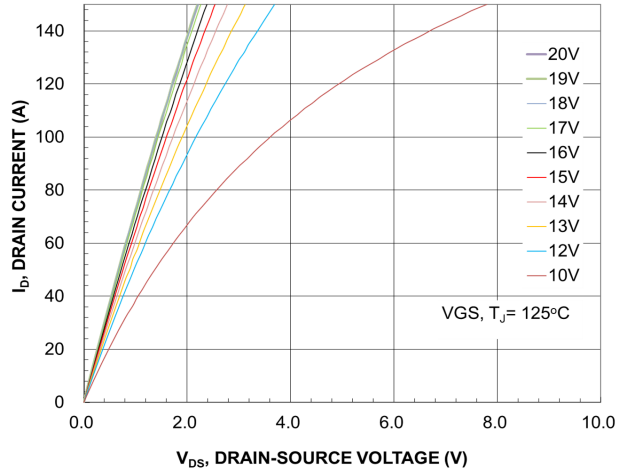


Figure 4. MOSFET Typical Output Characteristics

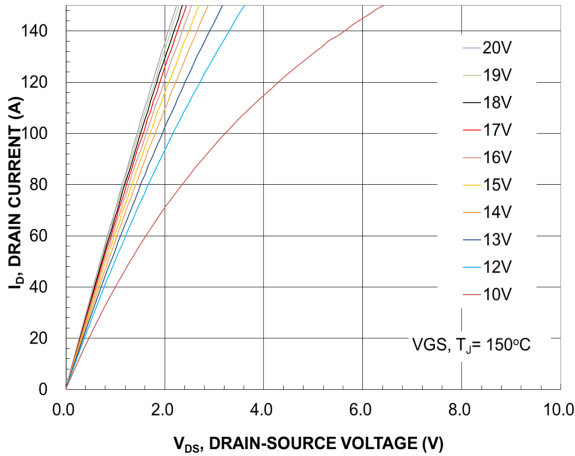


Figure 5. MOSFET Typical Output Characteristics

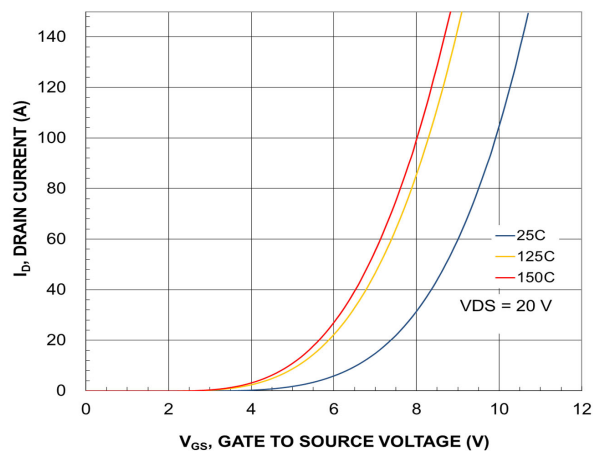


Figure 6. MOSFET Typical Transfer Characteristics

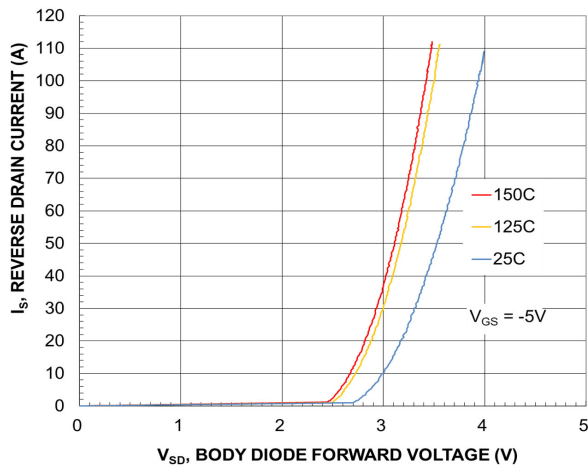


Figure 7. Body Diode Forward Characteristic

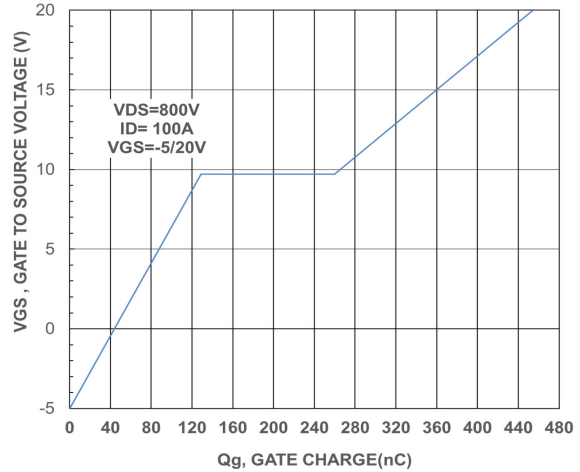


Figure 8. Gate-to-Source Voltage vs. Total Charge

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TYPICAL CHARACTERISTICS

SiC MOSFET (M1, M2)

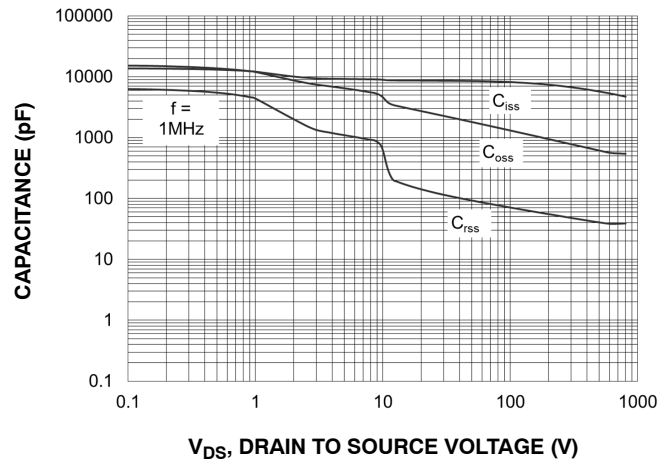


Figure 9. Capacitance vs. Drain-to-Source Voltage

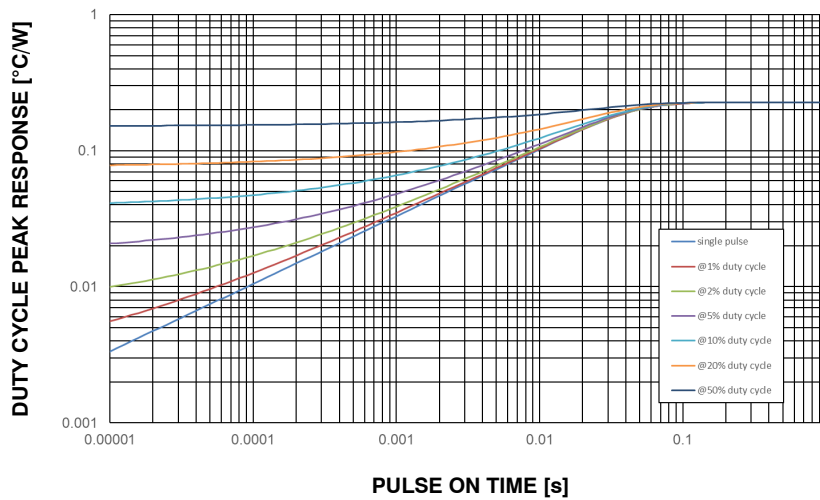


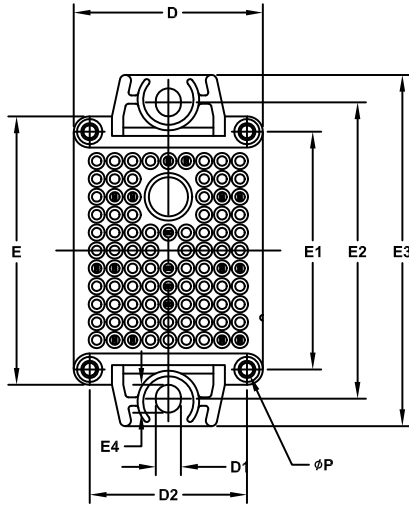
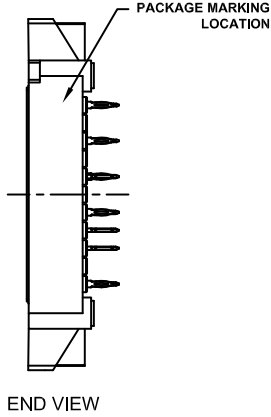
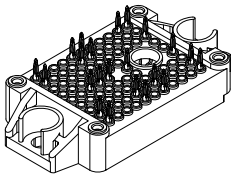
Figure 10. SiC Mosfet Junction-to-Case Transient Thermal Impedance

Element #	M1		M2	
	Rth (K/W)	Cth (Ws/K)	Rth (K/W)	Cth (Ws/K)
1	0.00569	0.00195	0.01290	0.00461
2	0.01079	0.00951	0.02387	0.02538
3	0.03005	0.01813	0.04253	0.02953
4	0.08398	0.08121	0.07199	0.08994
5	0.09325	0.11117	0.07823	0.06854

Figure 11. Table of Cauer Networks-M1, M2

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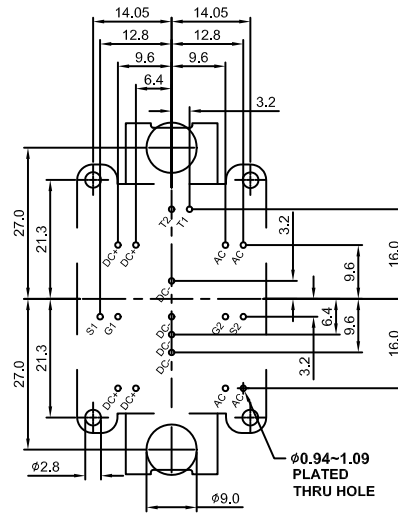
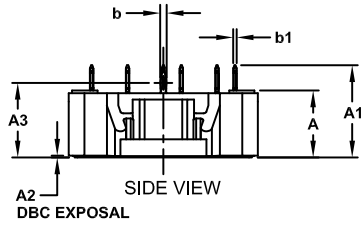
PIM18 33.8x42.5 (PRESS FIT) CASE 180BW ISSUE A




NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS
2. PIN POSITION TOLERANCE IS $\pm 0.4\text{mm}$

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	11.65	12.00	12.35
A1	16.00	16.50	17.00
A2	0.00	0.35	0.60
A3	12.85	13.35	13.85
b	1.15	1.20	1.25
b1	0.59	0.64	0.69
D	33.50	33.80	34.10
D1	4.40	4.50	4.60
D2	27.95	28.10	28.25
E	47.70	48.00	48.30
E1	42.35	42.50	42.65
E2	52.90	53.00	53.10
E3	62.30	62.80	63.30
E4	4.90	5.00	5.10
P	2.20	2.30	2.40



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