# Silicon Carbide (SiC) Module – EliteSiC, 3 mohm SiC M3 MOSFET, 1200 V, 2-PACK Half Bridge Topology, F2 Package with Si3N4 DBC

# NXH003P120M3F2PTNG

The NXH003P120M3F2PTNG is a power module containing 3 mΩ / 1200 V SiC MOSFET half−bridge and a thermistor with Si3N4 DBC in an F2 package.

### Features

- 3 mΩ / 1200 V M3S SiC MOSFET Half−Bridge
- Si3N4 DBC
- Thermistor
- Pre−Applied Thermal Interface Material (TIM)
- Press−Fit Pins
- These Devices are Pb−Free, Halide Free and are RoHS Compliant

### Typical Applications

- Solar Inverter
- Uninterruptible Power Supplies
- Electric Vehicle Charging Stations
- Industrial Power

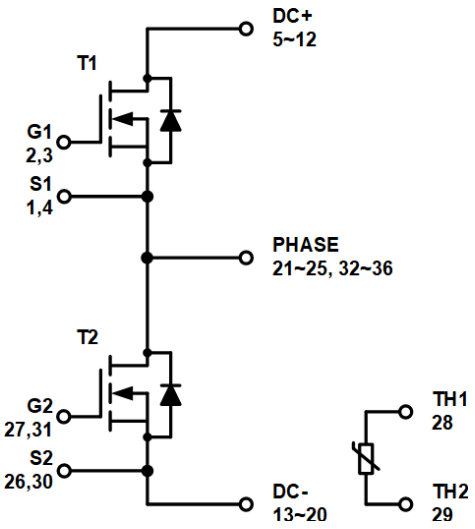
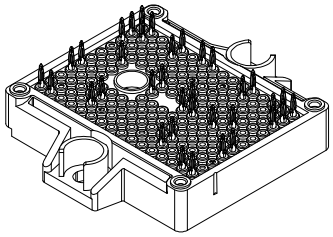


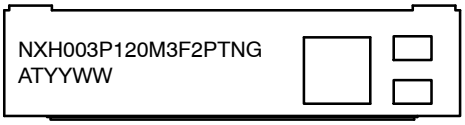

**Figure 1. NXH003P120MNF2 Schematic Diagram**

### PACKAGE PICTURE



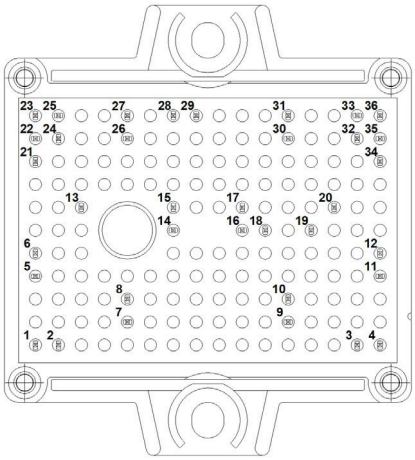
**PIM36 56.7x42.5 (PRESS FIT)**
**CASE 180BY**

### MARKING DIAGRAM




| | |
|---|---|
| NXH003P120M3F2PTNG | = Specific Device Code |
| AT | = Assembly & Test Site Code |
| YWW | = Year and Work Week Code |

### PIN CONNECTIONS



See Pin Function Description for pin names

### ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

## PIN FUNCTION DESCRIPTION

| Pin | Name | Description |
|---|---|---|
| 1 | S1 | Q1 Kelvin Emitter (High side switch) |
| 2 | G1 | Q1 Gate (High side switch) |
| 3 | G1 | Q1 Gate (High side switch) |
| 4 | S1 | Q1 Kelvin Emitter (High side switch) |
| 5 | DC+ | DC Positive Bus connection |
| 6 | DC+ | DC Positive Bus connection |
| 7 | DC+ | DC Positive Bus connection |
| 8 | DC+ | DC Positive Bus connection |
| 9 | DC+ | DC Positive Bus connection |
| 10 | DC+ | DC Positive Bus connection |
| 11 | DC+ | DC Positive Bus connection |
| 12 | DC+ | DC Positive Bus connection |
| 13 | DC* | DC Negative Bus connection |
| 14 | DC− | DC Negative Bus connection |
| 15 | DC− | DC Negative Bus connection |
| 16 | DC− | DC Negative Bus connection |
| 17 | DC− | DC Negative Bus connection |
| 18 | DC− | DC Negative Bus connection |
| 19 | DC− | DC Negative Bus connection |
| 20 | DC− | DC Negative Bus connection |
| 21 | PHASE | Center point of half bridge |
| 22 | PHASE | Center point of half bridge |
| 23 | PHASE | Center point of half bridge |
| 24 | PHASE | Center point of half bridge |
| 25 | PHASE | Center point of half bridge |
| 26 | S2 | Q2 Kelvin Emitter (Low side switch) |
| 27 | G2 | Q2 Gate (Low side switch) |
| 28 | TH1 | Thermistor Connection 1 |
| 29 | TH2 | Thermistor Connection 2 |
| 30 | S2 | Q2 Kelvin Emitter (Low side switch) |
| 31 | G2 | Q2 Gate (Low side switch) |
| 32 | PHASE | Center point of half bridge |
| 33 | PHASE | Center point of half bridge |
| 34 | PHASE | Center point of half bridge |
| 35 | PHASE | Center point of half bridge |
| 36 | PHASE | Center point of half bridge |

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| **SiC MOSFET** | | | |
| Drain−Source Voltage | $V_{DSS}$ | 1200 | V |
| Gate−Source Voltage | $V_{GS}$ | +22/−10 | V |
| Continuous Drain Current @ $T_c$ = 80°C ($T_J$ = 175°C) | $I_D$ | 435 | A |
| Pulsed Drain Current ($T_J$ = 175°C) | $I_{Dpulse}$ | 870 | A |
| Maximum Power Dissipation @ $T_c$ = 80°C ($T_J$ = 175°C) | $P_{tot}$ | 1482 | W |
| Minimum Operating Junction Temperature | $T_{JMIN}$ | −40 | °C |
| Maximum Operating Junction Temperature | $T_{JMAX}$ | 175 | °C |
| **THERMAL PROPERTIES** | | | |
| Storage Temperature Range | $T_{stg}$ | −40 to 150 | °C |
| TIM Layer Thickness | $T_{TIM}$ | 160 ±20 | μm |
| **INSULATION PROPERTIES** | | | |
| Isolation Test Voltage, t = 1 s, 60 Hz | $V_{is}$ | 4800 | $V_{RMS}$ |
| Creepage Distance | | 12.7 | mm |
| CTI | | 600 | |
| Substrate Ceramic Material | | Si3N4 | |
| Substrate Ceramic Material Thickness | | 0.38 | mm |
| Substrate Warpage (Note 2) | W | Max 0.18 | mm |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. Height difference between horizontal plane and substrate copper bottom.

## RECOMMENDED OPERATING RANGES

| Rating | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Module Operating Junction Temperature | $T_J$ | −40 | 150 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SiC MOSFET CHARACTERISTICS** | | | | | | |
| Zero Gate Voltage Drain Current | $V_{GS}$ = 0 V, $V_{DS}$ = 1200 V | $I_{DSS}$ | – | – | 300 | μA |
| Drain−Source On Resistance | $V_{GS}$ = 18 V, $I_D$ = 200 A, $T_J$ = 25°C | $R_{DS(ON)}$ | – | 3.19 | 5 | mΩ |
| | $V_{GS}$ = 18 V, $I_D$ = 200 A, $T_J$ = 125°C | | – | 5.25 | – | |
| | $V_{GS}$ = 18 V, $I_D$ = 200 A, $T_J$ = 150°C | | – | 5.88 | – | |
| Gate−Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 160 mA | $V_{GS(TH)}$ | 1.8 | 2.4 | 4.4 | V |
| Gate Leakage Current | $V_{GS}$ = −10 V / 20 V, $V_{DS}$ = 0 V | $I_{GSS}$ | −800 | – | 800 | nA |
| Input Capacitance | $V_{DS}$ = 800 V, $V_{GS}$ = 0 V, f = 100 kHz | $C_{ISS}$ | – | 20889 | – | pF |
| Reverse Transfer Capacitance | | $C_{RSS}$ | – | 90 | – | |
| Output Capacitance | | $C_{OSS}$ | – | 1225 | – | |

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (continued)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SiC MOSFET CHARACTERISTICS** | | | | | | |
| Total Gate Charge | $V_{DS}$ = 800 V, $V_{GS}$ = −5/20 V, $I_D$ = 200 A | $Q_{G(TOTAL)}$ | – | 1195 | – | nC |
| Gate−Source Charge | | $Q_{GS}$ | – | 232 | – | nC |
| Gate−Drain Charge | | $Q_{GD}$ | – | 210 | – | nC |
| Turn−on Delay Time | $T_J$ = 25°C<br>$V_{DS}$= 600 V, $I_D$ = 200 A<br>$V_{GS}$ = −5 V / 18 V, $R_G$ = 1 Ω | $t_{d(on)}$ | – | 49 | – | ns |
| Rise Time | | $t_r$ | – | 17 | – | |
| Turn−off Delay Time | | $t_{d(off)}$ | – | 144 | – | |
| Fall Time | | $t_f$ | – | 16 | – | |
| Turn−on Switching Loss per Pulse | | $E_{ON}$ | – | 1.79 | – | mJ |
| Turn−off Switching Loss per Pulse | | $E_{OFF}$ | – | 1.13 | – | |
| Turn−on Delay Time | $T_J$ = 150°C<br>$V_{DS}$ = 600 V, $I_D$ = 200 A<br>$V_{GS}$ = −5 V / 18 V, $R_G$ = 1 Ω | $t_{d(on)}$ | – | 48 | – | ns |
| Rise Time | | $t_r$ | – | 15 | – | |
| Turn−off Delay Time | | $t_{d(off)}$ | – | 154 | – | |
| Fall Time | | $t_f$ | – | 15 | – | |
| Turn−on Switching Loss per Pulse | | $E_{ON}$ | – | 1.94 | – | mJ |
| Turn off Switching Loss per Pulse | | $E_{OFF}$ | – | 1.12 | – | |
| Diode Forward Voltage | $I_D$ = 200 A, $T_J$ = 25°C | $V_{SD}$ | – | 4.8 | 7.5 | V |
| | $I_D$ = 200 A, $T_J$ = 125°C | | – | 4.5 | – | |
| | $I_D$ = 200 A, $T_J$ = 150°C | | – | 4.4 | – | |
| Thermal Resistance − Chip−to−Case | M1, M2 | $R_{thJC}$ | – | 0.0641 | – | °C/W |
| Thermal Resistance − Chip−to−Heatsink | Thermal grease, Thickness = 2 Mil +2%, A = 2.8 W/mK | $R_{thJH}$ | – | 0.1605 | – | °C/W |
| **THERMISTOR CHARACTERISTICS** | | | | | | |
| Nominal Resistance | $T_{NTC}$ = 25°C | $R_{25}$ | – | 5 | – | kΩ |
| | $T_{NTC}$ = 100°C | $R_{100}$ | – | 493 | – | Ω |
| | $T_{NTC}$ = 150°C | $R_{150}$ | – | 159.5 | – | Ω |
| Deviation of $R_{100}$ | $T_{NTC}$ = 100°C | ΔR/R | −5 | – | 5 | % |
| Power Dissipation − Recommended limit | 0.15 mA, non−self−heating effect | $P_D$ | – | 0.1 | – | mW |
| Power Dissipation − Absolute maximum | 5 mA | $P_D$ | – | 34.2 | – | mW |
| Power Dissipation Constant | | | – | 1.4 | – | mW/K |
| B−value | B (25/50), tolerance ±2% | | – | 3375 | – | K |
| B−value | B (25/100), tolerance ±2% | | – | 3436 | – | K |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## ORDERING INFORMATION

| Orderable Part Number | Marking | Package | Shipping |
|---|---|---|---|
| NXH003P120M3F2PTNG | NXH003P120M3F2PTNG | F2HALFBR: Case 180BY<br>Press−fit Pins with pre−applied thermal interface material (TIM)<br>(Pb-Free / Halide Free) | 20 Units / Blister Tray |

## TYPICAL CHARACTERISTIC

(M1/M2 SiC MOSFET CHARACTERISTIC)

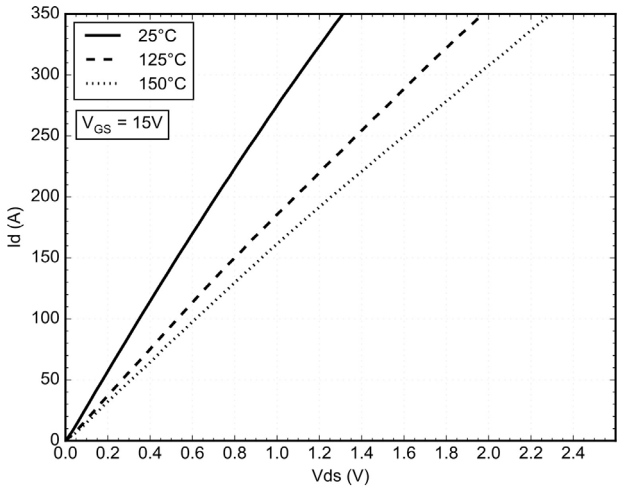



**Figure 2. MOSFET Typical Output Characteristic**

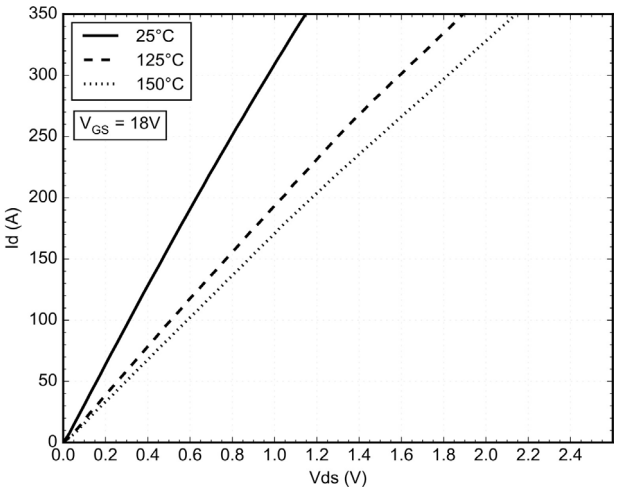



**Figure 3. MOSFET Typical Output Characteristic**

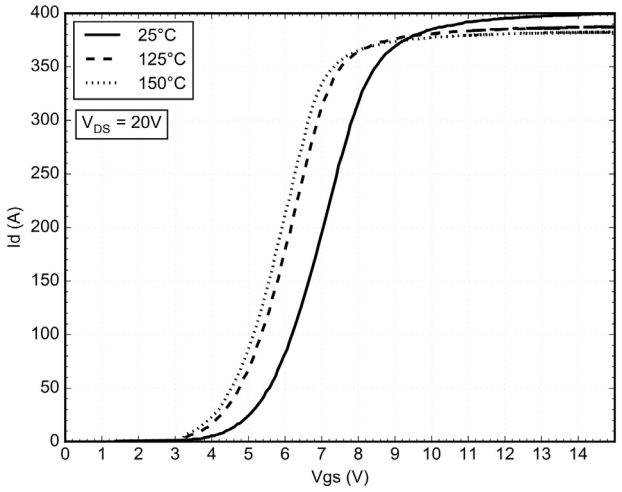



**Figure 4. MOSFET Typical Transfer Characteristic**

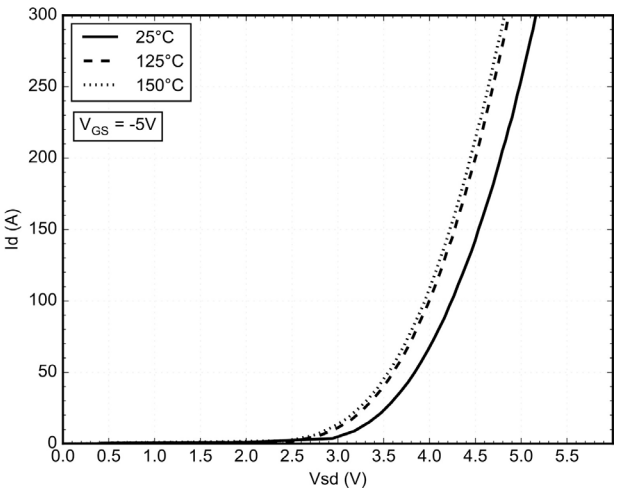



**Figure 5. Body Diode Forward Characteristic**

## TYPICAL CHARACTERISTIC

(M1/M2 SiC MOSFET CHARACTERISTIC)

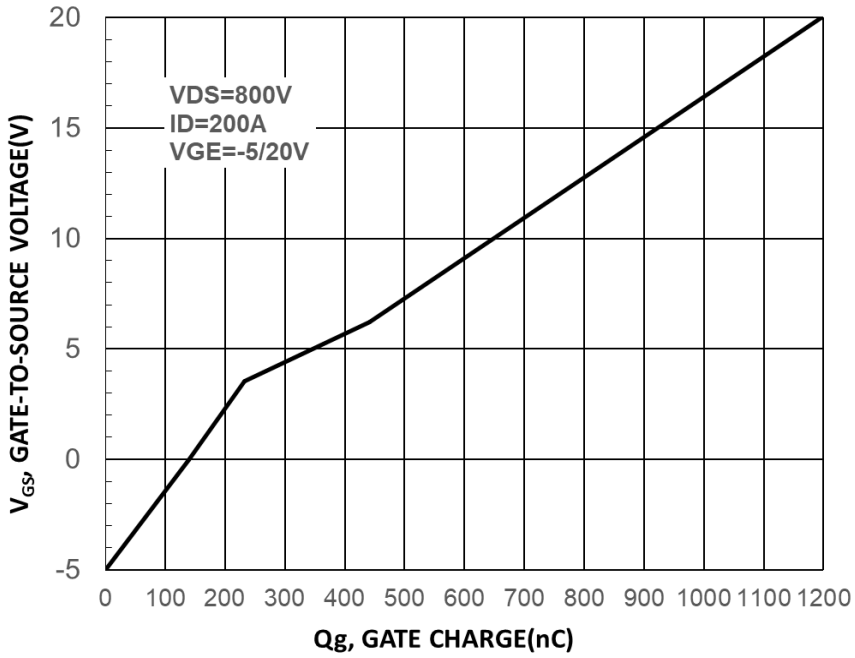



**Figure 6. Gate−to−Source Voltage vs. Total Charge**

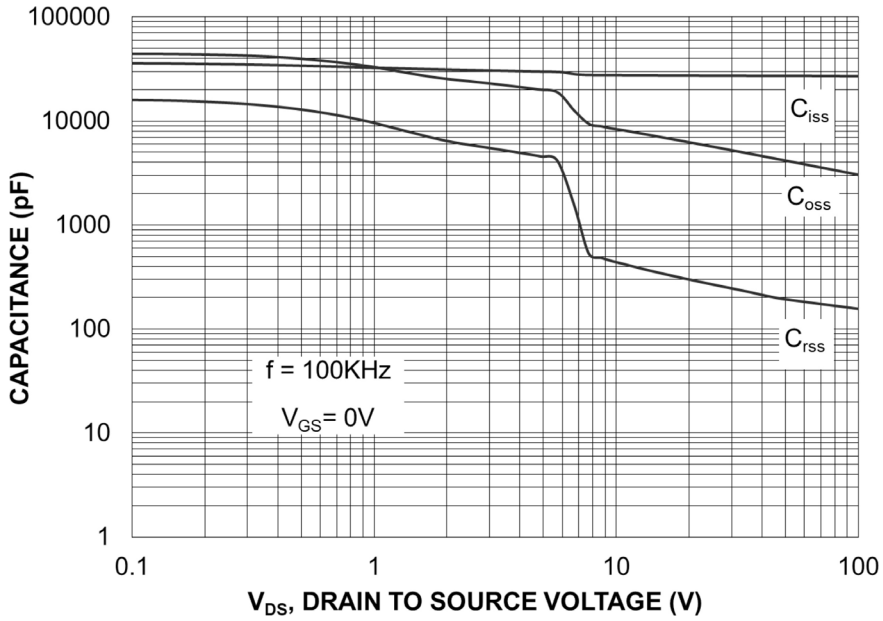



**Figure 7. Capacitance vs. Drain−to−Source Voltage**

## TYPICAL CHARACTERISTIC

(M1/M1 SiC MOSFET SWITCHING CHARACTERISTIC)

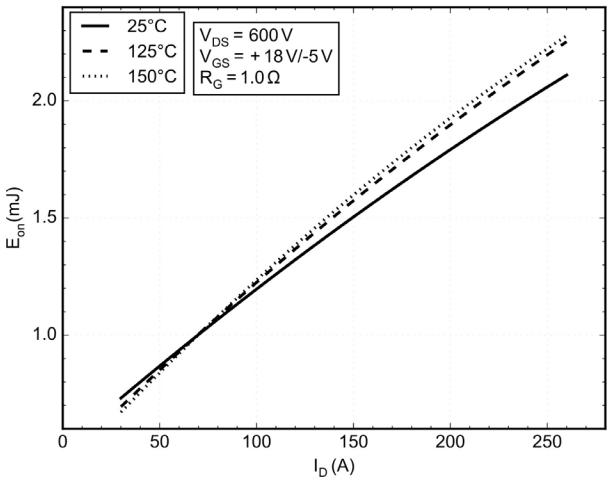



**Figure 8. Typical Switching Loss Eon vs. ID**

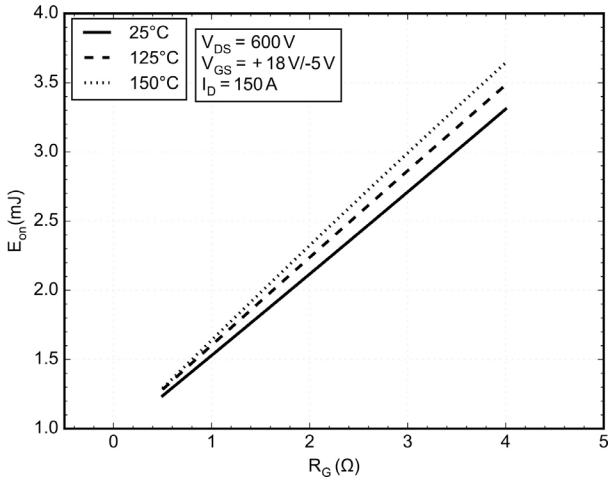



**Figure 9. Typical Switching Loss Eon vs. Rg**

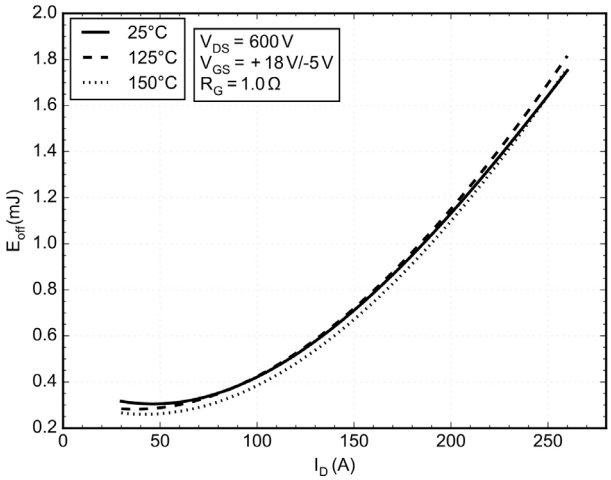



**Figure 10. Typical Switching Loss Eoff vs. ID**

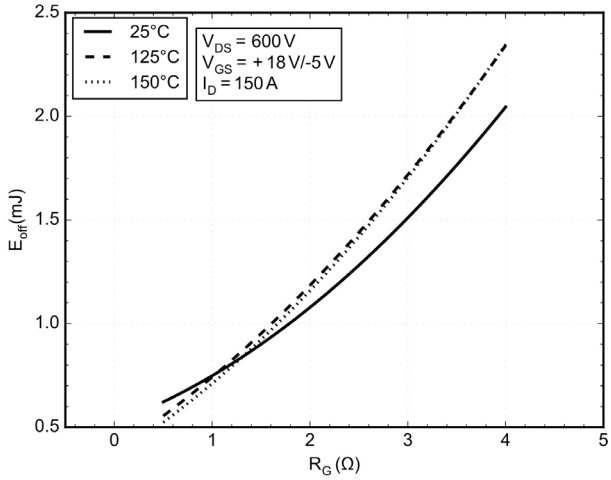



**Figure 11. Typical Switching Loss Eoff vs. Rg**

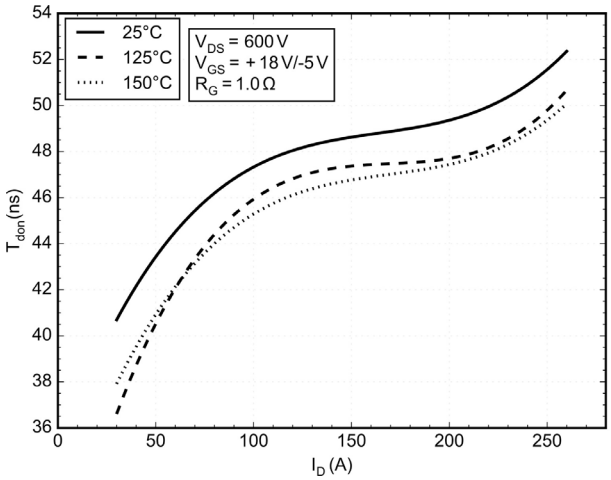



**Figure 12. Typical Switching Loss Tdon vs. ID**

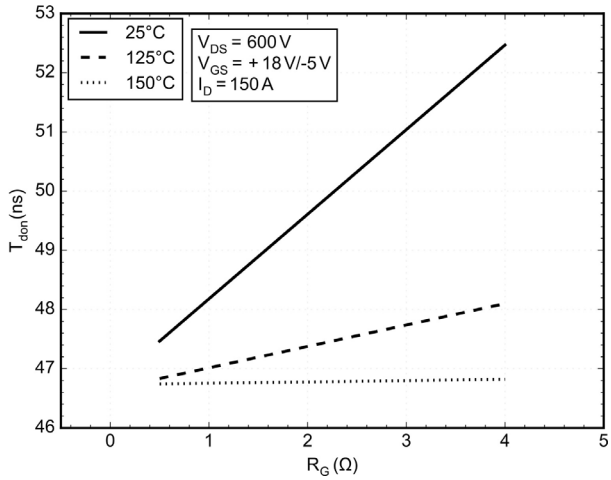



**Figure 13. Typical Switching Loss Tdon vs. Rg**

## TYPICAL CHARACTERISTIC

(M1/M1 SiC MOSFET SWITCHING CHARACTERISTIC)

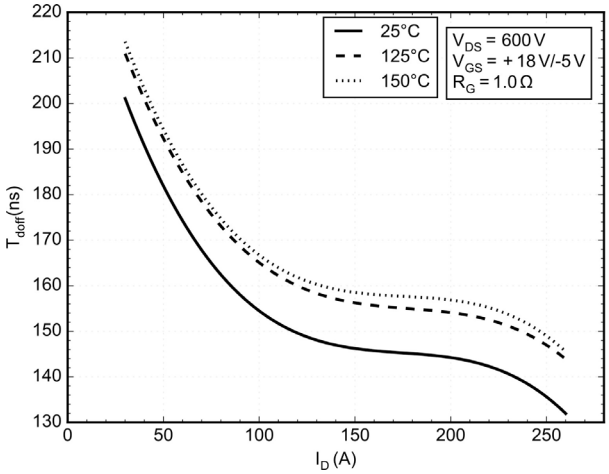



**Figure 14. Typical Switching Loss Tdoff vs. ID**

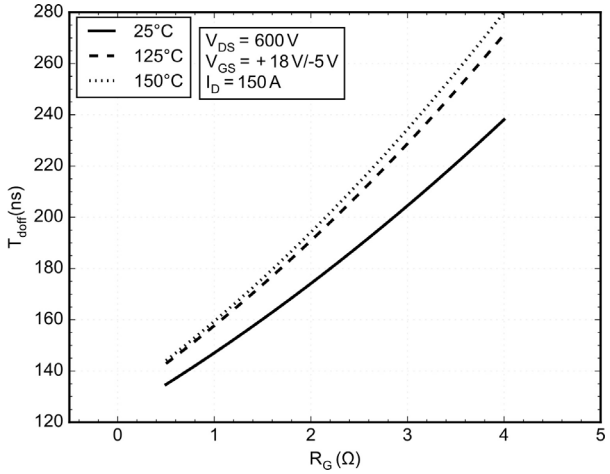



**Figure 15. Typical Switching Loss Tdoff vs. Rg**

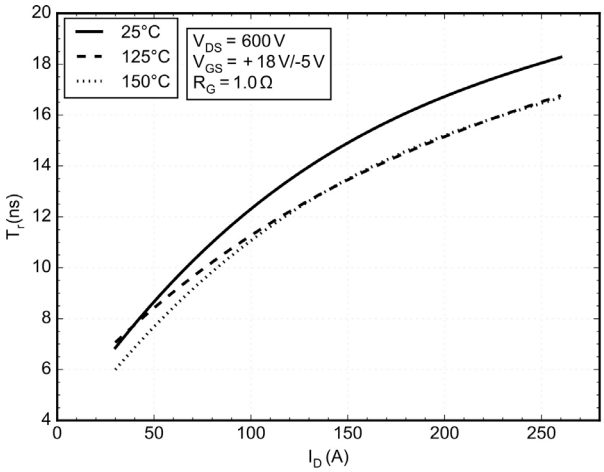



**Figure 16. Typical Switching Loss Tr vs. ID**

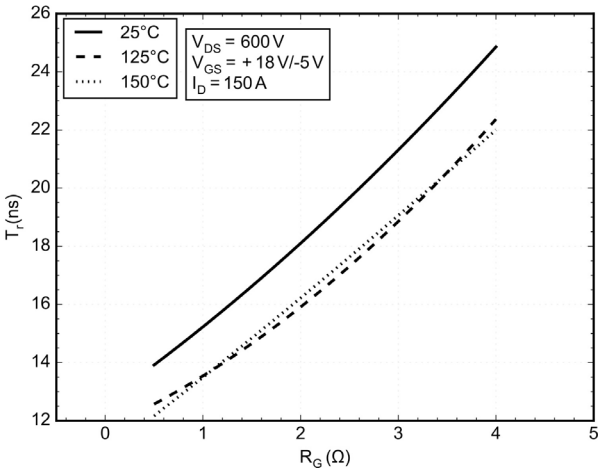



**Figure 17. Typical Switching Loss Tr vs. Rg**

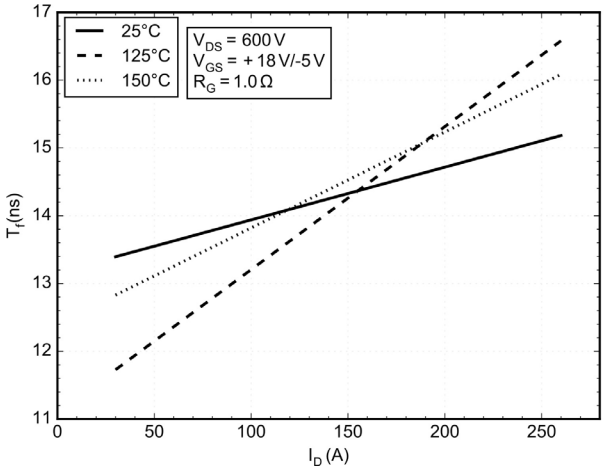



**Figure 18. Typical Switching Loss Tf vs. ID**

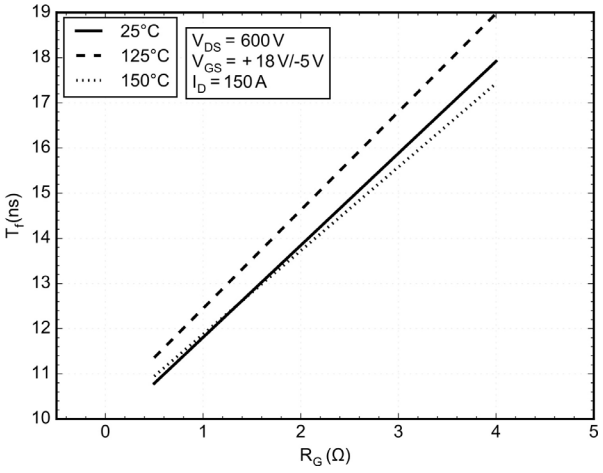



**Figure 19. Typical Switching Loss Tf vs. Rg**

## TYPICAL CHARACTERISTIC

(M1/M1 SiC MOSFET SWITCHING CHARACTERISTIC)

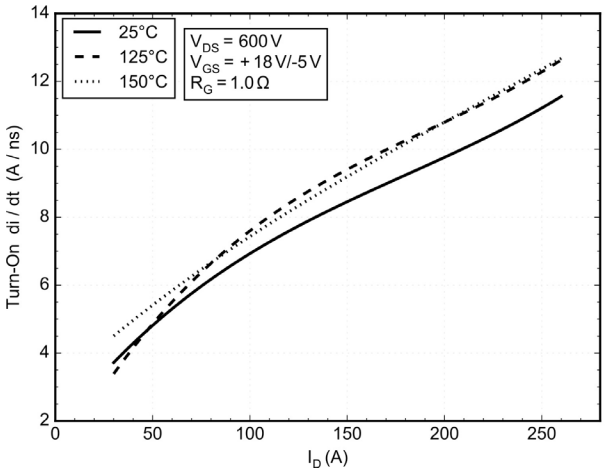



**Figure 20. di/dt ON vs. ID**

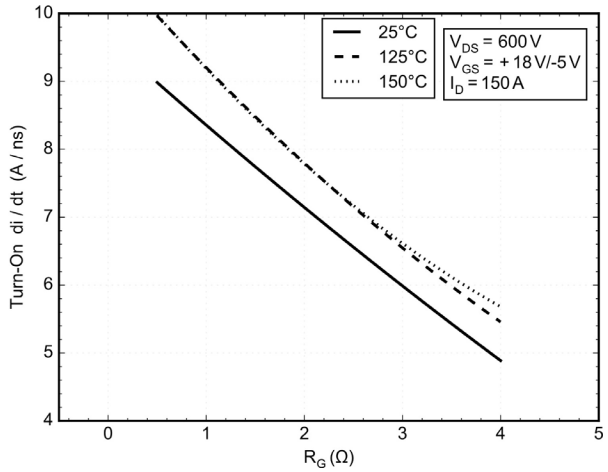



**Figure 21. di/dt ON vs. RG**

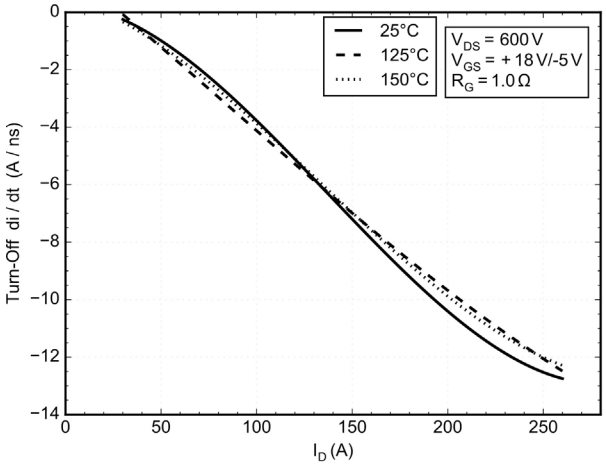



**Figure 22. di/dt OFF vs. ID**

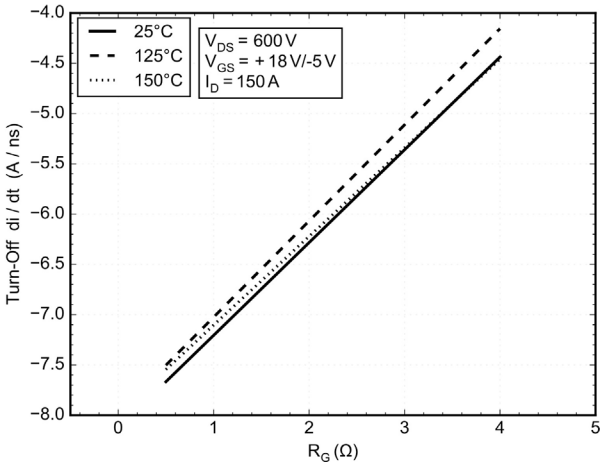



**Figure 23. di/dt OFF vs. RG**

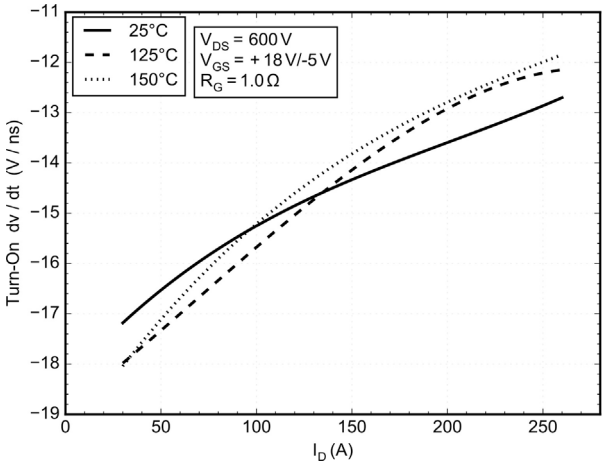



**Figure 24. dv/dt ON vs. ID**

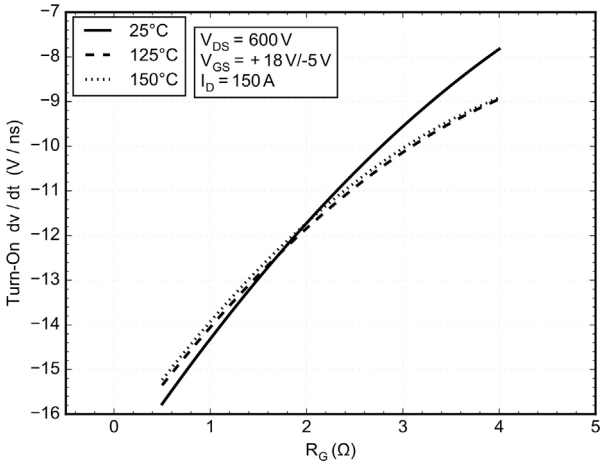



**Figure 25. dv/dt ON vs. RG**

## TYPICAL CHARACTERISTIC

(M1/M1 SiC MOSFET SWITCHING CHARACTERISTIC)

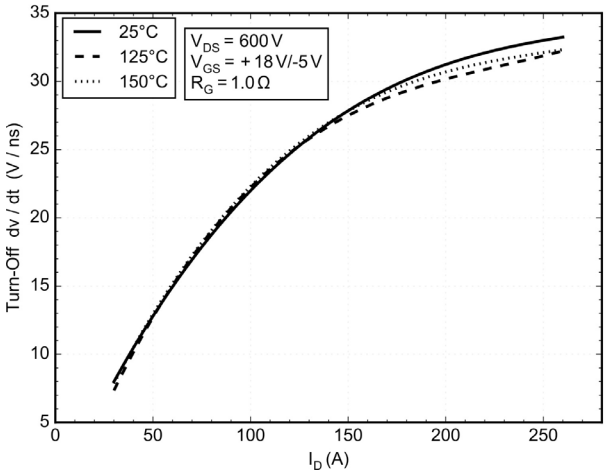



**Figure 26. dv/dt OFF vs. ID**

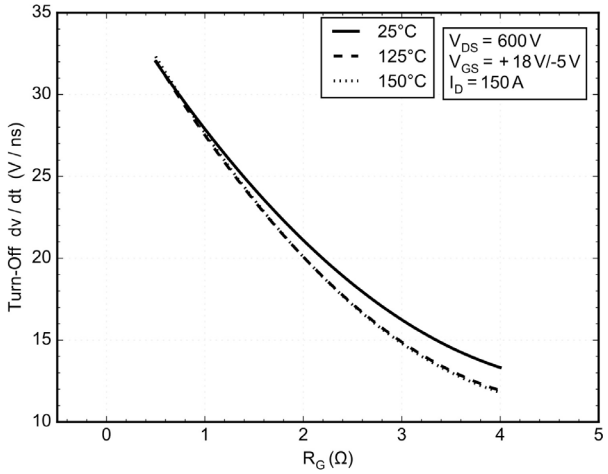



**Figure 27. dv/dt OFF vs. RG**

## TYPICAL CHARACTERISTIC

(M1/M1 SiC MOSFET CHARACTERISTIC)

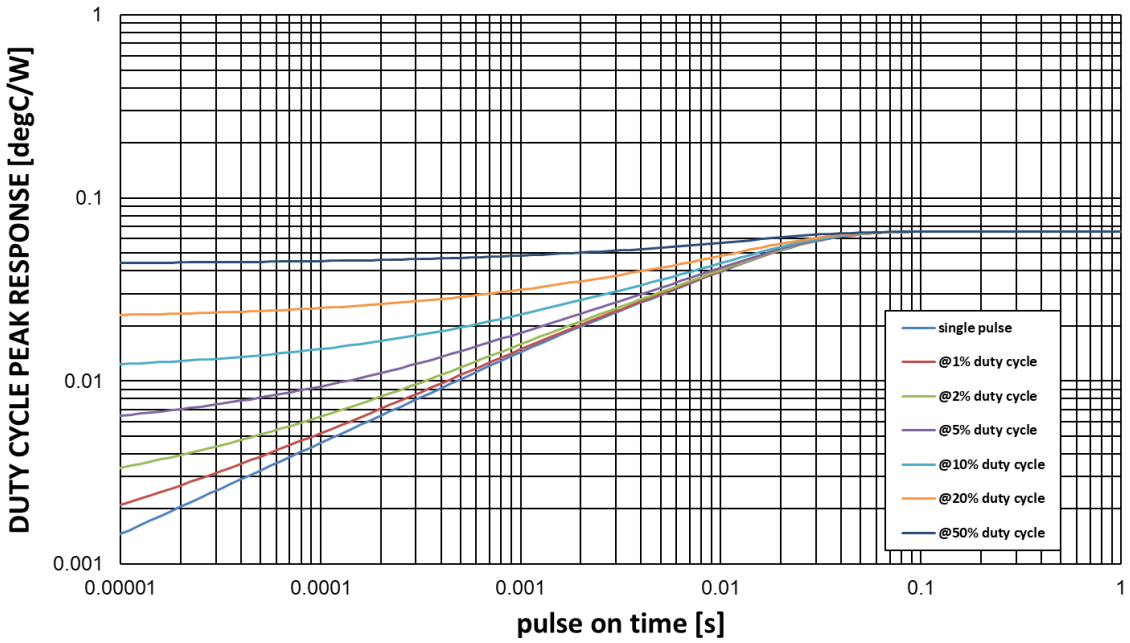



**Figure 28. MOSFET Junction−to−Case Transient Thermal Impedance**

### FOSTER NETWORKS − M1, M2

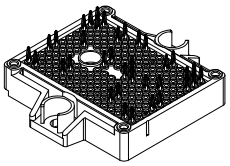
| Foster Element # | M1 | | M2 | |
|---|---|---|---|---|
| | Rth (K/W) | Cth (Ws/K) | Rth (K/W) | Cth (Ws/K) |
| 1 | 0.001954903 | 0.006320060 | 0.002108724 | 0.007173619 |
| 2 | 0.001774431 | 0.052561285 | 0.001674965 | 0.065286128 |
| 3 | 0.008518089 | 0.083667598 | 0.008103839 | 0.093513060 |
| 4 | 0.004782129 | 0.475971634 | 0.005782362 | 0.432951421 |
| 5 | 0.047293860 | 0.316094909 | 0.049861821 | 0.347078551 |

### CAUER NETWORKS − M1, M2

| Cauer Element # | M1 | | M2 | |
|---|---|---|---|---|
| | Rth (K/W) | Cth (Ws/K) | Rth (K/W) | Cth (Ws/K) |
| 1 | 0.002902720 | 0.005142224 | 0.003106026 | 0.005861615 |
| 2 | 0.005574283 | 0.027053480 | 0.005966663 | 0.031491586 |
| 3 | 0.012888434 | 0.041274318 | 0.012576945 | 0.044061233 |
| 4 | 0.022425186 | 0.197068008 | 0.021927720 | 0.198635336 |
| 5 | 0.020532788 | 0.257185833 | 0.023954356 | 0.274582811 |

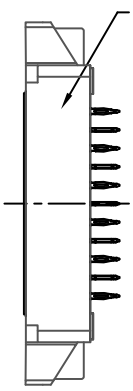
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

ON Semiconductor®

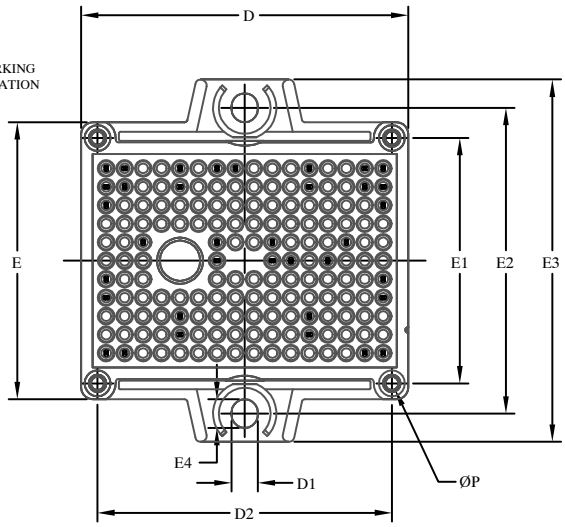


**PIM36 56.7x42.5 (PRESS FIT)**
CASE 180BY
ISSUE C

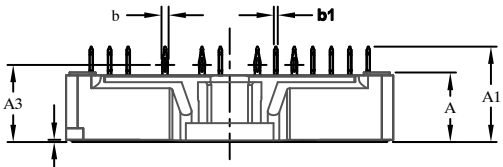
DATE 20 AUG 2021




SIDE VIEW



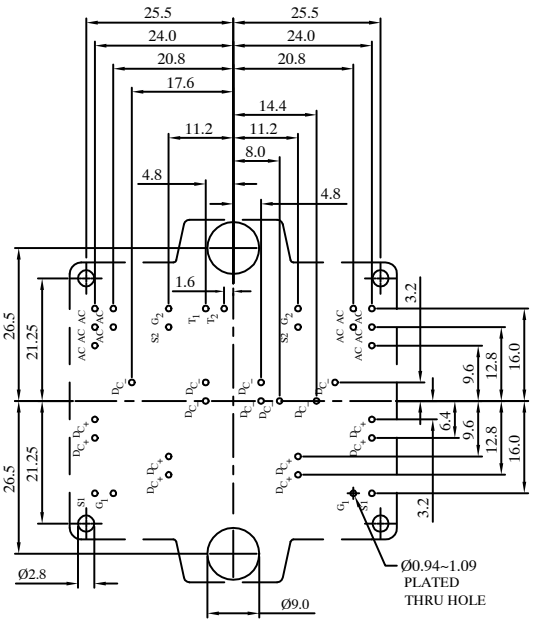

TOP VIEW




END VIEW

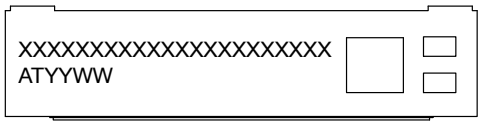
NOTES:
1. CONTROLLING DIMENSION: MILLIMETERS
2. PIN POSITION TOLERANCE IS ± 0.4mm

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN. | NOM. | MAX. |
| A | 11.65 | 12.00 | 12.35 |
| A1 | 16.00 | 16.50 | 17.00 |
| A2 | 0.00 | 0.35 | 0.60 |
| A3 | 12.85 | 13.35 | 13.85 |
| b | 1.15 | 1.20 | 1.25 |
| b1 | 0.59 | 0.64 | 0.69 |
| D | 56.40 | 56.70 | 57.00 |
| D1 | 4.40 | 4.50 | 4.60 |
| D2 | 50.85 | 51.00 | 51.15 |
| E | 47.70 | 48.00 | 48.30 |
| E1 | 42.35 | 42.50 | 42.65 |
| E2 | 52.90 | 53.00 | 53.10 |
| E3 | 62.30 | 62.80 | 63.30 |
| E4 | 4.90 | 5.00 | 5.10 |
| P | 2.20 | 2.30 | 2.40 |

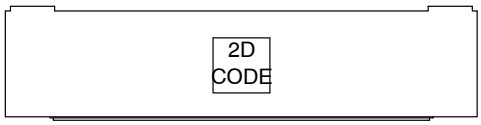



**RECOMMENDED MOUNTING PATTERN**

**GENERIC MARKING DIAGRAM***




FRONTSIDE MARKING




BACKSIDE MARKING

XXXXX = Specific Device Code
AT = Assembly & Test Site Code
YYWW = Year and Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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|---|---|---|
| DESCRIPTION: | PIM36 56.7x42.5 (PRESS FIT) | PAGE 1 OF 1 |

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