

MOSFET – Power, Single, N-Channel

100 V, 40.9 mΩ, 20 A

NVTYS040N10MCL

Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	100	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3)	Steady State	$T_C = 25^\circ\text{C}$	$I_D = 20$ A
		$T_C = 100^\circ\text{C}$	14
Power Dissipation $R_{\theta JC}$ (Notes 1, 2)	Steady State	$T_C = 25^\circ\text{C}$	$P_D = 37$ W
		$T_C = 100^\circ\text{C}$	18
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	$I_D = 6$ A
		$T_A = 100^\circ\text{C}$	4
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	$P_D = 3.1$ W
		$T_A = 100^\circ\text{C}$	1.5
Pulsed Drain Current	$T_C = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM} = 80$	A
Source Current (Body Diode)	I_S	28	A
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 0.9 \text{ A}$)	E_{AS}	1310	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

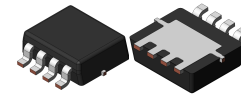
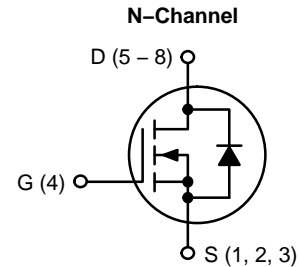
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	4.1	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	48	

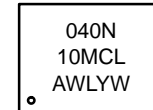
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(on) MAX}$	$I_D MAX$
100 V	40.9 mΩ @ 10 V	20 A
	63.2 mΩ @ 4.5 V	



LFPAK8
3.3x3.3
CASE 760AD

MARKING DIAGRAM



040N10MCL = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVTYS040N10MCL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	100	-	-	V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J		-	66.6	-	mV/°C	
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 100 V	T _J = 25°C	-	-	1.0	μA
			T _J = 125°C	-	-	250	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V	-	-	100	nA	

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 27 μA	1.0	1.6	3.0	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J		-	-6.4	-	mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 5 A	-	28.1	40.9	mΩ
		V _{GS} = 4.5 V, I _D = 5 A	-	37.4	63.2	
Forward Transconductance	g _{FS}	V _{DS} = 5 V, I _D = 5 A	-	18.5	-	S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 50 V	-	564	-	pF
Output Capacitance	C _{OSS}		-	218	-	
Reverse Transfer Capacitance	C _{RSS}		-	4	-	
Gate Resistance	R _G	f = 1 MHz	-	0.6	-	Ω
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 80 V; I _D = 5 A	-	4.1	-	nC
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 80 V; I _D = 5 A	-	8.6	-	
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 10 V, V _{DS} = 80 V; I _D = 5 A	-	0.5	-	nC
Gate-to-Source Charge	Q _{GS}		-	1.6	-	
Gate-to-Drain Charge	Q _{GD}		-	1.2	-	
Plateau Voltage	V _{GP}		-	2.8	-	

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DS} = 80 V, I _D = 5 A, R _G = 6 Ω	-	6.9	-	ns
Rise Time	t _r		-	2.3	-	
Turn-Off Delay Time	t _{d(OFF)}		-	15.7	-	
Fall Time	t _f		-	3.8	-	

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 5 A	T _J = 25°C	-	0.85	1.2	V
			T _J = 125°C	-	0.73	-	
Reverse Recovery Time	t _{RR}	I _F = 5 A, di/dt = 100 A/μs	-	25.5	-	ns	
Charge Time	t _a		-	12.5	-	ns	
Discharge Time	t _b		-	12.6	-	ns	
Reverse Recovery Charge	Q _{RR}		-	14	-	nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

NVTYS040N10MCL

TYPICAL CHARACTERISTICS

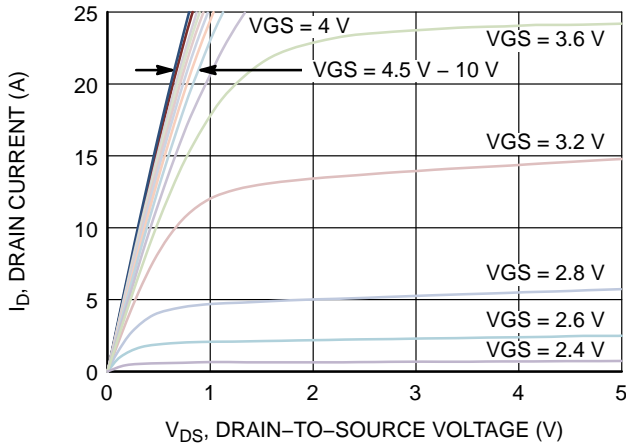


Figure 1. On-Region Characteristics

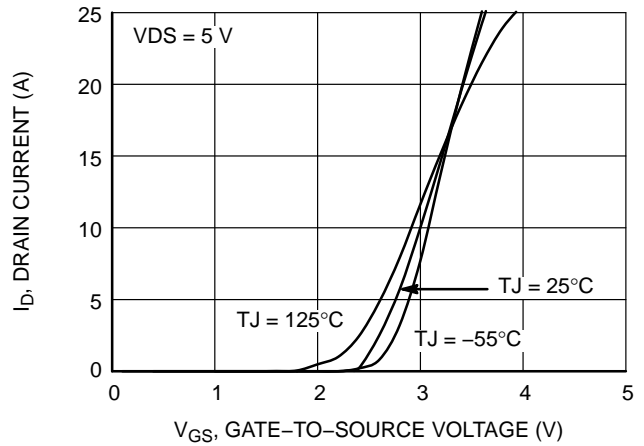


Figure 2. Transfer Characteristics

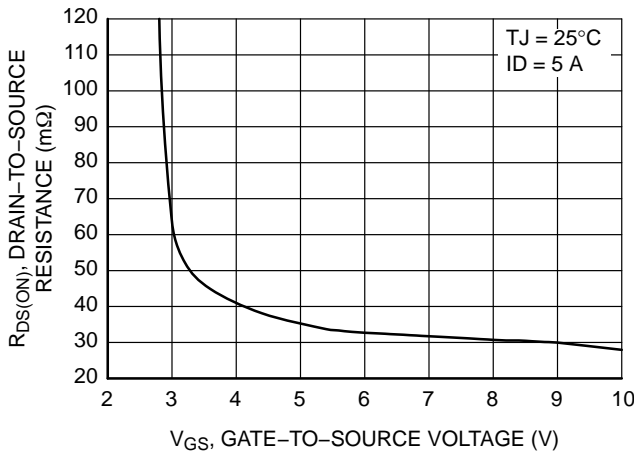


Figure 3. On-Resistance vs. Gate-to-Source Voltage

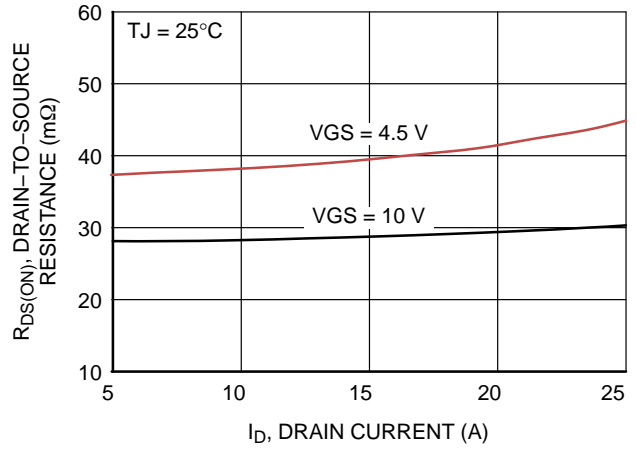


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

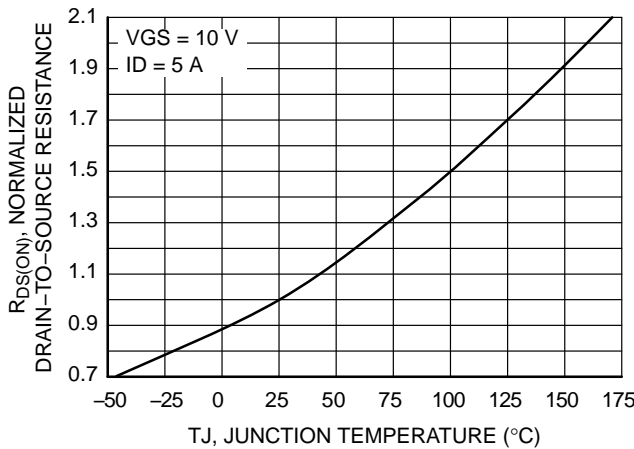


Figure 5. On-Resistance Variation with Temperature

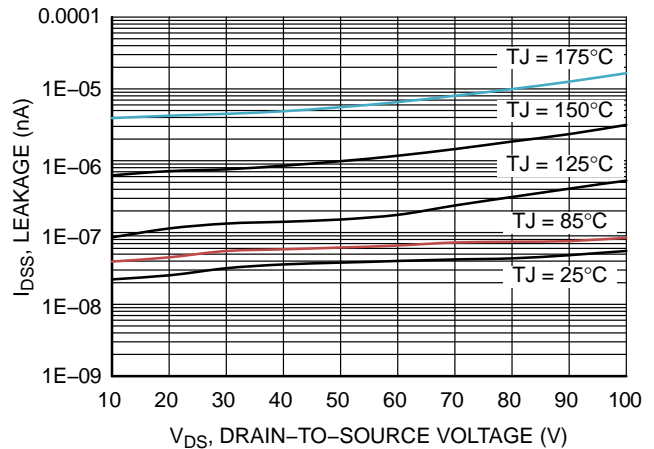


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NVTYS040N10MCL

TYPICAL CHARACTERISTICS

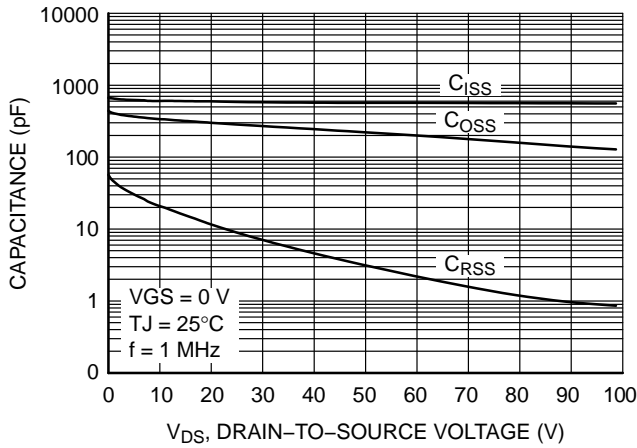


Figure 7. Capacitance Variation

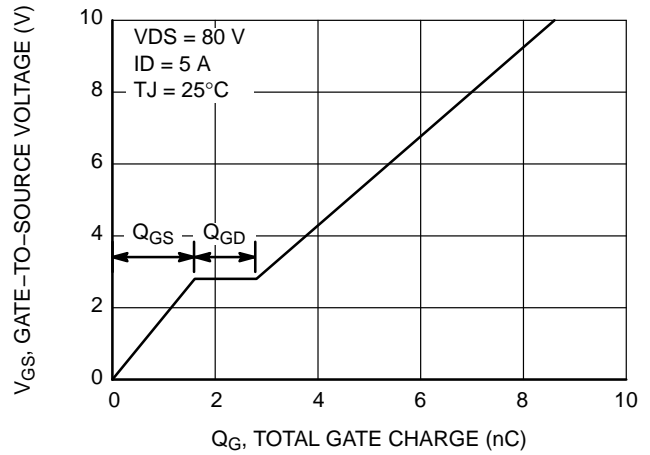


Figure 8. Gate-to-Source vs. Total Charge

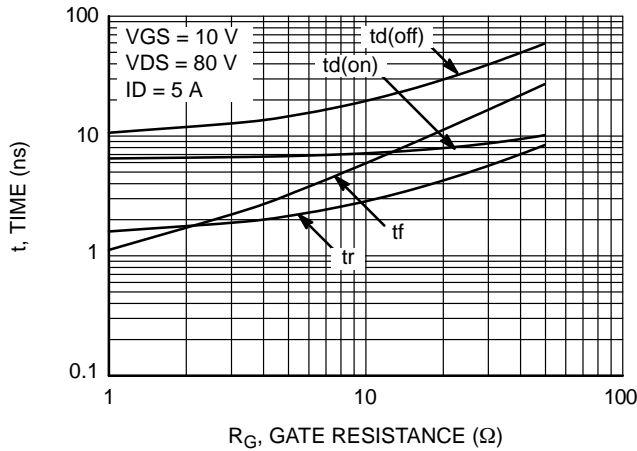


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

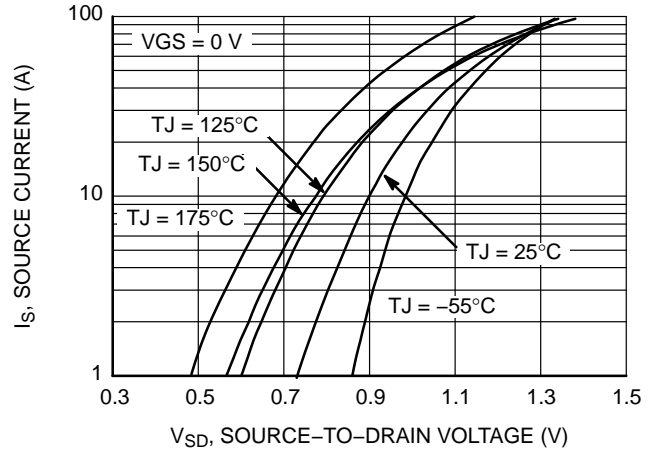


Figure 10. Resistive Switching Time Variation vs. Gate Resistance

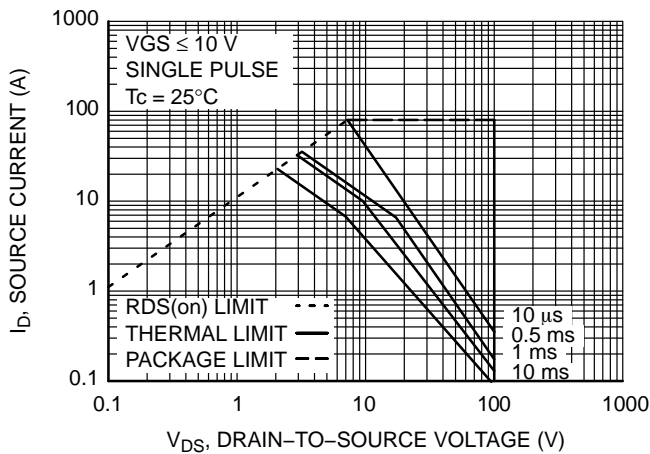


Figure 11. Maximum Rated Forward Biased Safe Operating Area

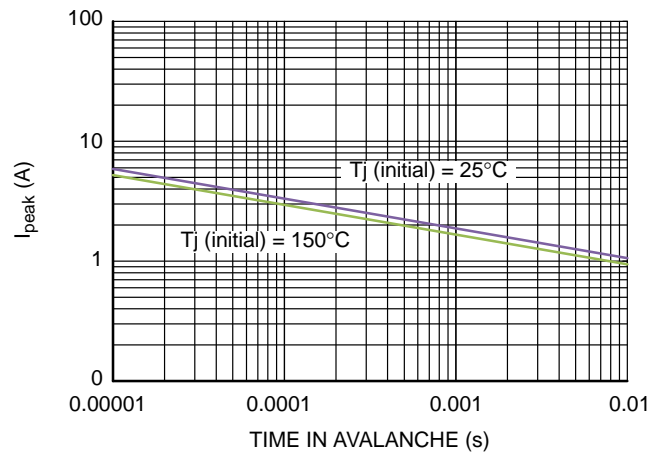


Figure 12. Maximum Drain Current vs. Time in Avalanche

NVTYS040N10MCL

TYPICAL CHARACTERISTICS

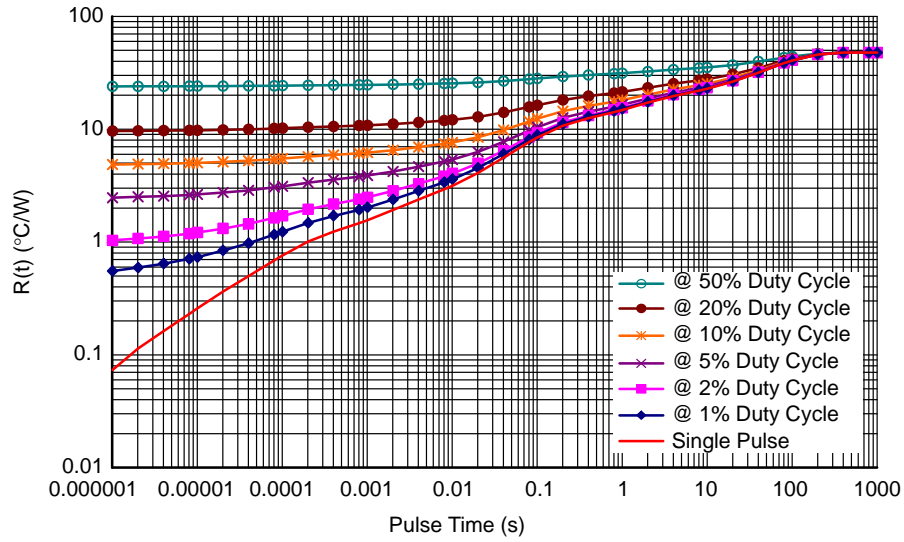


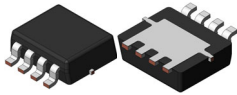
Figure 13. Thermal Response

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVTYS040N10MCLTWG	040N10MCL	LFPAK8 (Pb-Free)	3000 / Tape & Reel

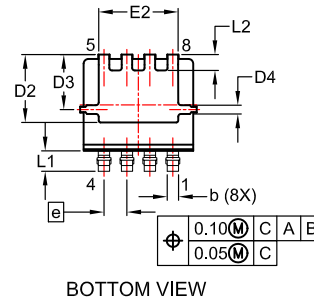
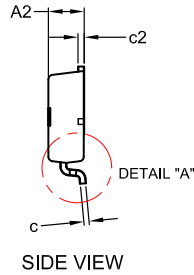
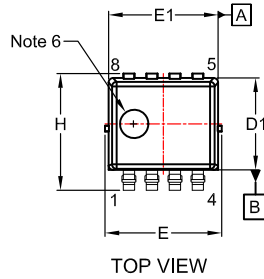
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

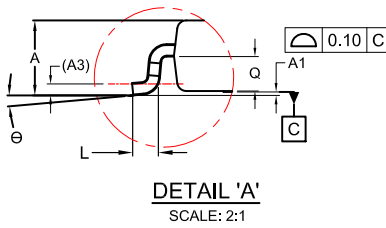


LFPAK8 3.3x3.3, 0.65P CASE 760AD ISSUE E

DATE 16 NOV 2020

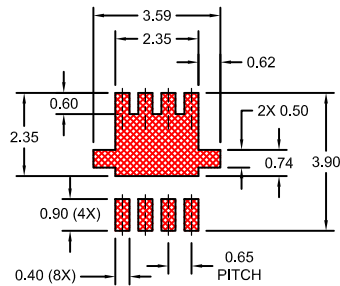


DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.95	1.05	1.15
A1	0.00	0.05	0.10
A2	0.95	1.00	1.05
A3	0.15 REF		
b	0.27	0.32	0.37
c	0.12	0.17	0.22
c2	0.12	0.17	0.22
D1	2.50	2.60	2.70
D2	1.82	1.92	2.02
D3	1.46	1.56	1.66
D4	0.20	0.25	0.30
E	3.20	3.30	3.40
E1	3.00	3.10	3.20
E2	2.15	2.25	2.35
e	0.65 BSC		
H	3.20	3.30	3.40
L	0.25	0.37	0.50
L1	0.48	0.58	0.68
L2	0.35	0.45	0.55
Q	0.45	0.50	0.55
θ	0°	4°	8°



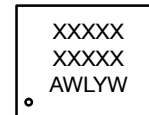
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS OR BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
6. OPTIONAL MOLD FEATURE.



*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "μ", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON05544H	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	LFPAK8 3.3x3.3, 0.65P	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative