# **MOSFET** - Power, Single

## **N-Channel**

40 V, 4.9 mΩ, 78 A

### **NVTYS004N04C**

#### **Features**

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

| Parameter   |                     |                            | Symbol                            | Value          | Unit |
|---|---------------------|----------------------------|-----------------------------------|----------------|------|
| Drain-to-Source Voltage   |                     |                            | $V_{DSS}$                         | 40             | V    |
| Gate-to-Source Voltage  | 9                   |                            | V <sub>GS</sub>                   | ±20            | V    |
| Continuous Drain  | Steady              | T <sub>C</sub> = 25°C      | I <sub>D</sub>                    | 78             | Α    |
| Current R <sub>θJC</sub> (Notes 1, 2, 3, 4)                                   |                     | T <sub>C</sub> = 100°C     |                                   | 55             |      |
| Power Dissipation   | State               | T <sub>C</sub> = 25°C      | $P_{D}$                           | 55             | W    |
| R <sub>θJC</sub> (Notes 1, 2, 3)  |                     | T <sub>C</sub> = 100°C     |                                   | 27             |      |
| Continuous Drain  |                     | T <sub>A</sub> = 25°C      | I <sub>D</sub>                    | 19             | Α    |
| Current R <sub>0JA</sub> (Notes 1, 3, 4)                                      | Steady              | T <sub>A</sub> = 100°C     |                                   | 13             |      |
| Power Dissipation   |                     |                            |                                   | 3.2            | W    |
| $R_{\theta JA}$ (Notes 1, 3)  |                     | T <sub>A</sub> = 100°C     |                                   | 1.6            |      |
| Pulsed Drain Current  | T <sub>A</sub> = 25 | °C, t <sub>p</sub> = 10 μs | I <sub>DM</sub>                   | 343            | Α    |
| Operating Junction and Storage Temperature Range                              |                     |                            | T <sub>J</sub> , T <sub>stg</sub> | -55 to<br>+175 | °C   |
| Source Current (Body Diode)   |                     |                            | Is                                | 46             | Α    |
| Single Pulse Drain-to-Source Avalanche<br>Energy (I <sub>L(pk)</sub> = 5.2 A) |                     |                            | E <sub>AS</sub>                   | 171            | mJ   |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s)             |                     |                            | TL                                | 260            | °C   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

| Parameter                                   | Symbol          | Value | Unit |
|---|-----------------|-------|------|
| Junction-to-Case - Steady State (Note 3)    | $R_{\theta JC}$ | 2.7   | °C/W |
| Junction-to-Ambient - Steady State (Note 3) | $R_{\theta JA}$ | 47.4  |      |

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- Psi (Ψ) is used as required per JESD51–12 for packages in which substantially less than 100% of the heat flows to single case surface.
- 3. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
- Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

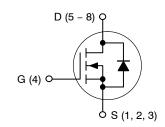


#### ON Semiconductor®

#### www.onsemi.com

| • | V <sub>(BR)DSS</sub> | R <sub>DS(on)</sub> MAX | I <sub>D</sub> MAX |
|---|----------------------|-------------------------|--------------------|
|   | 40 V                 | 4.9 m $\Omega$ @ 10 V   | 78 A               |

#### N-Channel





LFPAK8 3.3x3.3 CASE 760AD

#### MARKING DIAGRAM

004N 04C AWLYW

004N04C = Specific Device Code

A = Assembly Location

WL = Wafer Lot Y = Year W = Work Week

(Note: Microdot may be in either location)

#### **ORDERING INFORMATION**

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

### **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise noted)

| Parameter                         | Symbol               | Test Condition  |   | Min | Тур  | Max | Unit |
|-----------------------------------|----------------------|---|---|-----|------|-----|------|
| OFF CHARACTERISTICS               | -                    | -   |   |     | -    | -   | -    |
| Drain-to-Source Breakdown Voltage | V <sub>(BR)DSS</sub> | $V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$                                   |   | 40  |      |     | V    |
| Zero Gate Voltage Drain Current   | I <sub>DSS</sub>     | VGS = 0 V,  | T <sub>J</sub> = 25°C   |     |      | 10  | μΑ   |
|                                   |                      |   | T <sub>J</sub> = 125°C  |     |      | 250 | 1    |
| Gate-to-Source Leakage Current    | I <sub>GSS</sub>     | $V_{DS} = 0 V, V_{G}$   | <sub>S</sub> = 20 V   |     |      | 100 | nA   |
| ON CHARACTERISTICS (Note 5)       |                      |   |   |     |      |     |      |
| Gate Threshold Voltage            | V <sub>GS(TH)</sub>  | $V_{GS} = V_{DS}, I_{D}$  | = 50 μΑ   | 2.5 |      | 3.5 | V    |
| Drain-to-Source On Resistance     | R <sub>DS(on)</sub>  | V <sub>GS</sub> = 10 V, I <sub>E</sub>  | <sub>0</sub> = 20 A   |     | 4.1  | 4.0 | mΩ   |
| Forward Transconductance          | 9FS                  | $V_{DS} = 5 \text{ V}, I_{D}$   | = 35 A  |     | 70   |     | S    |
| CHARGES AND CAPACITANCES          |                      |   |   |     |      |     |      |
| Input Capacitance                 | C <sub>iss</sub>     | V <sub>GS</sub> = 0 V, f =  | 1.0 MHz,  |     | 1210 |     | pF   |
| Output Capacitance                | C <sub>oss</sub>     | V <sub>DS</sub> = 25  | o V   |     | 590  |     | 1    |
| Reverse Transfer Capacitance      | C <sub>rss</sub>     |   |   |     | 21   |     | 1    |
| Threshold Gate Charge             | Q <sub>G(TH)</sub>   |   | V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 32 V, I <sub>D</sub> = 35 A |     | 3.2  |     | nC   |
| Gate-to-Source Charge             | $Q_{GS}$             | V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 3                                     |   |     | 5.7  |     | 1    |
| Gate-to-Drain Charge              | $Q_{GD}$             |   |   |     | 4.3  |     | 1    |
| Total Gate Charge                 | Q <sub>G(TOT)</sub>  | V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 32 V, I <sub>D</sub> = 35 A           |   |     | 19   |     | nC   |
| SWITCHING CHARACTERISTICS (No     | te 6)                |   |   |     | •    | •   |      |
| Turn-On Delay Time                | t <sub>d(on)</sub>   |   |   |     | 9.9  |     | ns   |
| Rise Time                         | t <sub>r</sub>       | V <sub>GS</sub> = 10 V, V <sub>D</sub>  | s = 32 V.   |     | 3.6  |     |      |
| Turn-Off Delay Time               | t <sub>d(off)</sub>  | $I_D = 35  A,  R_C$   | 3 = 1 Ω   |     | 14   |     |      |
| Fall Time                         | t <sub>f</sub>       |   |   |     | 6    |     | 1    |
| DRAIN-SOURCE DIODE CHARACTEF      | RISTICS              |   |   |     |      |     |      |
| Forward Diode Voltage             | $V_{SD}$             | V <sub>GS</sub> = 0 V,<br>I <sub>S</sub> = 35 A                                 | T <sub>J</sub> = 25°C   |     | 0.86 | 1.2 | V    |
|                                   |                      |   | T <sub>J</sub> = 125°C  |     | 0.75 |     | 1    |
| Reverse Recovery Time             | t <sub>RR</sub>      | V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs,<br>I <sub>S</sub> = 35 A |   |     | 33   |     | ns   |
| Charge Time                       | t <sub>a</sub>       |   |   |     | 12   |     |      |
| Discharge Time                    | t <sub>b</sub>       |   |   |     | 21   |     |      |
| Reverse Recovery Charge           | Q <sub>RR</sub>      |   |   |     | 13   |     | nC   |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

#### **TYPICAL CHARACTERISTICS**

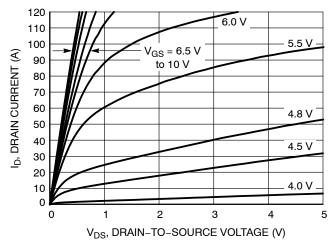


Figure 1. On-Region Characteristics

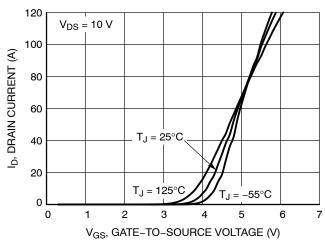


Figure 2. Transfer Characteristics

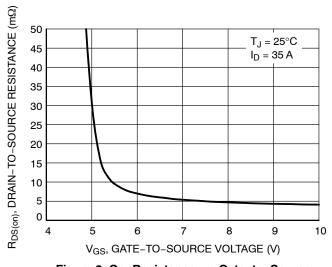


Figure 3. On-Resistance vs. Gate-to-Source Voltage

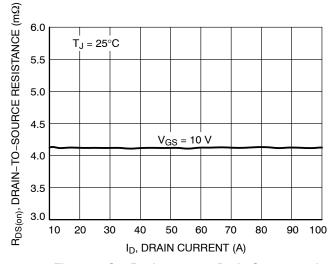


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

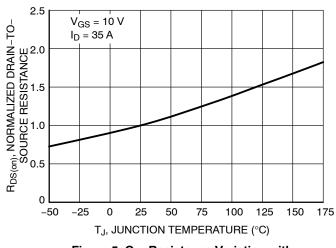


Figure 5. On–Resistance Variation with Temperature

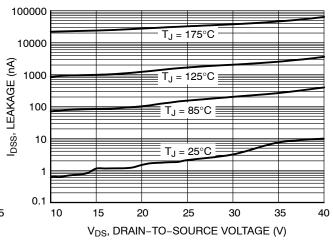
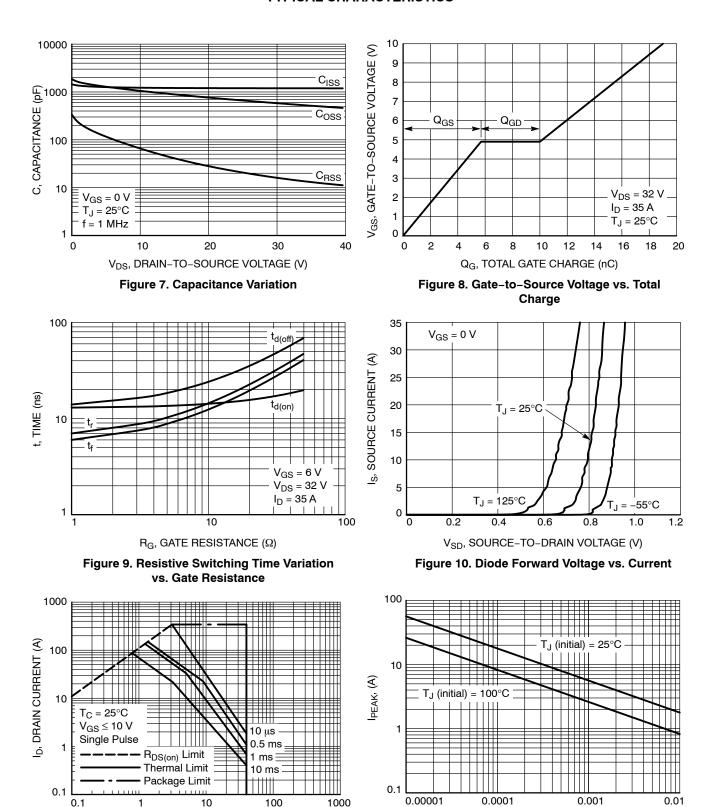


Figure 6. Drain-to-Source Leakage Current vs. Voltage

#### **TYPICAL CHARACTERISTICS**



V<sub>DS</sub>, DRAIN-TO-SOURCE VOLTAGE (V) Figure 11. Safe Operating Area

100

TIME IN AVALANCHE (s) Figure 12. I<sub>PEAK</sub> vs. Time in Avalanche

1000

#### **TYPICAL CHARACTERISTICS**

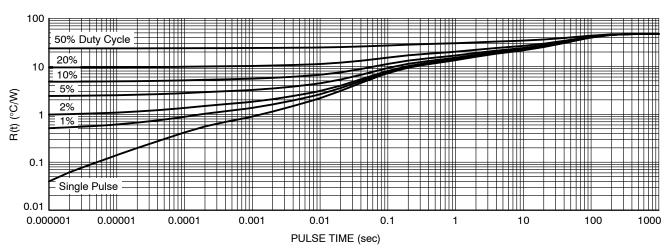


Figure 13. Thermal Characteristics

#### **DEVICE ORDERING INFORMATION**

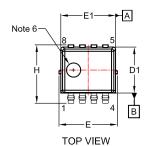
| Device          | Marking     | Package              | Shipping <sup>†</sup> |
|-----------------|-------------|----------------------|-----------------------|
| NVTYS004N04CTWG | 004N<br>04C | LFPAK33<br>(Pb-Free) | 3000 / Tape & Reel    |

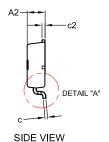
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

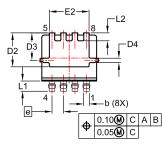
#### PACKAGE DIMENSIONS

### LFPAK8 3.3x3.3, 0.65P

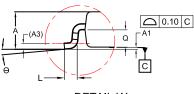
CASE 760AD ISSUE E



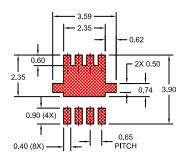




**BOTTOM VIEW** 



DETAIL 'A' SCALE: 2:1



# LAND PATTERN RECOMMENDATION

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS OR BURRS SHALL NOT EXCEED 0,150mm PER SIDE,
- 4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
- 6. OPTIONAL MOLD FEATURE.

| DIM   | MILLIMETERS |             |      |  |
|-------|-------------|-------------|------|--|
| Silvi | MIN.        | MIN. NOM. M |      |  |
| Α     | 0.95        | 1.05        | 1.15 |  |
| A1    | 0.00        | 0.05        | 0.10 |  |
| A2    | 0.95        | 1.00        | 1.05 |  |
| A3    |             | 0.15 RE     | F    |  |
| b     | 0.27        | 0.32        | 0.37 |  |
| С     | 0.12        | 0.17        | 0.22 |  |
| c2    | 0.12        | 0.17        | 0.22 |  |
| D1    | 2.50        | 2.60        | 2.70 |  |
| D2    | 1.82        | 1.92        | 2.02 |  |
| D3    | 1.46        | 1.56        | 1.66 |  |
| D4    | 0.20        | 0.25        | 0.30 |  |
| Е     | 3.20        | 3.30        | 3.40 |  |
| E1    | 3.00        | 3.10        | 3.20 |  |
| E2    | 2.15        | 2.25        | 2.35 |  |
| е     | 0.65 BSC    |             |      |  |
| Н     | 3.20        | 3.30        | 3.40 |  |
| L     | 0.25        | 0.37        | 0.50 |  |
| L1    | 0.48        | 0.58        | 0.68 |  |
| L2    | 0.35        | 0.45        | 0.55 |  |
| Ŋ     | 0.45        | 0.50        | 0.55 |  |
| Φ     | 0°          | 4°          | 8°   |  |
|       |             |             |      |  |

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