

# MOSFET – Power, Single, N-Channel

## 30 V, 98 A



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## NVTYS003N03CL

### Features

- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

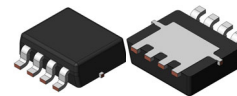
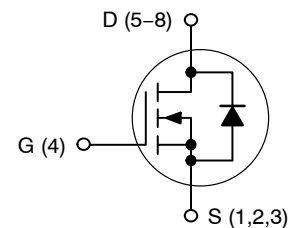
Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DSS}$	30	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current $R_{\theta JA}$ (Note 1)	$I_D$	$T_A = 25^\circ\text{C}$	23	A
		$T_A = 100^\circ\text{C}$	16	
Power Dissipation $R_{\theta JA}$ (Note 1)	$P_D$	$T_A = 25^\circ\text{C}$	3	W
		$T_A = 100^\circ\text{C}$	2	
Continuous Drain Current $R_{\theta JC}$ (Note 1)	$I_D$	$T_C = 25^\circ\text{C}$	98	A
		$T_C = 100^\circ\text{C}$	70	
Power Dissipation $R_{\theta JC}$ (Note 1)	$P_D$	$T_C = 25^\circ\text{C}$	59	W
		$T_C = 100^\circ\text{C}$	30	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$	446	A
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)	$I_S$	50	A	
Single Pulse Drain-to-Source Avalanche Energy ( $I_L = 7.4 \text{ A}_{pk}$ )	$E_{AS}$	173	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
30 V	3.6 m $\Omega$ @ 10 V	98 A
	5.1 m $\Omega$ @ 4.5 V	

### N-Channel MOSFET



**LFPAK8**  
3.3x3.3  
CASE 760AD

### MARKING DIAGRAM

003N 03CL AWLYW
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003N03CL = Specific Device Code  
 A = Assembly Location  
 WL = Wafer Lot  
 Y = Year  
 W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping†
NVTYS003N03CLTWG	LFPAK33 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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## THEMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	2.5	°C/W
Junction-to-Ambient – Steady State	$R_{\theta JA}$	47.2	

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
- Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			19		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.3		2.2	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-5.46		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$		2.7	3.6	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 30\text{ A}$		4	5.1	
Forward Transconductance	$g_{FS}$	$V_{DS} = 1.5\text{ V}, I_D = 15\text{ A}$		64		S
Gate Resistance	$R_G$	$T_A = 25^\circ\text{C}$		0.8		$\Omega$

### CHARGES AND CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 15\text{ V}$		1870		pF
Output Capacitance	$C_{OSS}$			983		
Reverse Transfer Capacitance	$C_{RSS}$			30		
Capacitance Ratio	$C_{RSS}/C_{ISS}$	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}, f = 1\text{ MHz}$		0.016		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$		12		nC
Threshold Gate Charge	$Q_{G(TH)}$			2.5		
Gate-to-Source Charge	$Q_{GS}$			5		
Gate-to-Drain Charge	$Q_{GD}$			2		
Gate Plateau Voltage	$V_{GP}$			2.5		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$		26		nC

### SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		15		ns
Rise Time	$t_r$			7		
Turn-Off Delay Time	$t_{d(OFF)}$			20		
Fall Time	$t_f$			7		

- Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Switching characteristics are independent of operating junction temperatures.

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## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>SWITCHING CHARACTERISTICS</b> (Note 6)						
Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A, R <sub>G</sub> = 3.0 Ω		10		ns
Rise Time	t <sub>r</sub>			3		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			27		
Fall Time	t <sub>f</sub>			4		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 30 A	T <sub>J</sub> = 25°C		0.82	1.1	V
			T <sub>J</sub> = 125°C		0.69		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 30 A		39		ns	
Charge Time	t <sub>a</sub>			16.5			
Discharge Time	t <sub>b</sub>			17.6			
Reverse Recovery Charge	Q <sub>RR</sub>			17		nC	

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

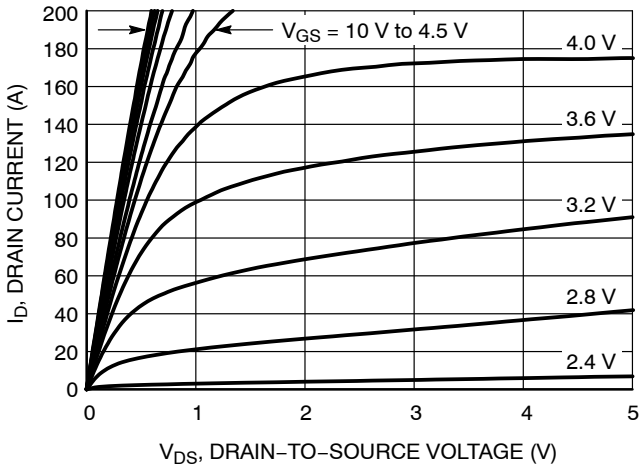


Figure 1. On-Region Characteristics

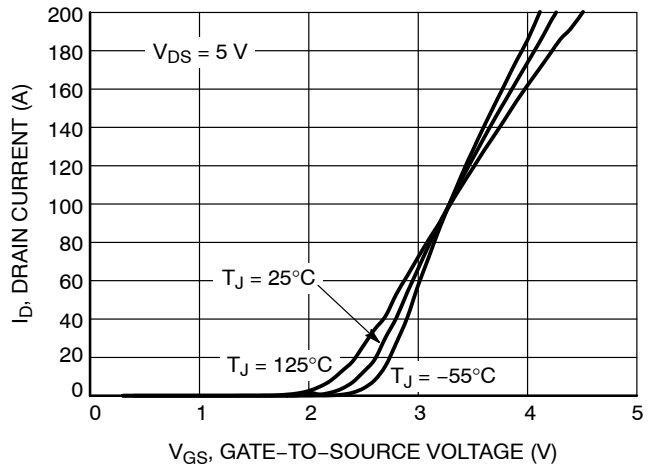


Figure 2. Transfer Characteristics

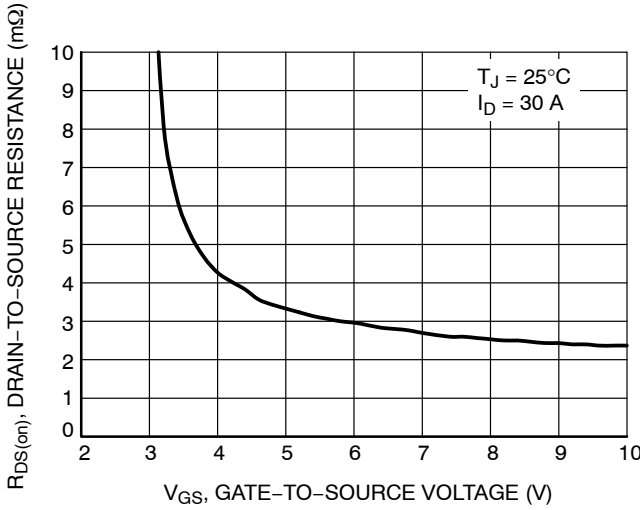


Figure 3. On-Resistance vs. Gate-to-Source Voltage

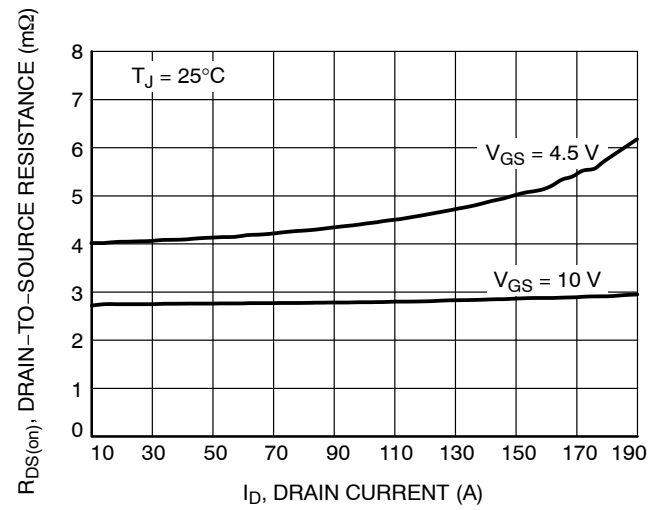


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

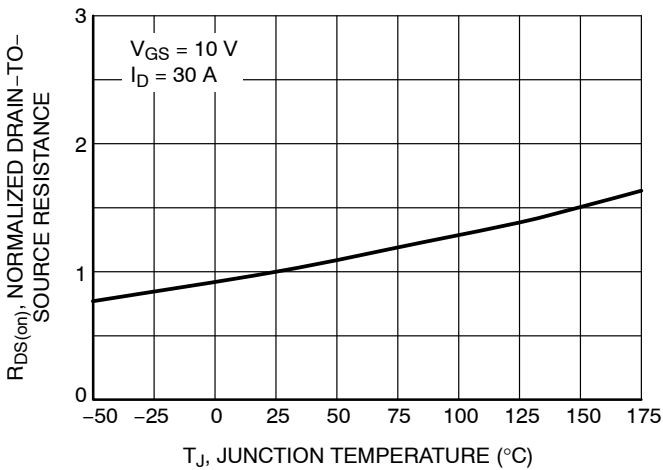


Figure 5. On-Resistance Variation with Temperature

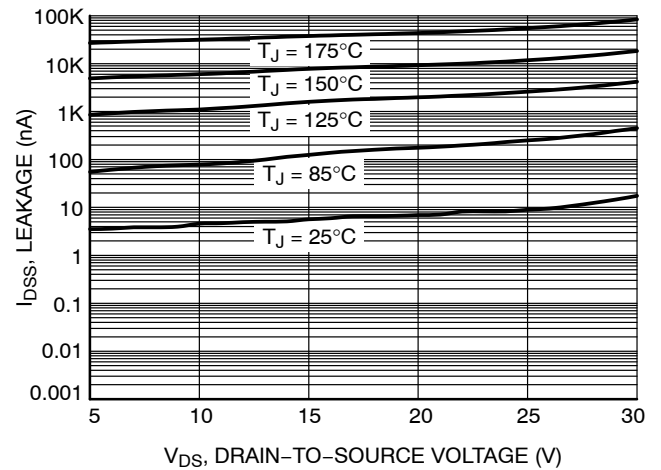


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

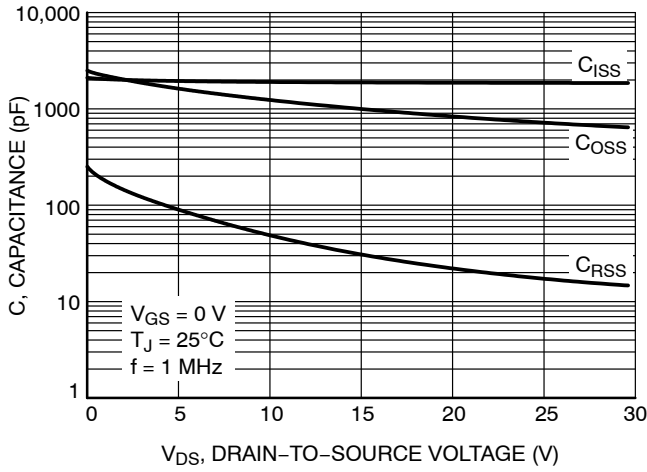


Figure 7. Capacitance Variation

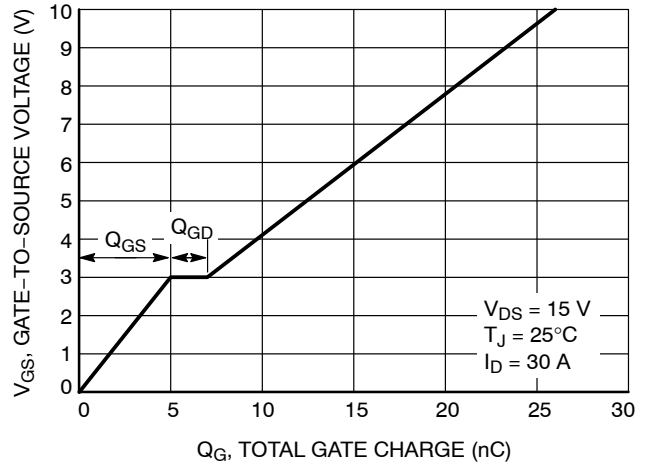


Figure 8. Gate-to-Source Voltage vs. Total Charge

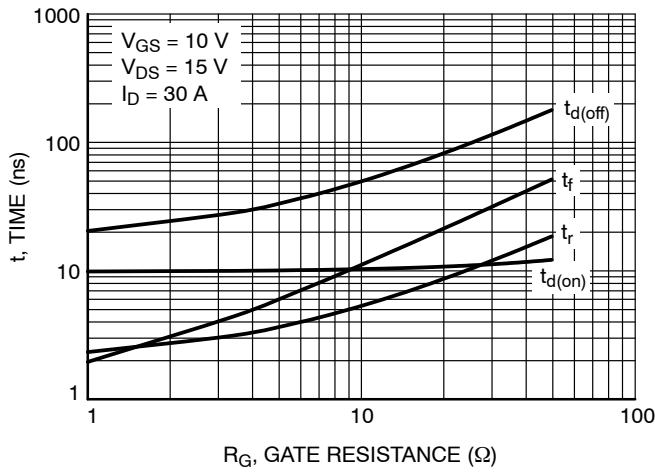


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

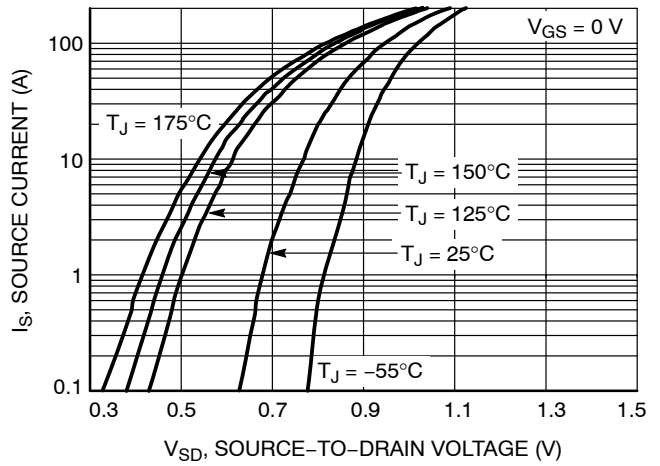


Figure 10. Diode Forward Voltage vs. Current

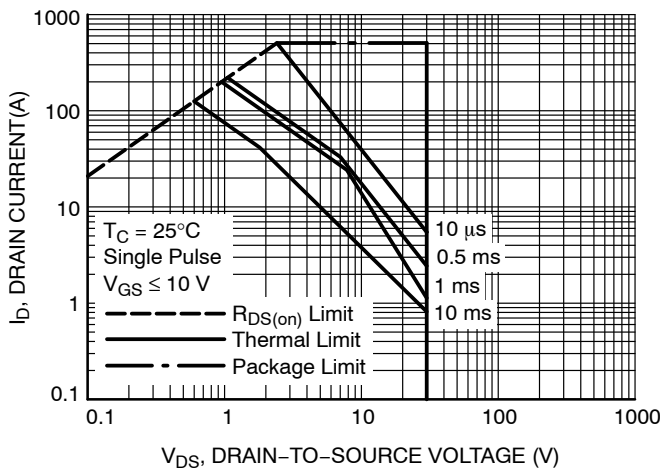


Figure 11. Maximum Rated Forward Biased Safe Operating Area

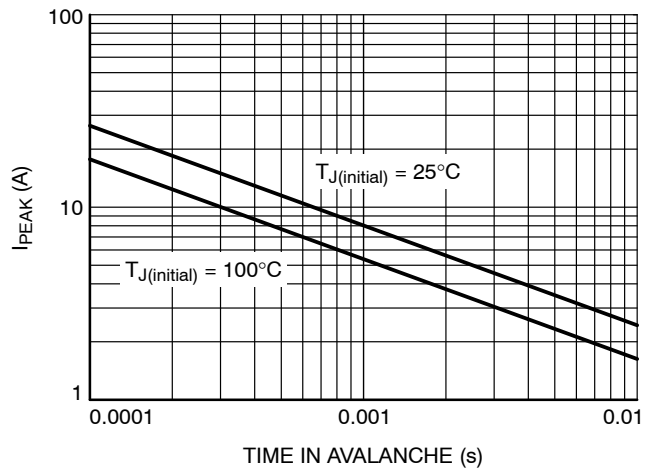


Figure 12. IPEAK vs. Time in Avalanche

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## TYPICAL CHARACTERISTICS

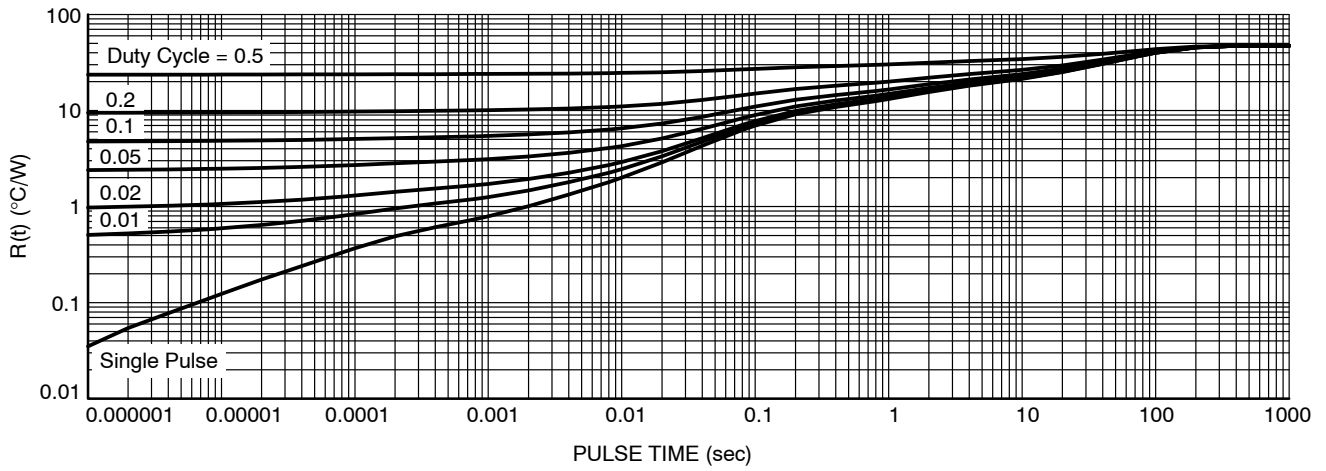
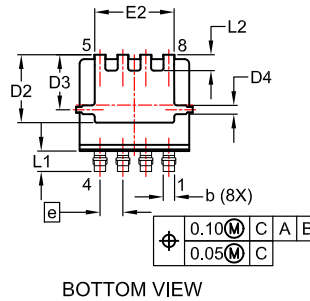
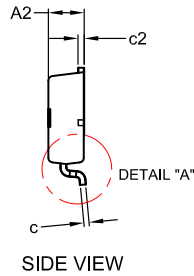
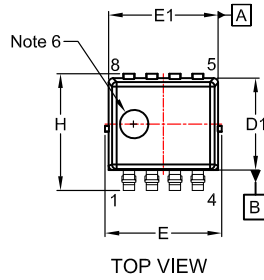


Figure 13. Thermal Characteristics

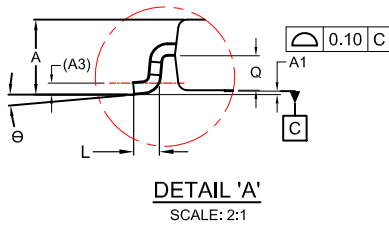
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## PACKAGE DIMENSIONS

### LFPAK8 3.3x3.3, 0.65P CASE 760AD ISSUE E

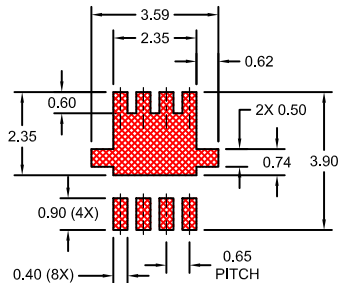


DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.95	1.05	1.15
A1	0.00	0.05	0.10
A2	0.95	1.00	1.05
A3	0.15 REF		
b	0.27	0.32	0.37
c	0.12	0.17	0.22
c2	0.12	0.17	0.22
D1	2.50	2.60	2.70
D2	1.82	1.92	2.02
D3	1.46	1.56	1.66
D4	0.20	0.25	0.30
E	3.20	3.30	3.40
E1	3.00	3.10	3.20
E2	2.15	2.25	2.35
e	0.65 BSC		
H	3.20	3.30	3.40
L	0.25	0.37	0.50
L1	0.48	0.58	0.68
L2	0.35	0.45	0.55
Q	0.45	0.50	0.55
θ	0°	4°	8°



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS OR BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
6. OPTIONAL MOLD FEATURE.



\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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