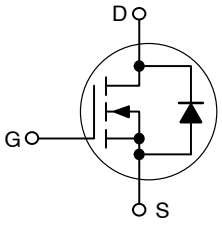
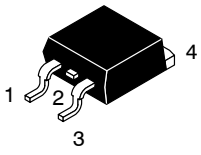
# MOSFET - N-Channel SuperFET® V, FRFET®
## 600 V, 55 mΩ, 45 A

# NVB055N60S5F

| $V_{(BR)DSS}$ | $R_{DS(on)}$ TYP | $I_D$ MAX |
|---|---|---|
| 600 V | 55 mΩ @ $V_{GS}$ = 10 V | 45 A |

**N−CHANNEL MOSFET**




**D²PAK**
**CASE 418AJ**

### Features

- Ultra Low Gate Charge & Low Effective Output Capacitance
- Lower FOM ($R_{DS(on)\ max.}$ x $Q_{g\ typ.}$ & $R_{DS(on)\ max.}$ x $E_{OSS}$)
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

### MAXIMUM RATINGS ($T_J$ = 25°C unless otherwise noted)

| Parameter | | Symbol | Value | Unit |
|---|---|---|---|---|
| Drain−to−Source Voltage | | $V_{DSS}$ | 600 | V |
| Gate−to−Source Voltage | DC | $V_{GS}$ | ±30 | V |
| | AC (f > 1 Hz) | | ±30 | |
| Continuous Drain Current | $T_C$ = 25°C | $I_D$ | 45 | A |
| | $T_C$ = 100°C | | 28 | |
| Power Dissipation | $T_C$ = 25°C | $P_D$ | 275 | W |
| Pulsed Drain Current | $T_C$ = 25°C, $t_P$ = 10 μs | $I_{DM}$ | 159 | A |
| Pulsed Source Current (Body Diode) | | $I_{SM}$ | 159 | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | −55 to +150 | °C |
| Source Current (Body Diode) | | $I_S$ | 45 | A |
| Single Pulse Avalanche Energy | ($I_L$ = 7 A, $R_G$ = 25 Ω) | $E_{AS}$ | 417 | mJ |
| Avalanche Current | | $I_{AS}$ | 7 | A |
| Repetitive Avalanche Energy (Note 1) | | $E_{AR}$ | 2.78 | mJ |
| MOSFET dv/dt | | dvdt | 120 | V/ns |
| Peak Diode Recovery dv/dt (Note 2) | | | 70 | |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | | $T_L$ | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

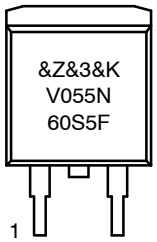
1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. $I_{SD}$ ≤ 22.5 A, di/dt ≤ 200 A/μs, $V_{DD}$ ≤ 400 V, starting $T_J$ = 25°C.

### THERMAL RESISTANCE

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance, Junction−to−Case (Notes 3, 4) | $R_{\theta JC}$ | 0.45 | °C/W |
| Thermal Resistance, Junction−to−Ambient (Notes 3, 4) | $R_{\theta JA}$ | 62.5 | |

3. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted.
4. Assembled to an infinite heatsink with perfect heat transfer from the case (assumes 0 K/W thermal interface).

### MARKING DIAGRAM




&Z = Assembly Plant Code
&3 = Date Code (Year & Week)
&K = Assembly Lot
V055N60S5F = Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

## ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = 1 mA, $T_J$ = 25°C | 600 | | | V |
| Drain−to−Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/\Delta T_J$ | $I_D$ = 10 mA, Referenced to 25°C | | 581 | | mV/°C |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 600 V, $T_J$ = 25°C | | | 10 | μA |
| Gate−to−Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±30 V, $V_{DS}$ = 0 V | | | ±100 | nA |
| **ON CHARACTERISTICS** | | | | | | |
| Drain−to−Source On Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 22.5 A, $T_J$ = 25°C | | 44 | 55 | mΩ |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 5.2 mA, $T_J$ = 25°C | 3.2 | 4.12 | 4.8 | V |
| Gate Threshold Voltage Temperature Coefficient | $V_{GS(th)}/\Delta T_J$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 5.2 mA | | −6.61 | | mV/°C |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ = 20 V, $I_D$ = 22.5 A | | 44.8 | | S |
| **CHARGES, CAPACITANCES & GATE RESISTANCE** | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{DS}$ = 400 V, $V_{GS}$ = 0 V, f = 250 KHz | | 4603 | | pF |
| Output Capacitance | $C_{OSS}$ | | | 72.9 | | |
| Energy Related Output Capacitance | $C_{OSS(er)}$ | $V_{DS}$ = 0 to 400 V, $V_{GS}$ = 0 V | | 125 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{DD}$ = 400 V, $I_D$ = 22.5 A, $V_{GS}$ = 10 V | | 85.2 | | nC |
| Gate−to−Source Charge | $Q_{GS}$ | | | 26.2 | | |
| Gate−to−Drain Charge | $Q_{GD}$ | | | 24.9 | | |
| Gate Resistance | $R_G$ | f = 1 MHz | | 4.32 | | Ω |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| Turn-On Delay Time | $t_{d(ON)}$ | $V_{GS}$ = 0/10 V, $V_{DD}$ = 400 V, $I_D$ = 22.5 A, $R_G$ = 4.7 Ω | | 44 | | ns |
| Rise Time | $t_r$ | | | 26.2 | | |
| Turn−Off Delay Time | $t_{d(OFF)}$ | | | 108 | | |
| Fall Time | $t_f$ | | | 2.6 | | |
| **SOURCE−TO−DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward Diode Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_{SD}$ = 22.5 A, $T_J$ = 25°C | | 1.07 | | V |
| | | $V_{GS}$ = 0 V, $I_{SD}$ = 22.5 A, $T_J$ = 150°C | | 0.82 | | |
| Reverse Recovery Time | $t_{RR}$ | $V_{GS}$ = 0 V, $I_{SD}$ = 22.5 A, dI/dt = 100 A/μs, $V_{DD}$ = 400 V | | 128 | | ns |
| Reverse Recovery Charge | $Q_{RR}$ | | | 758 | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## PACKAGE MARKING AND ORDERING INFORMATION

| Part Number | Top Marking | Package | Packing Method | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|---|
| NVB055N60S5F | V055N60S5F | $D^2PAK$ | Tape & Reel† | 330 mm | 24 mm | 800 Units |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## TYPICAL CHARACTERISTICS

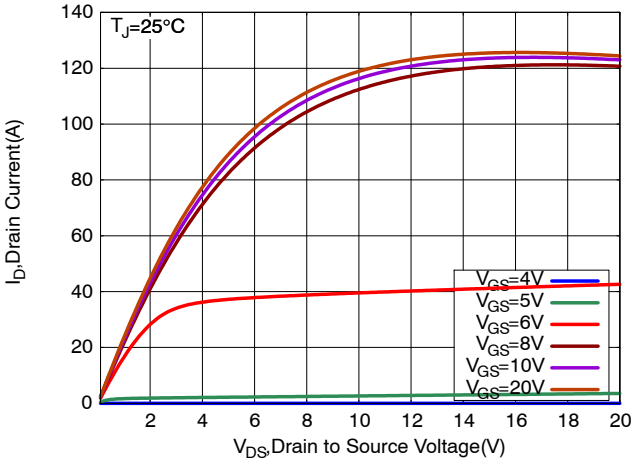



**Figure 1. On−Region Characteristics**

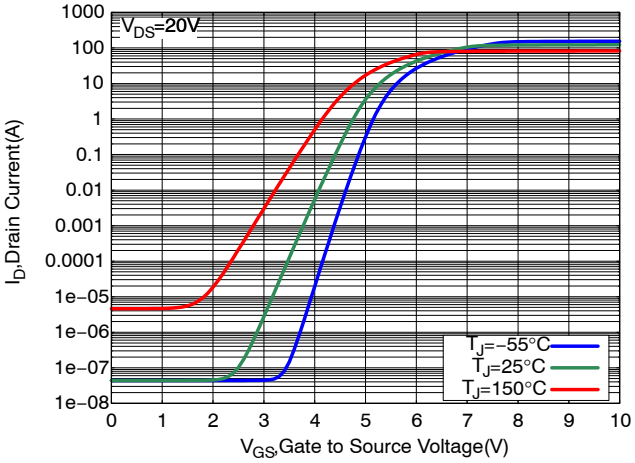



**Figure 2. Transfer Characteristics**

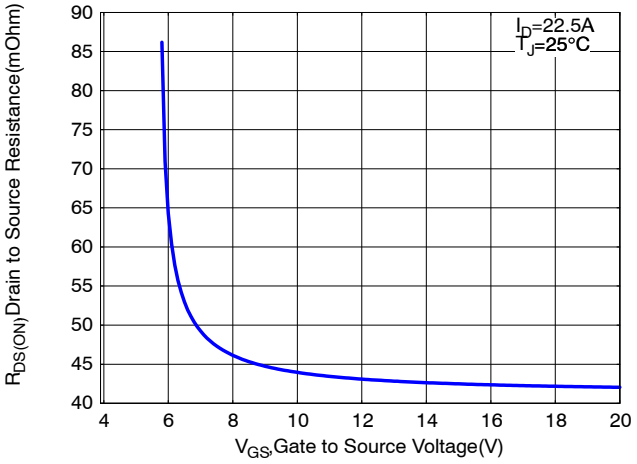



**Figure 3. On−Resistance vs. $V_{GS}$**

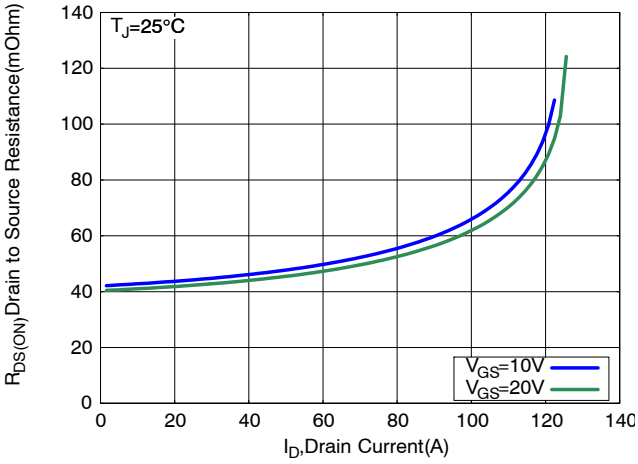



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

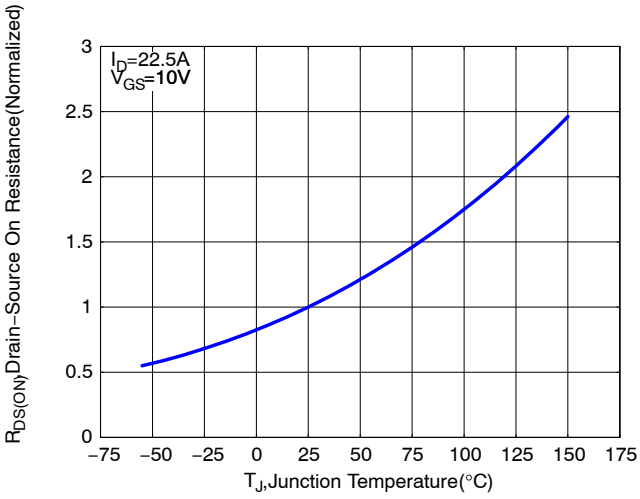



**Figure 5. On−Resistance Variation with Temperature**

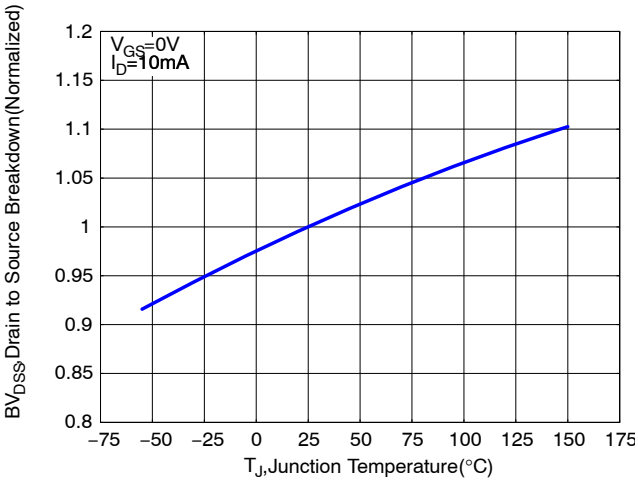



**Figure 6. Breakdown Voltage Variation with Temperature**

## TYPICAL CHARACTERISTICS

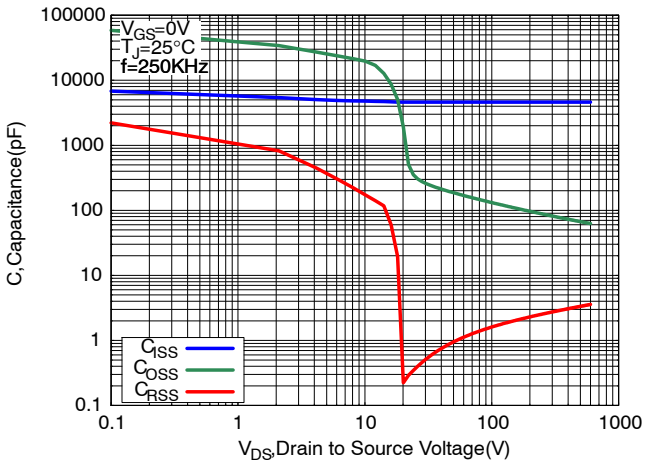



**Figure 7. Capacitance Variation**

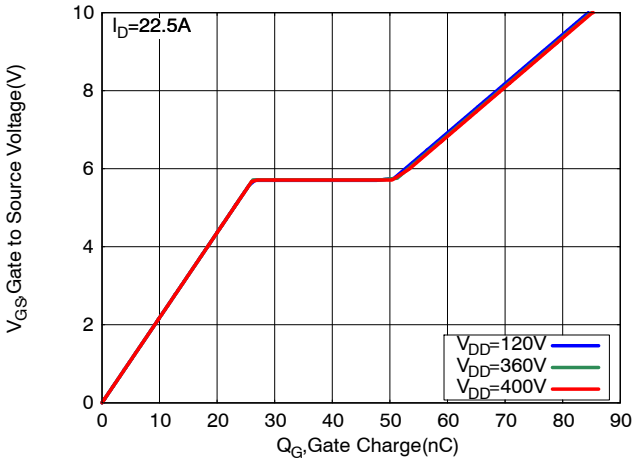



**Figure 8. Gate−to−Source Voltage vs. Total Charge**

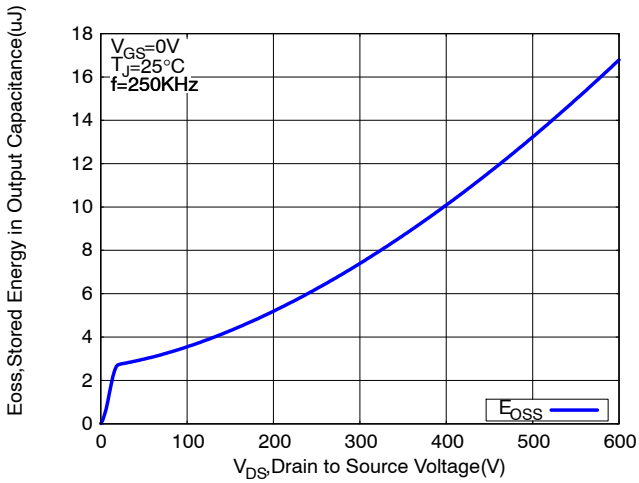



**Figure 9. Eoss vs. Drain−to−Source Voltage**

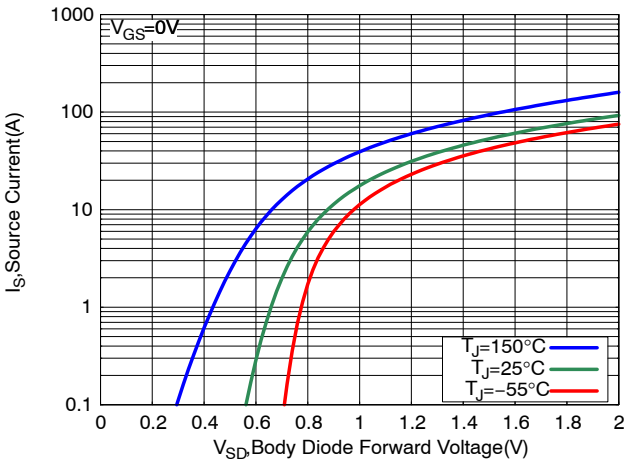



**Figure 10. Diode Forward Voltage vs. Current**

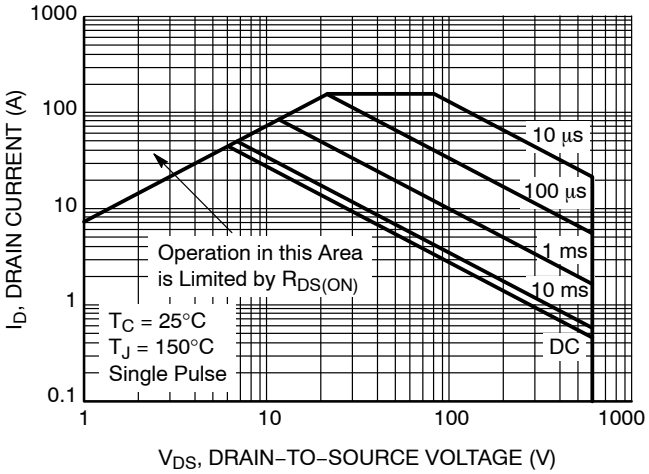



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

## TYPICAL CHARACTERISTICS

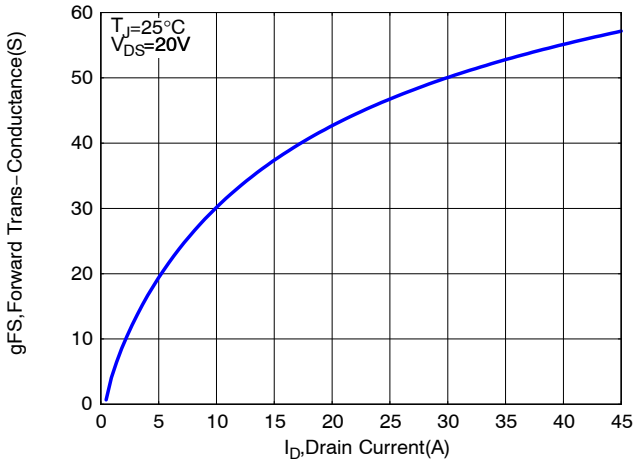



**Figure 12. $g_{FS}$ vs. $I_D$**

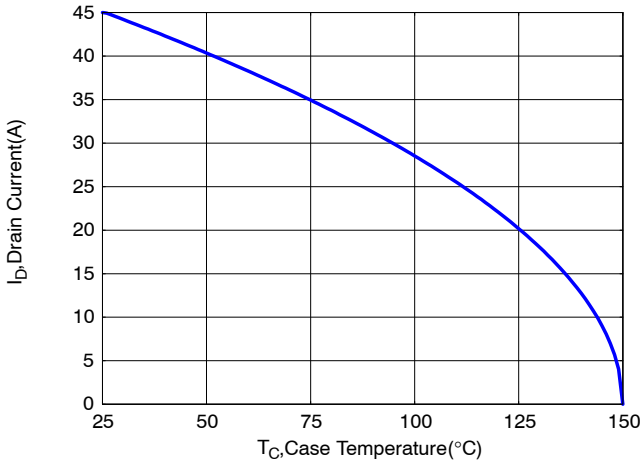



**Figure 13. Maximum Current vs. Case Temperature**

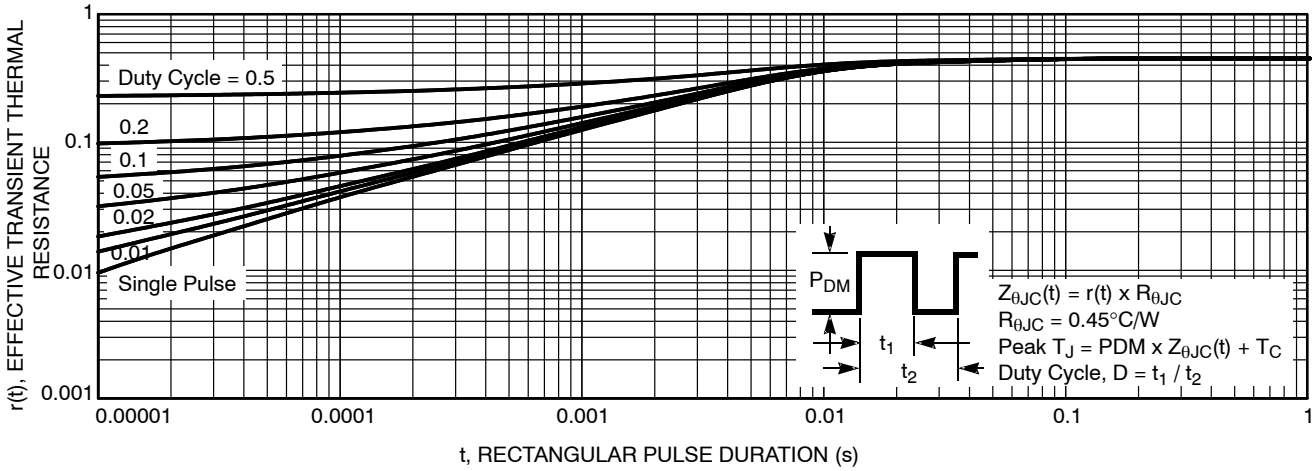
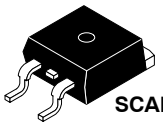



**Figure 14. Thermal Response**

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

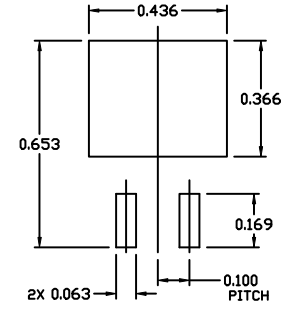
ON Semiconductor®



SCALE 1:1

**D²PAK–3 (TO–263, 3–LEAD)**
CASE 418AJ
ISSUE F

DATE 11 MAR 2021



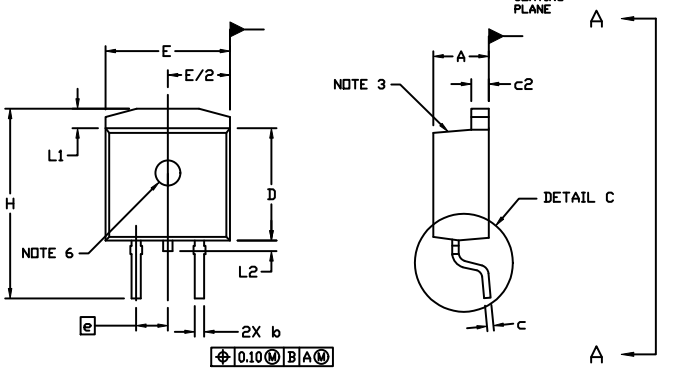

RECOMMENDED
MOUNTING FOOTPRINT

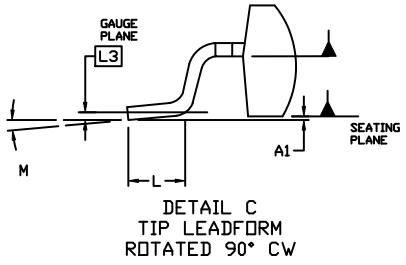
* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

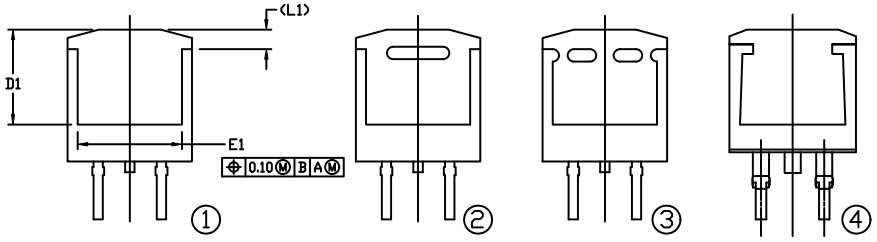
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN. | MAX. | MIN. | MAX. |
| A | 0.160 | 0.190 | 4.06 | 4.83 |
| A1 | 0.000 | 0.010 | 0.00 | 0.25 |
| b | 0.020 | 0.039 | 0.51 | 0.99 |
| c | 0.012 | 0.029 | 0.30 | 0.74 |
| c2 | 0.045 | 0.065 | 1.14 | 1.65 |
| D | 0.330 | 0.380 | 8.38 | 9.65 |
| D1 | 0.260 | --- | 6.60 | --- |
| E | 0.380 | 0.420 | 9.65 | 10.67 |
| E1 | 0.245 | --- | 6.22 | --- |
| e | 0.100 BSC | | 2.54 BSC | |
| H | 0.575 | 0.625 | 14.60 | 15.88 |
| L | 0.070 | 0.110 | 1.78 | 2.79 |
| L1 | --- | 0.066 | --- | 1.68 |
| L2 | --- | 0.070 | --- | 1.78 |
| L3 | 0.010 BSC | | 0.25 BSC | |
| M | 0° | 8° | 0° | 8° |



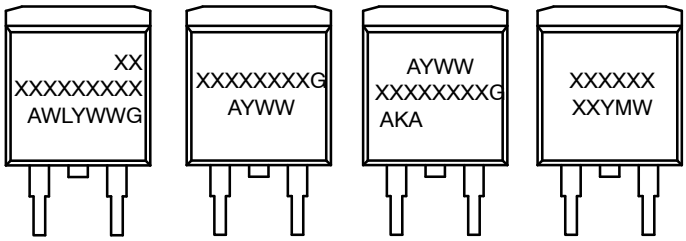

DETAIL C
TIP LEADFORM
ROTATED 90° CW




VIEW A–A

VIEW A–A
OPTIONAL CONSTRUCTIONS

### GENERIC MARKING DIAGRAMS*




IC | Standard | Rectifier | SSG

XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb–Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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| **DESCRIPTION:** | **D²PAK–3 (TO–263, 3–LEAD)** | **PAGE 1 OF 1** |

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