

NTTFS1D8N02P1E

Product Preview

Power MOSFET

25 V, 152 A, Single N-Channel, Power33

Features

- Small Footprint for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- DC-DC Converters
- Power Load Switch
- Notebook Battery Management

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	25	V	
Gate-to-Source Voltage	V_{GS}	+16, -12	V	
Continuous Drain Current $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	152	A
		$T_C = 85^\circ\text{C}$	110	
		$T_C = 25^\circ\text{C}$	P_D	48
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)	Steady State	$T_A = 25^\circ\text{C}$	36	A
		$T_A = 85^\circ\text{C}$	26	
		$T_A = 25^\circ\text{C}$	P_D	2.7
Continuous Drain Current $R_{\theta JA}$ (Notes 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	20	A
		$T_A = 85^\circ\text{C}$	14	
		$T_A = 25^\circ\text{C}$	P_D	0.8
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM}	TBD	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = \text{TBD A}, L = 0.1 \text{ mH}$) (Note 4)	E_{AS}	TBD	mJ	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$	
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using a 1 in² pad size, 2 oz Cu pad.
2. Surface-mounted on FR4 board using minimum pad size, 2 oz Cu pad.
3. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted. Actual continuous current will be limited by thermal & electro-mechanical application board design. $R_{\theta CA}$ is determined by the user's board design.
4. 100% UIS tested at $L = 0.1 \text{ mH}, I_{AV} = \text{TBD A}$.

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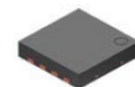
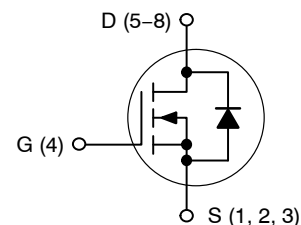


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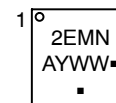
$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
25 V	1.3 m Ω @ 10 V	152 A
	1.8 m Ω @ 4.5 V	

NMOS



**PqFN8
(Power33)
CASE 483AW**

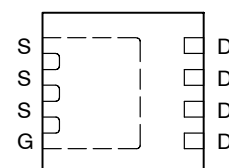
MARKING DIAGRAM



- 2EMN = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

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THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case – Steady State (Note 1)	$R_{\theta JC}$	2.7	°C/W
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	47	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	152	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	25			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\ \mu\text{A}$, ref to 25°C		TBD		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = +16\text{ V}, -12\text{ V}$			± 100	$\pm\text{nA}$

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 700\ \mu\text{A}$	1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 934\ \mu\text{A}$, ref to 25°C		TBD		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 30\text{ A}$	1.15	1.3	m Ω
		$V_{GS} = 4.5\text{ V}$	$I_D = 27\text{ A}$	1.4	1.8	
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 27\text{ A}$		TBD		S
Gate Resistance	R_G	$T_A = 25^\circ\text{C}$		0.8		Ω

CHARGES & CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, V_{DS} = 13\text{ V}, f = 1\text{ MHz}$		3159		pF
Output Capacitance	C_{OSS}			860		
Reverse Capacitance	C_{RSS}			41		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 13\text{ V}; I_D = 27\text{ A}$		19		nC
Threshold Gate Charge	$Q_{G(TH)}$			TBD		
Gate-to-Drain Charge	Q_{GD}			2.8		
Gate-to-Source Charge	Q_{GS}			7.6		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 13\text{ V}; I_D = 30\text{ A}$		38		

SWITCHING CHARACTERISTICS, $V_{GS} = 4.5\text{ V}$ (Note 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DD} = 13\text{ V}, I_D = 27\text{ A}, R_G = 6\ \Omega$		TBD		ns
Rise Time	t_r			TBD		
Turn-Off Delay Time	$t_{d(OFF)}$			TBD		
Fall Time	t_f			TBD		

SWITCHING CHARACTERISTICS, $V_{GS} = 10\text{ V}$ (Note 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DD} = 13\text{ V}, I_D = 30\text{ A}, R_G = 6\ \Omega$		TBD		ns
Rise Time	t_r			TBD		
Turn-Off Delay Time	$t_{d(OFF)}$			TBD		
Fall Time	t_f			TBD		

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 30\text{ A}$	$T_J = 25^\circ\text{C}$	0.77	1.3	V
			$T_J = 125^\circ\text{C}$	0.63		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, di/dt = 100\text{ A}/\mu\text{s}, I_S = 30\text{ A}$		TBD		ns
Reverse Recovery Charge	Q_{RR}			TBD		nC

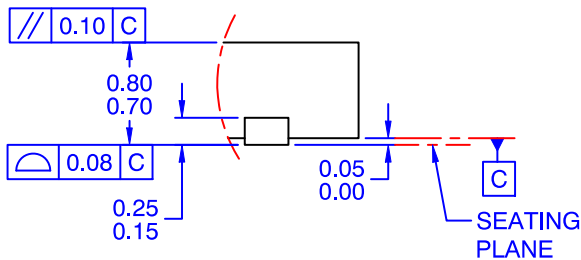
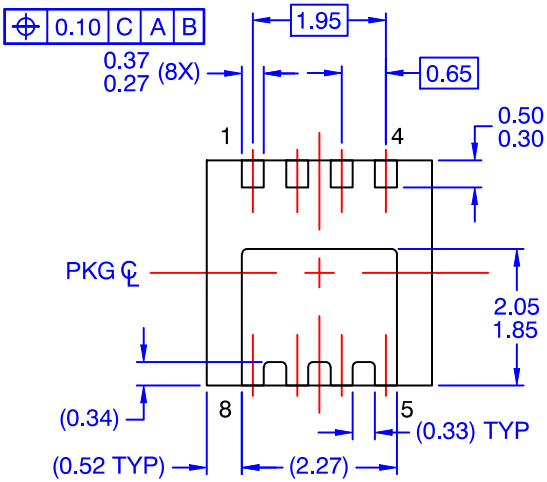
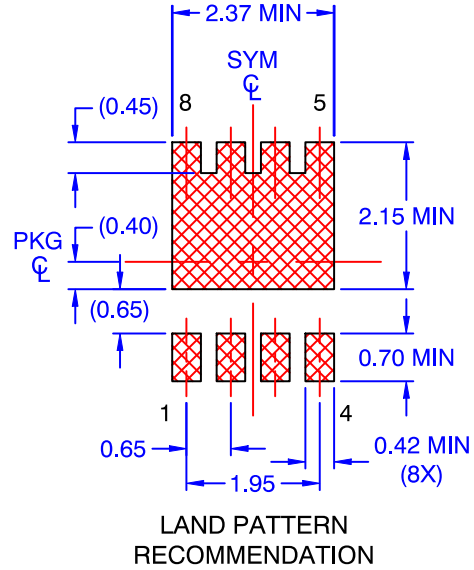
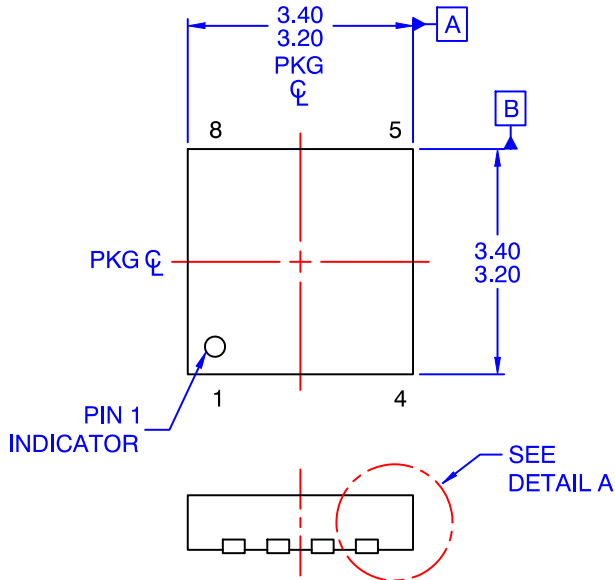
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Switching characteristics are independent of operating junction temperatures.

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PACKAGE DIMENSIONS

PQFN8 3.3X3.3, 0.65P
CASE 483AW
ISSUE O



DETAIL A
SCALE: 2X

NOTES: UNLESS OTHERWISE SPECIFIED


- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA, DATED OCTOBER 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

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ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTTFS1D8N02P1E	2EMN	Power33 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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