NTTFS1D8N02P1E

Product Preview

Power MOSFET

25 V, 152 A, Single N−Channel, Power33

Features

- Small Footprint for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- DC−DC Converters
- Power Load Switch
- Notebook Battery Management

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	25	V
Gate−to−Source Voltage			V_{GS}	+16, −12	V
Continuous Drain Current $R_{\theta JC}$ (Note 1)	Steady State	T_C = 25°C	I_D	152	A
		T_C = 85°C		110	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	48	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3)	Steady State	T_A = 25°C	I_D	36	A
		T_A = 85°C		26	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)		T_A = 25°C	P_D	2.7	W
Continuous Drain Current $R_{\theta JA}$ (Notes 2, 3)	Steady State	T_A = 25°C	I_D	20	A
		T_A = 85°C		14	
Power Dissipation $R_{\theta JA}$ (Notes 2, 3)		T_A = 25°C	P_D	0.8	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	TBD	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = TBD A, L = 0.1 mH) (Note 4)			E_{AS}	TBD	mJ
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +150	°C
Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface−mounted on FR4 board using a 1 in^2 pad size, 2 oz Cu pad.
2. Surface−mounted on FR4 board using minimum pad size, 2 oz Cu pad.
3. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted. Actual continuous current will be limited by thermal & electro−mechanical application board design. $R_{\theta CA}$ is determined by the user's board design.
4. 100% UIS tested at L = 0.1 mH, I_{AV} = TBD A.

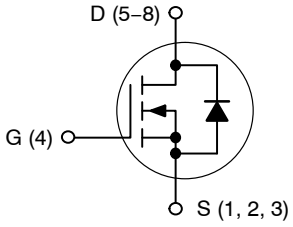
This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

ON Semiconductor®

www.onsemi.com

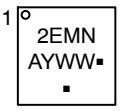
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
25 V	1.3 mΩ @ 10 V	152 A
	1.8 mΩ @ 4.5 V	

NMOS



PQFN8
(Power33)
CASE 483AW

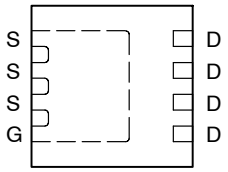
MARKING DIAGRAM



2EMN	= Specific Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Case − Steady State (Note 1)	$R_{\theta JC}$	2.7	°C/W
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	47	
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	152	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

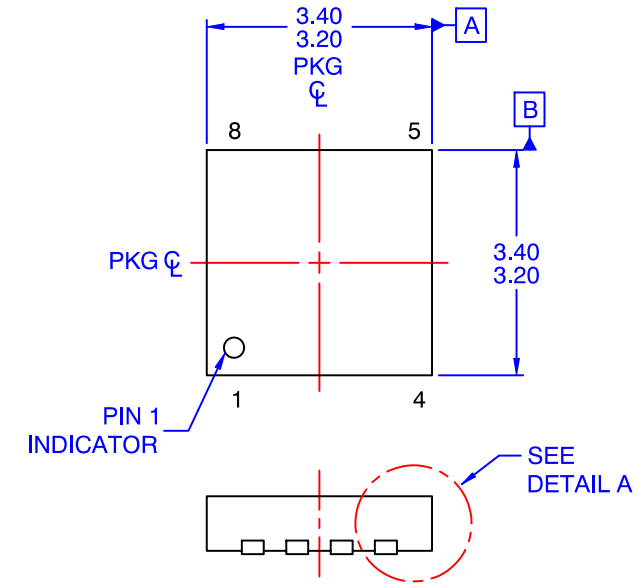
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		25			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, ref to 25°C			TBD		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 20 V	T_J = 25°C			1.0	μA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = +16 V, −12 V				±100	±nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 700 μA		1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 934 μA, ref to 25°C			TBD		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 30 A		1.15	1.3	mΩ
		V_{GS} = 4.5 V	I_D = 27 A		1.4	1.8	
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 27 A			TBD		S
Gate Resistance	R_G	T_A = 25°C			0.8		Ω
CHARGES & CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, V_{DS} = 13 V, f = 1 MHz			3159		pF
Output Capacitance	C_{OSS}				860		
Reverse Capacitance	C_{RSS}				41		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 13 V; I_D = 27 A			19		nC
Threshold Gate Charge	$Q_{G(TH)}$				TBD		
Gate−to−Drain Charge	Q_{GD}				2.8		
Gate−to−Source Charge	Q_{GS}				7.6		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 13 V; I_D = 30 A			38		
SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DD} = 13 V, I_D = 27 A, R_G = 6 Ω			TBD		ns
Rise Time	t_r				TBD		
Turn−Off Delay Time	$t_{d(OFF)}$				TBD		
Fall Time	t_f				TBD		
SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DD} = 13 V, I_D = 30 A, R_G = 6 Ω			TBD		ns
Rise Time	t_r				TBD		
Turn−Off Delay Time	$t_{d(OFF)}$				TBD		
Fall Time	t_f				TBD		
SOURCE−TO−DRAIN DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 30 A	T_J = 25°C		0.77	1.3	V
			T_J = 125°C		0.63		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI/dt = 100 A/μs, I_S = 30 A			TBD		ns
Reverse Recovery Charge	Q_{RR}				TBD		nC

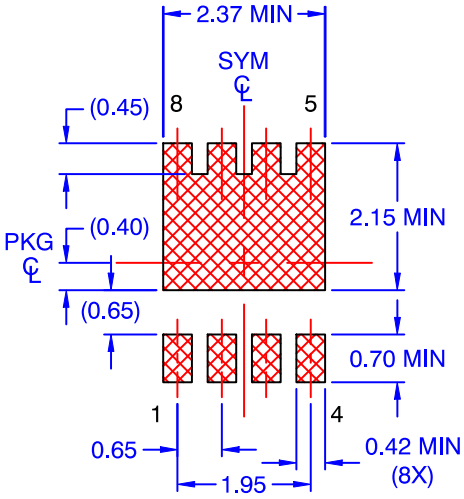
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Switching characteristics are independent of operating junction temperatures.

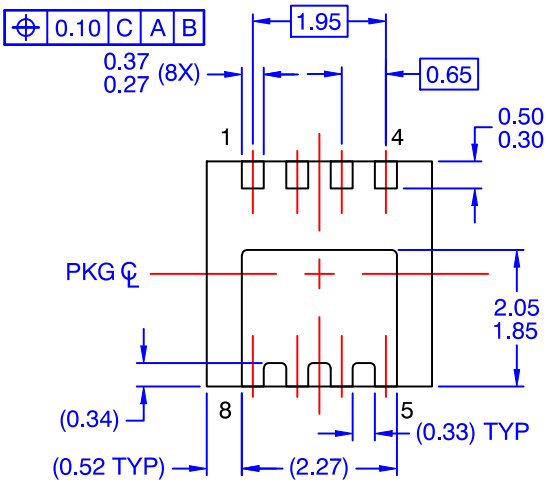
PACKAGE DIMENSIONS

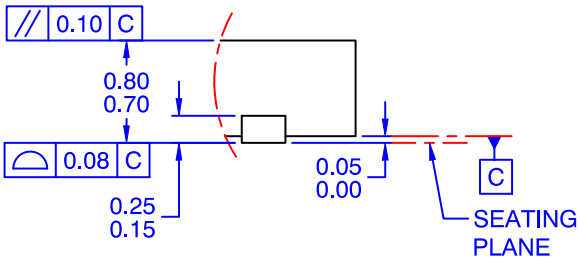
PQFN8 3.3X3.3, 0.65P
CASE 483AW
ISSUE O





LAND PATTERN
RECOMMENDATION





DETAIL A
SCALE: 2X

NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE: JEDEC MO−240, ISSUE A, VAR. BA, DATED OCTOBER 2002.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTTFS1D8N02P1E	2EMN	Power33 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative