NTTFS010N10MCL

MOSFET, N-Channel, Shielded Gate, POWERTRENCH®

100 V, 50 A, 10.6 mΩ

General Description

This N−Channel POWETRENCH® MOSFET is produced using ON Semiconductor’s advanced POWERTRENCH® process that incorporates Shielded Gate technology. This process has been optimized to minimize on−state resistance and yet maintain superior switching performance with best in class soft body diode.

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 10.6 mΩ at V_{GS} = 10 V, I_D = 15 A
- Max $r_{DS(on)}$ = 15.9 mΩ at V_{GS} = 4.5 V, I_D = 12 A
- 50% Lower Qrr than Other MOSFET Suppliers
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested
- RoHS Compliant

Applications

- Primary DC−DC MOSFET
- Synchronous Rectifier in DC−DC and AC−DC
- Motor Drive

ON Semiconductor®

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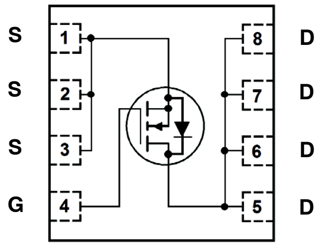
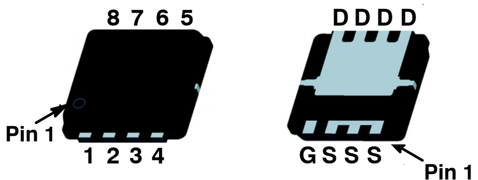
ELECTRICAL CONNECTION



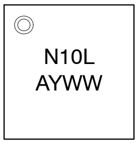
N-Channel MOSFET



Top **Bottom**

WDFN8
(3.3x3.3, 0.65 P)
CASE 511DY

MARKING DIAGRAM



N10L = Device Code
A = Assembly Location
Y = Year Code
WW = Work Week Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current –Continuous $T_C = 25°C$ (Note 5)	50	A
	–Continuous $T_C = 100°C$ (Note 5)	32	
	–Continuous $T_A = 25°C$ (Note 1a)	10.7	
	–Pulsed (Note 4)	250	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	73	mJ
P_D	Power Dissipation $T_C = 25°C$	52	W
	Power Dissipation $T_A = 25°C$ (Note 1a)	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Quantity
NTTFS010N10MCL	N10L	WDFN8 (3.3x3.3)	7”	12 mm	1500 Units

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu A$, $V_{GS} = 0\ V$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu A$, referenced to 25°C		64		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\ V$, $V_{GS} = 0\ V$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ V$, $V_{DS} = 0\ V$			100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 85\ \mu A$	1.0	1.5	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 85\ \mu A$, referenced to 25°C		–5.3		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ V$, $I_D = 15\ A$		9.1	10.6	mΩ
		$V_{GS} = 4.5\ V$, $I_D = 12\ A$		13.5	15.9	
		$V_{GS} = 10\ V$, $I_D = 15\ A$, $T_J = 125°C$		15.3	17.8	
g_{FS}	Forward Transconductance	$V_{DS} = 5\ V$, $I_D = 15\ A$		54		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	$V_{DS} = 50\ V$, $V_{GS} = 0\ V$, f = 1 MHz		1530	2150	pF
C_{OSS}	Output Capacitance			625	875	
C_{RSS}	Reverse Transfer Capacitance			10	18	
R_G	Gate Resistance		0.1	1.1	2.1	Ω

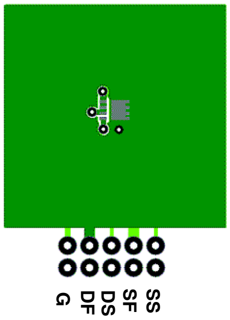
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS						
$t_{d(ON)}$	Turn – On Delay Time	V_{DD} = 50 V, I_D = 15 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		9	19	ns
$t_{rd(ON)}$	Rise Time			3	10	
$t_{d(OFF)}$	Turn – Off Delay Time			28	45	
t_f	Fall Time			5	10	
Q_g	Total Gate Charge	V_{GS} = 0V to 10 V V_{DD} = 50 V I_D = 15 A		22	30	nC
Q_g	Total Gate Charge	V_{GS} = 0V to 4.5 V		10		
Q_{gs}	Gate to Source Charge			4		
Q_{gd}	Gate to Drain “Miller” Charge			3		
Q_{oss}	Output Charge	V_{DD} = 50 V, V_{GS} = 0 V		41		nC
Q_{sync}	Total Gate Charge Sync	V_{DS} = 0 V, V_{GS} = 0 to 10 V		19		
DRAIN–SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2 A (Note 2)		0.7	1.2	V
		V_{GS} = 0 V, I_S = 15 A (Note 2)		0.8	1.3	
t_{rr}	Reverse Recovery Time	I_F = 8 A, di/dt = 300 A/μs		22	36	ns
Q_{rr}	Reverse Recovery Charge			35	56	nC
t_{rr}	Reverse Recovery Time	I_F = 8 A, di/dt = 1000 A/μs		17	30	ns
Q_{rr}	Reverse Recovery Charge			79	126	nC

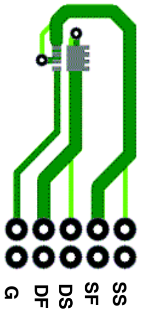
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta CA}$ is determined by the user’s board design.



a) 53°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 125°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 73 mJ is based on starting T_J = 25°C; L = 3 mH, I_{AS} = 7 A, V_{DD} = 100 V, V_{GS} = 10 V. 100% test at L = 0.5 mH, I_{AS} = 13 A.
4. Pulsed I_D please refer to Figure 11 SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro−mechanical application board design.

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

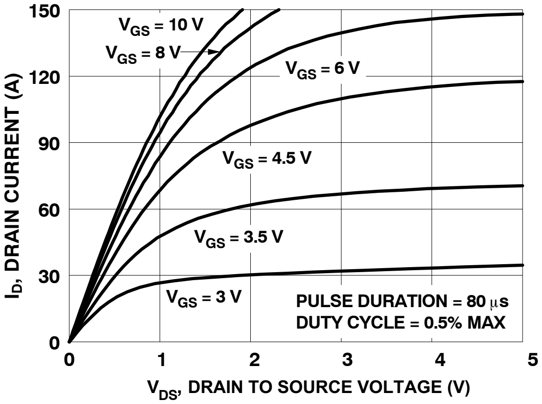


Figure 1. On Region Characteristics

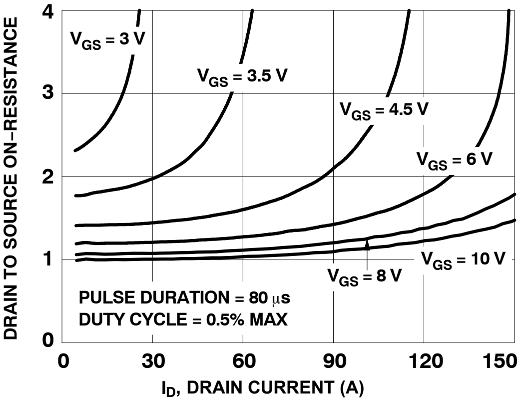


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

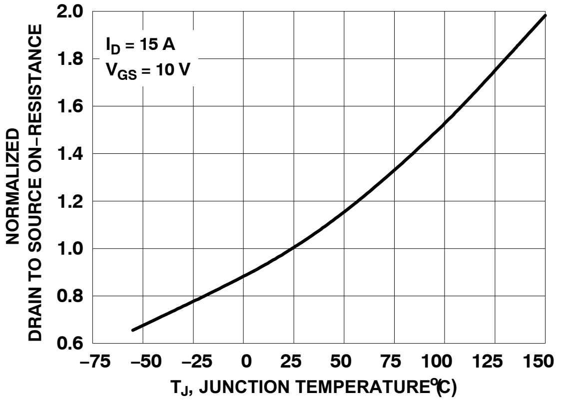


Figure 3. Normalized On Resistance vs. Junction Temperature

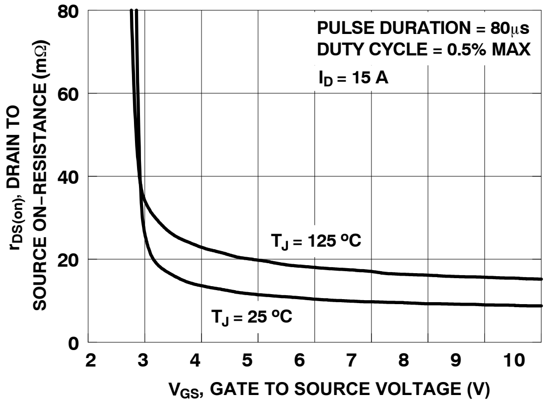


Figure 4. On-Resistance vs. Gate to Source Voltage

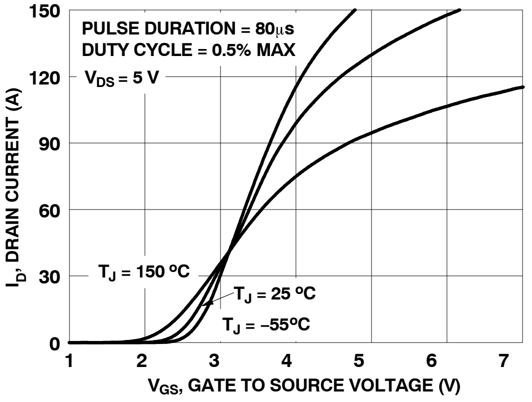


Figure 5. Transfer Characteristics

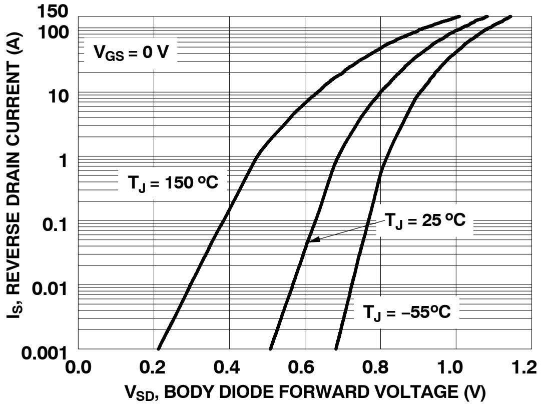


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (T$_J$ = 25°C unless otherwise noted)

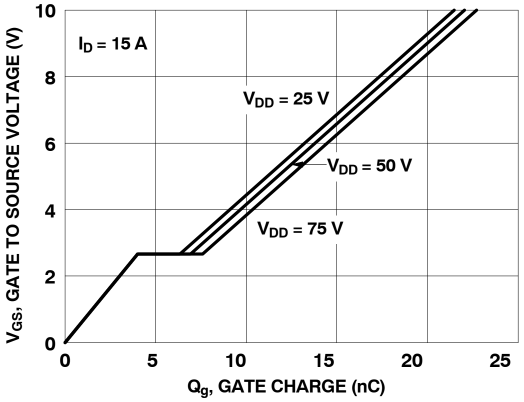


Figure 7. Gate Charge Characteristics

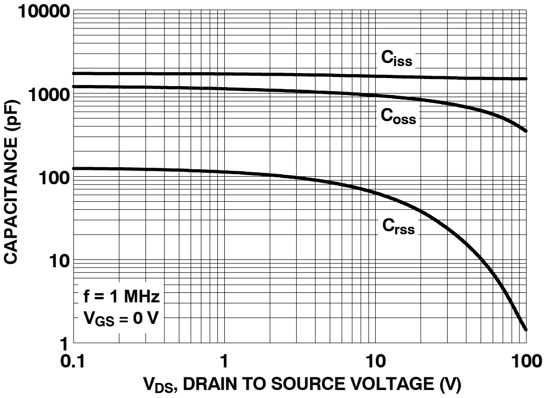


Figure 8. Capacitance vs. Drain to Source Voltage

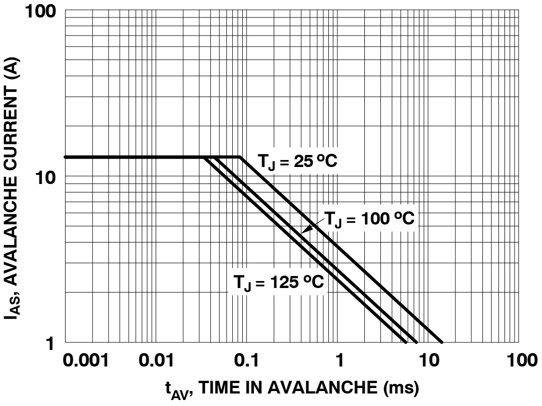


Figure 9. Unclamped Inductive Switching Capability

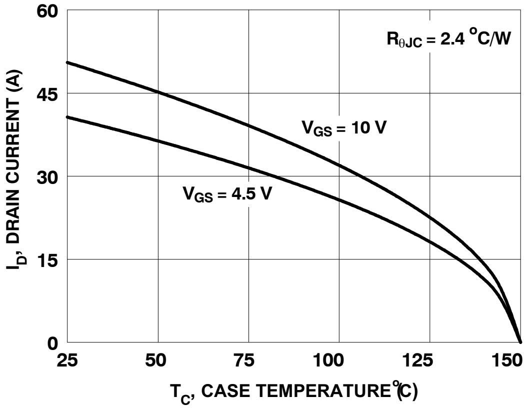


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

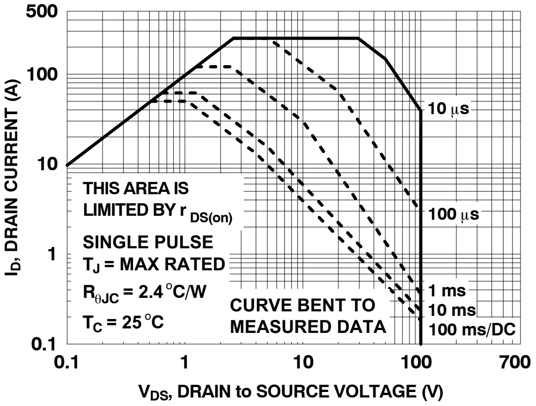


Figure 11. Forward Bias Safe Operating Area

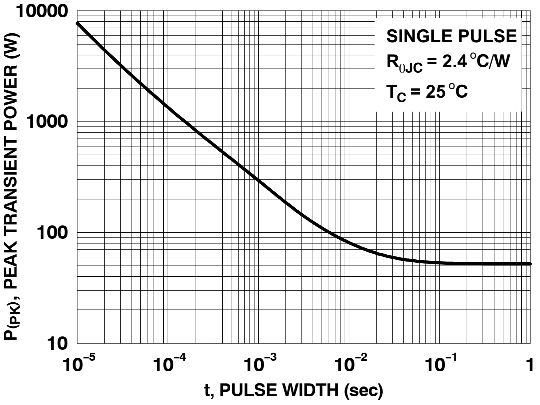


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

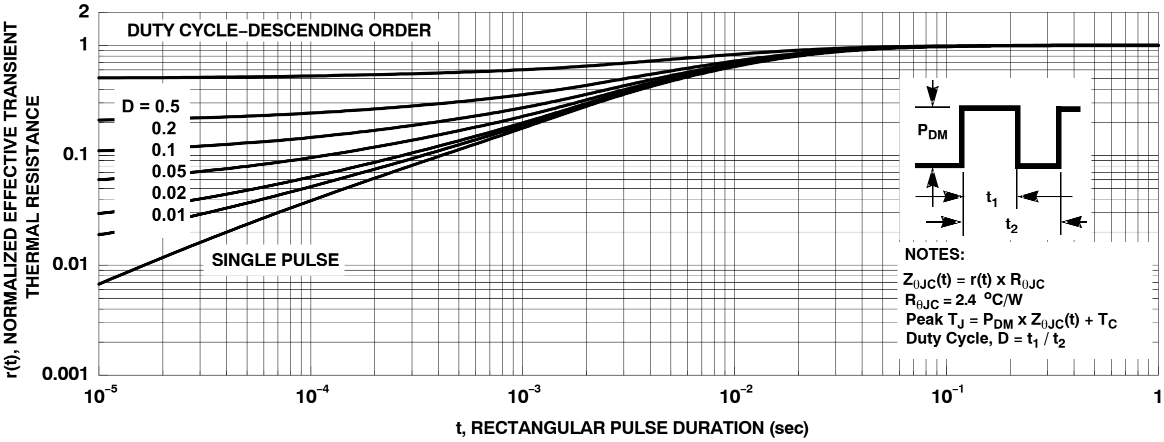
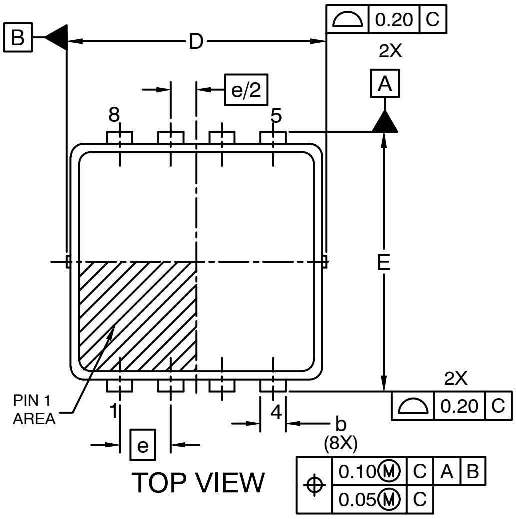


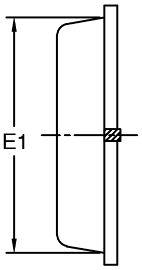
Figure 13. Junction−to−Case Transient Thermal Response Curve

PACKAGE DIMENSIONS

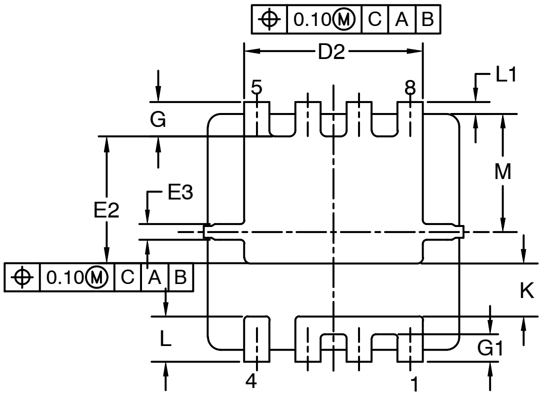
WDFN8 3.3x3.3, 0.65P
CASE 511DY
ISSUE A



TOP VIEW

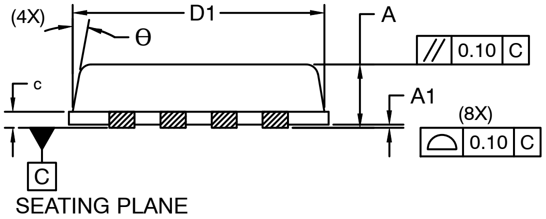


SIDE VIEW



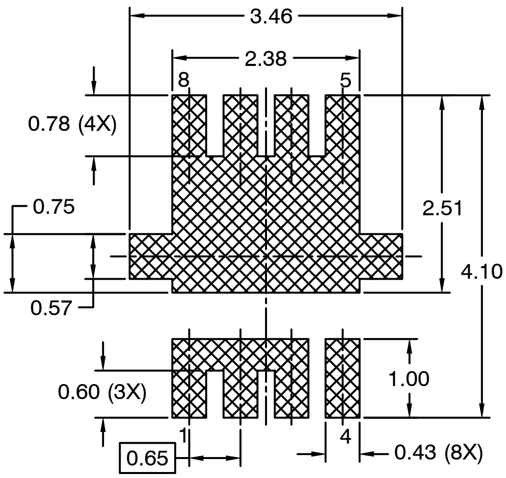
BOTTOM VIEW

NOTES:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS D1 & E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS.



END VIEW

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	–	0.05
b	0.23	0.33	0.43
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	2.95	3.13	3.30
D2	1.98	2.20	2.40
E	3.20	3.30	3.40
E1	2.80	3.00	3.15
E2	1.40	1.60	1.80
E3	0.15	0.25	0.40
e	0.65 BSC		
G	0.30	0.43	0.55
G1	0.25	0.35	0.45
K	0.55	0.75	0.95
L	0.35	0.52	0.65
L1	0.06	0.15	0.30
M	1.35	1.50	1.60
θ	0	–	12



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