MOSFET – Power, N-Channel, SUPERFET® III

800 V, 600 mΩ, 8 A

NTPF600N80S3Z

ON Semiconductor®

www.onsemi.com

Description

800 V SUPERFET III MOSFET is ON Semiconductor's high performance MOSFET family offering 800 V breakdown voltage.

New 800 V SUPERFET III MOSFET which is optimized for primary switch of flyback converter, enables lower switching losses and case temperature without sacrificing EMI performance thanks to its optimized design. In addition, internal Zener Diode significantly improves ESD capability.

This new family of 800 V SUPERFET III MOSFET enables to make more efficient, compact, cooler and more robust applications because of its remarkable performance in switching power applications such as Laptop adapter, Audio, Lighting, ATX power and industrial power supplies.

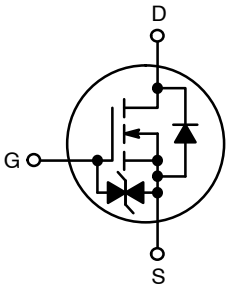
Features

- Typ. $R_{DS(on)}$ = 550 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 15.5 nC)
- Low Stored Energy in Output Capacitance (Eoss = 1.74 μJ @ 400 V)
- 100% Avalanche Tested
- ESD Improved Capability with Zener Diode
- RoHS Compliant

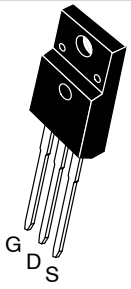
Applications

- Adapters / Chargers
- LED Lighting
- AUX Power
- Audio
- Industrial Power

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
800 V	600 mΩ	8 A

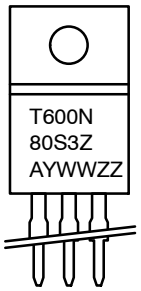


POWER MOSFET



TO−220F
CASE 221D

MARKING DIAGRAM



T600N80S3Z	= Specific Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
ZZ	= Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_J = 25°C, unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain−to−Source Voltage		800	V
V_{GS}	Gate−to−Source Voltage	DC	±20	V
		AC (f > 1 Hz)	±30	
I_D	Drain Current	Continuous (T_C = 25°C)	8*	A
		Continuous (T_C = 100°C)	5*	
I_{DM}	Drain Current	Pulsed (Note 1)	21*	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		24	mJ
I_{AS}	Avalanche Current (Note 2)		1.2	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		0.28	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		10	
P_D	Power Dissipation	(T_C = 25°C)	28	W
		Derate Above 25°C	0.23	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +150	°C
T_L	Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from Case for 10 seconds)		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*Drain current limited by maximum junction temperature.

1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. I_{AS} = 1.2 A, R_G = 25 Ω, starting T_J = 25°C.
3. $I_{SD} \le 2$ A, di/dt ≤ 200 A/μs, $V_{DD} \le 400$ V, starting T_J = 25°C.

THERMAL RESISTANCE RATINGS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction−to−Case − Steady State	4.4	°C/W
$R_{\theta JA}$	Junction−to−Ambient − Steady State	62.5	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packaging Method	Reel Size	Tape Width	Quantity
NTPF600N80S3Z	NTPF600N80S3Z	TO−220F	Tube	N/A	N/A	50 Units

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−to−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	800			V
		V_{GS} = 0 V, I_D = 1 mA, T_J = 150°C	900			V
ΔBV_{DSS} / ΔT_J	Drain−to−Source Breakdown Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C		1.1		V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 800 V, V_{GS} = 0 V			1	μA
		V_{DS} = 640 V, T_C = 125°C		0.8		
I_{GSS}	Gate−to−Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			1	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 0.18 mA	2.2		3.8	V
$R_{DS(on)}$	Static Drain−to−Source On Resistance	V_{GS} = 10 V, I_D = 4 A		550	600	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 4 A		9.4		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 250 kHz		725		pF
C_{oss}	Output Capacitance			12		pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		139		pF
$C_{oss(er.)}$	Energy Related Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		21		pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DD} = 400 V, I_D = 4 A, V_{GS} = 10 V (Note 4)		15.5		nC
Q_{gs}	Gate−to−Source Gate Charge			3.1		nC
Q_{gd}	Gate−to−Drain “Miller” Charge			5.1		nC
ESR	Equivalent Series Resistance	f = 1 MHz		3.5		Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 400 V, I_D = 4 A, V_{GS} = 10 V, R_g = 4.7 Ω (Note 4)		12.3		ns
t_r	Turn-On Rise Time			5.9		ns
$t_{d(off)}$	Turn-Off Delay Time			39.5		ns
t_f	Turn-Off Fall Time			8.2		ns
SOURCE−TO−DRAIN DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source−to−Drain Diode Forward Current				8	A
I_{SM}	Maximum Pulsed Source−to−Drain Diode Forward Current				21	A
V_{SD}	Source−to−Drain Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 4 A			1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 2 A, dI_F/dt = 100 A/μs		137		ns
Q_{rr}	Reverse Recovery Charge			0.91		μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS

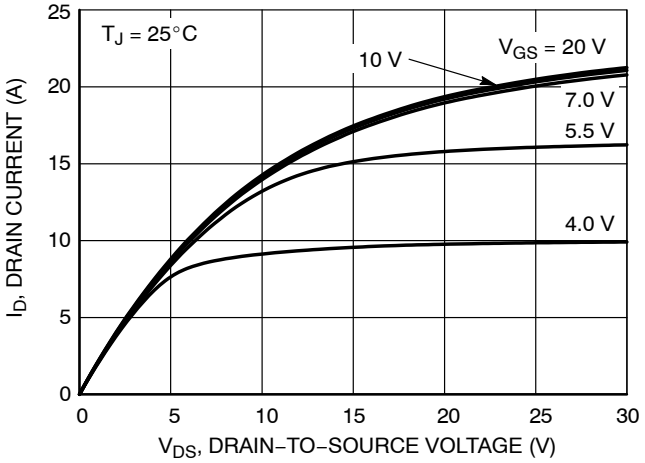


Figure 1. On−Region Characteristics

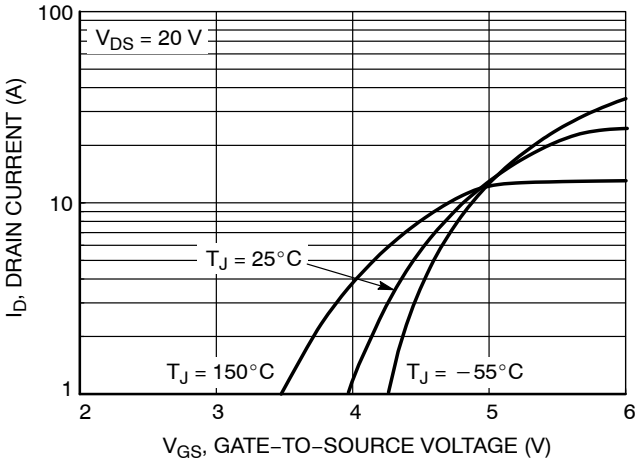


Figure 2. Transfer Characteristics

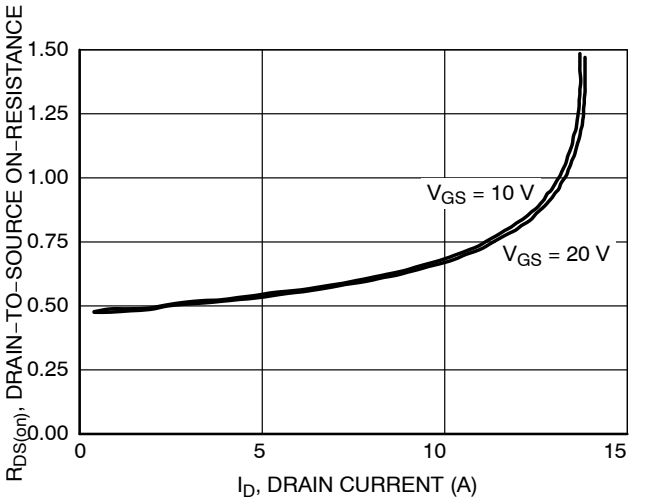


Figure 3. On Resistance vs. Drain Current

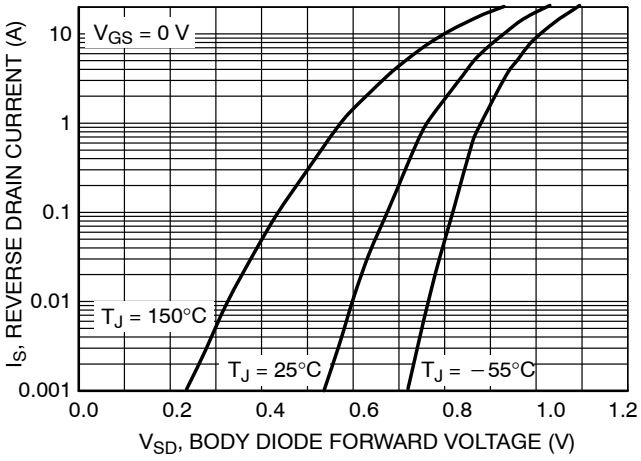


Figure 4. Diode Forward Voltage vs. Current

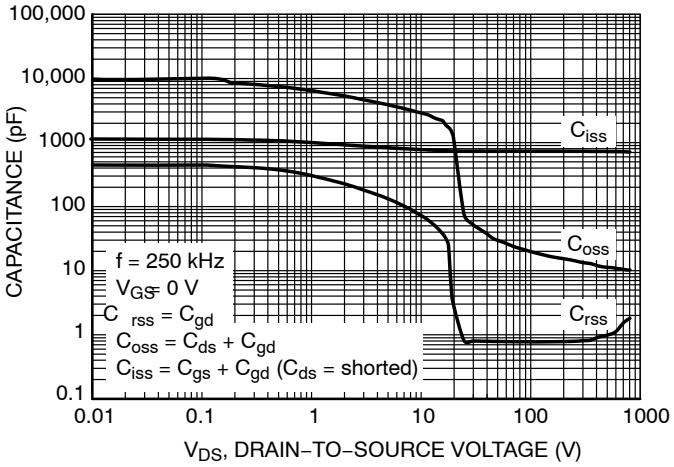


Figure 5. Capacitance Characteristics

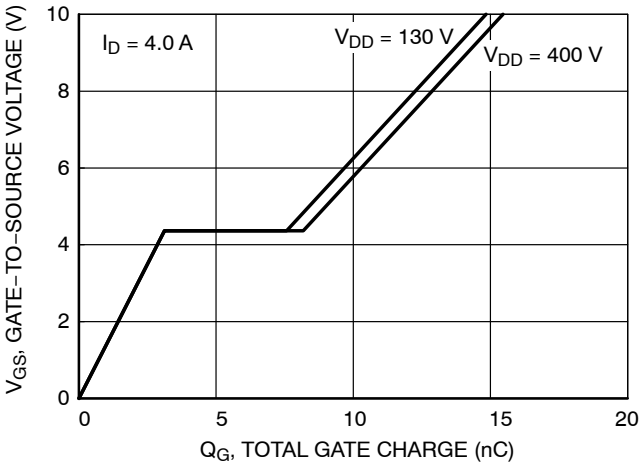


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

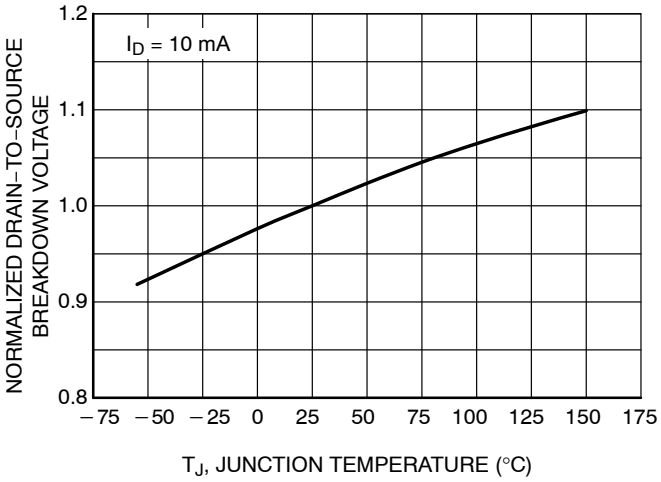


Figure 7. Normalized BV_{DSS} vs. Temperature

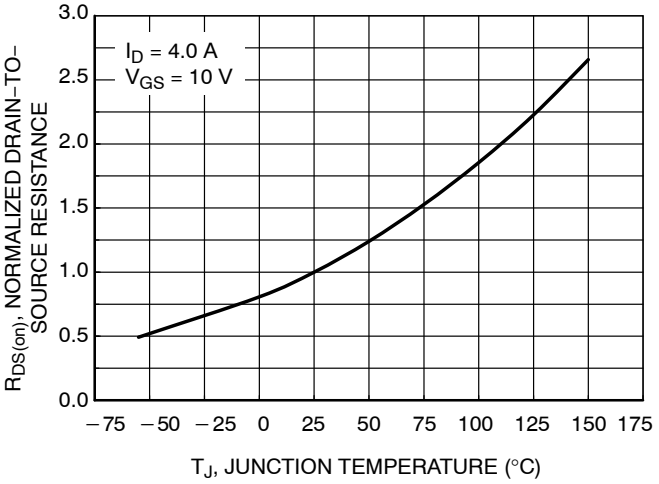


Figure 8. On−Resistance Variation vs. Temperature

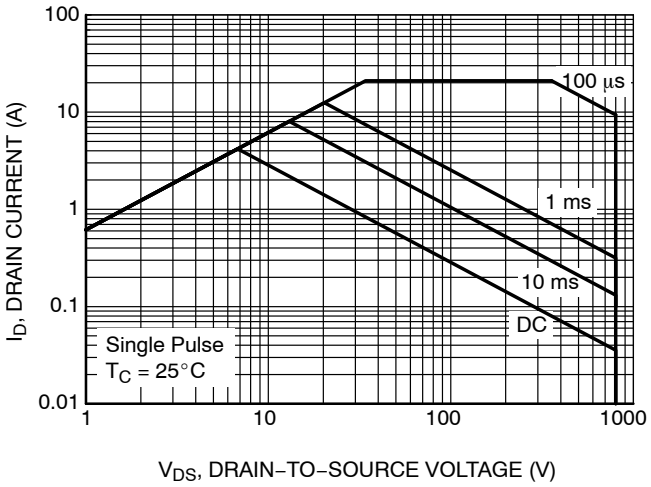


Figure 9. Safe Operating Area

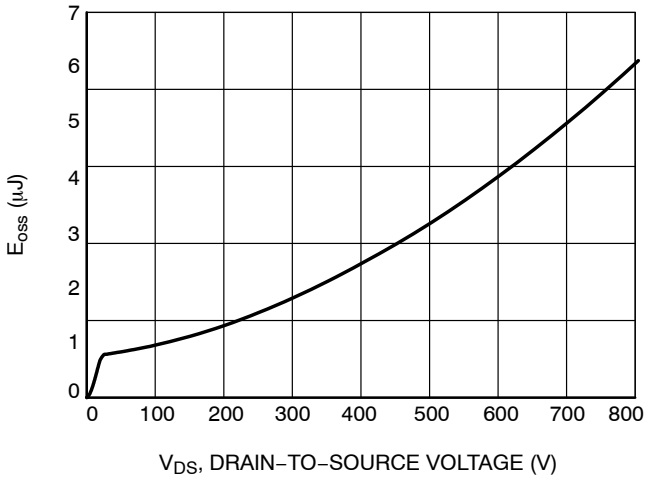


Figure 10. E_{oss} vs. Drain−to−Source Voltage

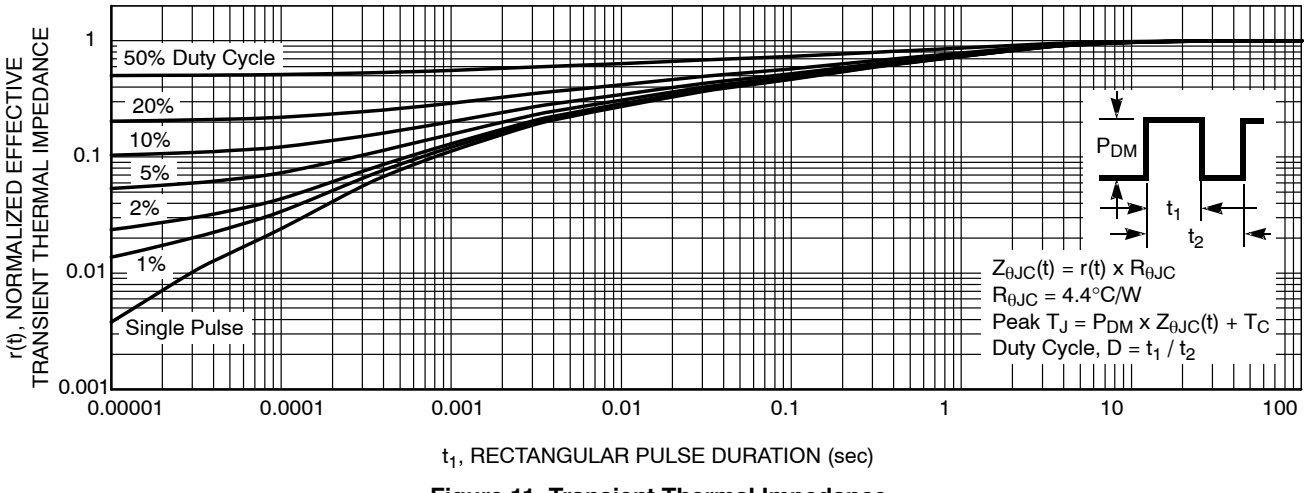


Figure 11. Transient Thermal Impedance

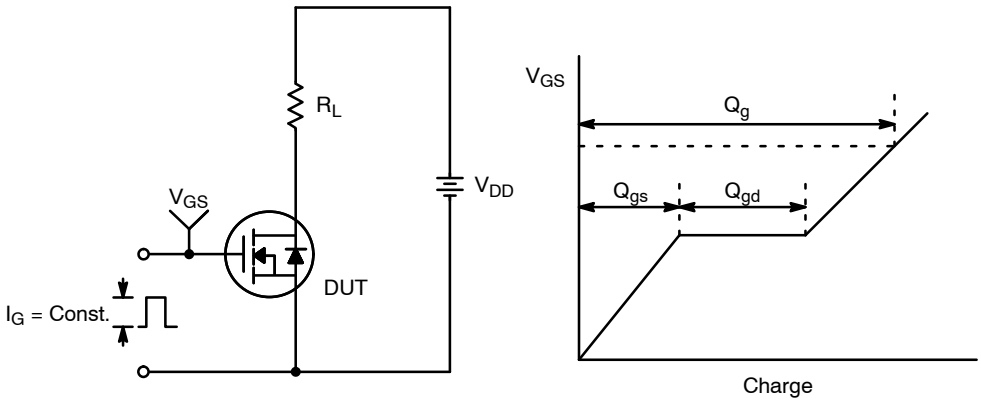


Figure 12. Gate Charge Test Circuit & Waveform

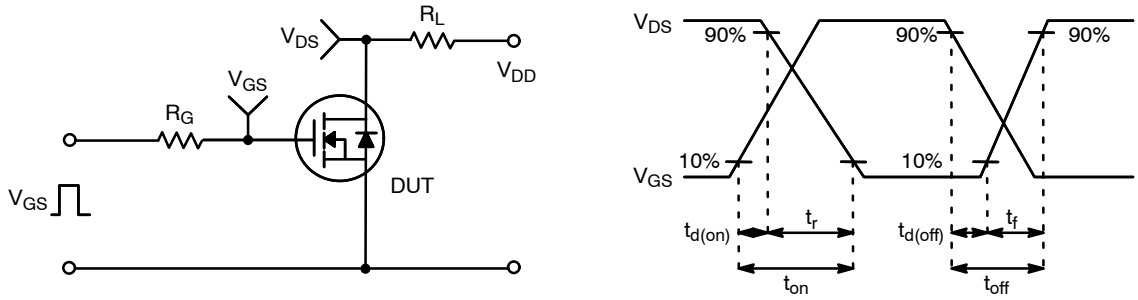


Figure 13. Resistive Switching Test Circuit & Waveforms

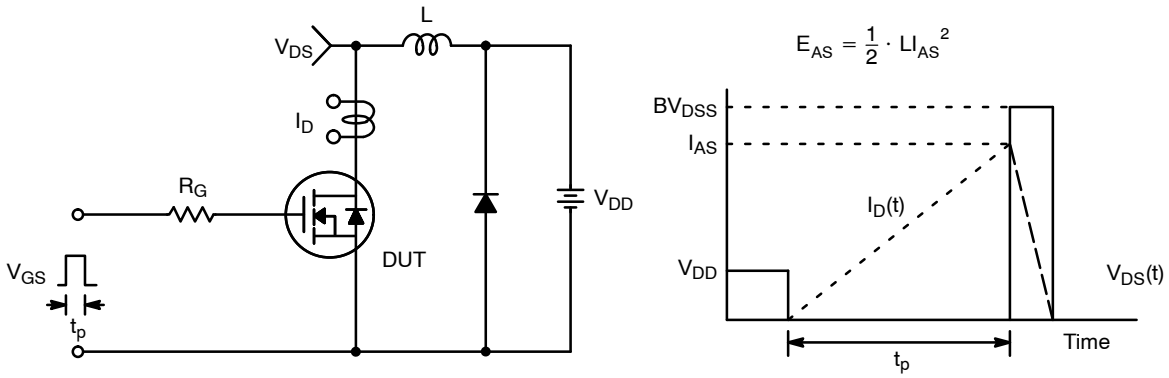


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

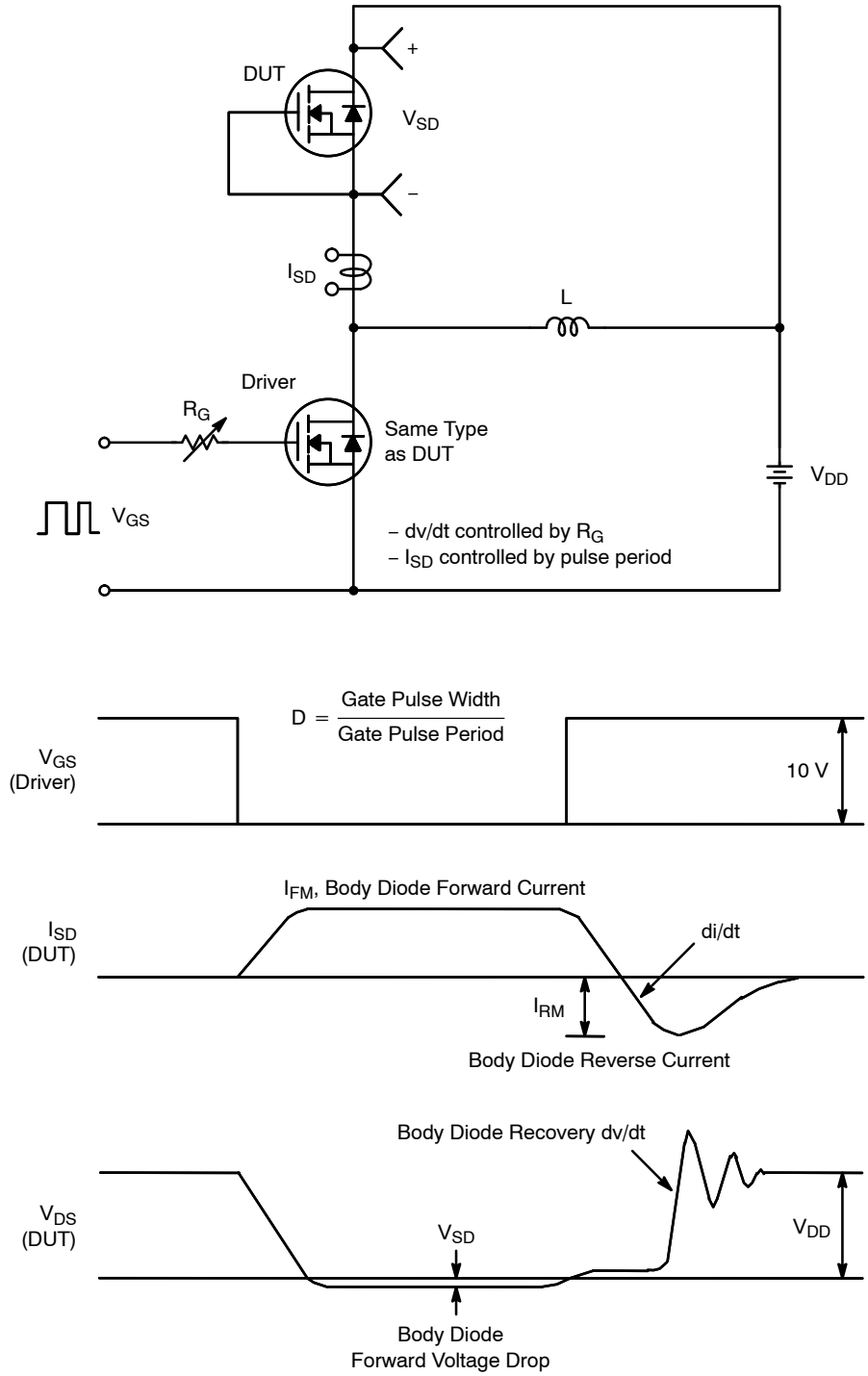


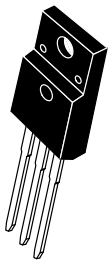
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

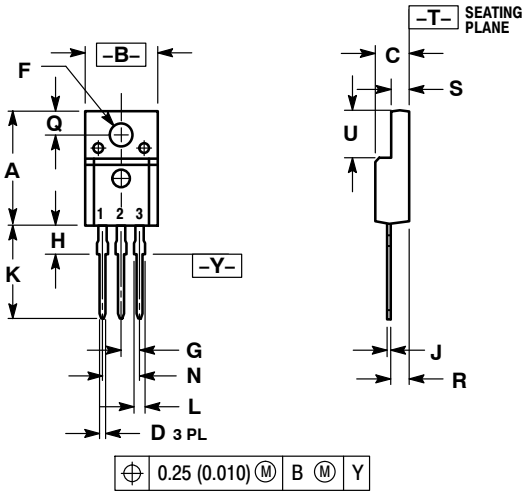
ON Semiconductor®

TO−220 FULLPAK
CASE 221D−03
ISSUE K

DATE 27 FEB 2009



SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. 221D−01 THRU 221D−02 OBSOLETE, NEW STANDARD 221D−03.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

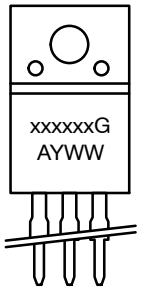
STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. CATHODE

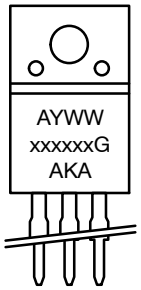
STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 6:
PIN 1. MT 1
2. MT 2
3. GATE

MARKING DIAGRAMS



Bipolar



Rectifier

xxxxxx	= Specific Device Code
G	= Pb−Free Package
A	= Assembly Location
Y	= Year
WW	= Work Week

A	= Assembly Location
Y	= Year
WW	= Work Week
xxxxxx	= Device Code
G	= Pb−Free Package
AKA	= Polarity Designator

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DESCRIPTION:	**TO−220 FULLPAK**	**PAGE 1 OF 1**

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