MOSFET – Power, Dual, N-Channel, Power Trench, Power Clip, Asymmetric
25 V

NTMFD1D4N02P1E

ON Semiconductor®

www.onsemi.com

Features
- Small Footprint (5x6mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These are Pb−free, Halogen Free / BFR Free and are RoHS Compliant

Typical Applications
- DC−DC Converters
- System Voltage Rails

FET	$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
Q1	25 V	3.3 mΩ @ 10 V	74 A
		4.2 mΩ @ 4.5 V	
Q2	25 V	1.1 mΩ @ 10 V	155 A
		1.33 mΩ @ 4.5 V	

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Q1	Q2	Unit
Drain−to−Source Voltage			V_{DSS}	25	25	V
Gate−to−Source Voltage			V_{GS}	+16V −12V	+16V −12V	V
Continuous Drain Current $R_{θJC}$ (Note 3)	Steady State	T_C = 25°C	I_D	74	155	A
		T_C = 85°C		53	112	
Power Dissipation $R_{θJC}$ (Note 3)		T_A = 25°C	P_D	25	41	W
Continuous Drain Current $R_{θJA}$ (Notes 1, 3)	Steady State	T_A = 25°C	I_D	20	36	A
		T_A = 85°C		14	26	
Power Dissipation $R_{θJA}$ (Notes 1, 3)		T_A = 25°C	P_D	2.1	2.3	W
Continuous Drain Current $R_{θJA}$ (Notes 2, 3)	Steady State	T_A = 25°C	I_D	13	24	A
		T_A = 85°C		10	17	
Power Dissipation $R_{θJA}$ (Notes 2, 3)		T_A = 25°C	P_D	0.96	1.0	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	325	552	A
Single Pulse Drain−to−Source Avalanche Energy Q1: I_L = 9.4 A_{pk}, L = 3 mH (Note 4) Q2: I_L = 20.1 A_{pk}, L = 3 mH (Note 4)			E_{AS}	134	604	mJ
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to 150		°C
Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s)			T_L	260		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

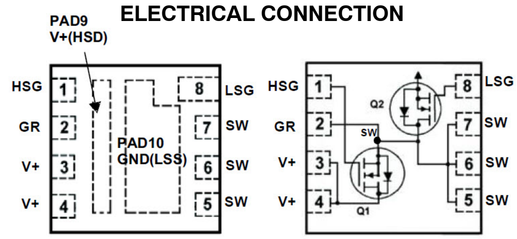
PQFN8
POWER CLIP
CASE 483AR

MARKING DIAGRAM

2EKN
AYWWZZ

2EKN = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

ELECTRICAL CONNECTION



ORDERING INFORMATION

Device	Package	Shipping†
NTMFD1D4N02P1E	PQFN8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

January, 2020 − Rev. 1

Publication Order Number:
NTMFD1D4N02P1E/D

Table 1. THERMAL RESISTANCE RATINGS

Parameter	Symbol	Q1 Max	Q2 Max	Units
Junction−to−Case − Steady State (Note 1, 3)	$R_{\theta JC}$	4.4	2.9	°C/W
Junction−to−Ambient − Steady State (Note 1, 3)	$R_{\theta JA}$	60	55	
Junction−to−Ambient − Steady State (Note 2, 3)	$R_{\theta JA}$	130	120	

1. Surface−mounted on FR4 board using 1 in^2 pad size, 2 oz Cu pad.
2. Surface−mounted on FR4 board using minimum pad size, 2 oz Cu pad.
3. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted. Actual continuous current will be limited by thermal & electro−mechanical application board design. $R_{\theta CA}$ is determined by the user's board design.
4. Q1 100% UIS tested at L = 0.1 mH, I_{AS} = 16.5 A.
   Q2 100% UIS tested at L = 0.1 mH, I_{AS} = 36 A.

Table 2. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Test Condition		FET	Min	Typ	Max	Unit
OFF CHARACTERISTICS								
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		Q1	25			V
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA		Q2	25			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}$ / T_J	I_D = 250 μA, ref to 25°C		Q1		16		mV/°C
		I_D = 1 mA, ref to 25°C		Q2		19		
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 20 V	T_J = 25°C	Q1			10	μA
				Q2			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = +16 V / −12 V		Q1			±100	nA
		V_{DS} = 0 V, V_{GS} = +16 V / −12 V		Q2			±100	
ON CHARACTERISTICS (Note 5)								
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		Q1	1.2	1.54	2.0	V
		V_{GS} = V_{DS}, I_D = 800 μA		Q2	1.2	1.55	2.0	
Threshold Temperature Coefficient	$V_{GS(TH)}$ / T_J	I_D = 250 μA, ref to 25°C		Q1		−4.3		mV/°C
		I_D = 800 μA, ref to 25°C		Q2		−4.4		
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A		Q1		2.6	3.3	mΩ
		V_{GS} = 4.5 V, I_D = 18 A				3.4	4.2	
		V_{GS} = 10 V, I_D = 37 A		Q2		0.81	1.1	
		V_{GS} = 4.5 V, I_D = 33 A				1.04	1.33	
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 20 A		Q1		125		
		V_{DS} = 5 V, I_D = 37 A		Q2		285		
Gate Resistance	R_G	T_A = 25°C		Q1		0.44		Ω
				Q2		0.6		
CHARGES & CAPACITANCES								
Input Capacitance	C_{ISS}	V_{GS} = 0 V, V_{DS} = 13 V, f = 1 MHz		Q1		1180		pF
				Q2		3603		
Output Capacitance	C_{OSS}			Q1		320		pF
				Q2		940		
Reverse Capacitance	C_{RSS}			Q1		22		pF
				Q2		64		

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
6. Switching characteristics are independent of operating junction temperatures

Table 2. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Test Condition		FET	Min	Typ	Max	Unit
CHARGES & CAPACITANCES								
Total Gate Charge	$Q_{G(TOT)}$	Q1: V_{GS} = 4.5V, V_{DS} = 13V, I_D = 20A Q2: V_{GS} = 4.5V, V_{DS} = 13V, I_D = 37A		Q1		7.2		nC
				Q2		21.5		
Gate−to−Drain Charge	Q_{GD}			Q1		1.35		nC
				Q2		3.9		
Gate−to−Source Charge	Q_{GS}			Q1		3.15		nC
				Q2		9.1		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 13 V, I_D = 20 A		Q1		16.4		nC
		V_{GS} = 10 V, V_{DS} = 13 V, I_D = 37 A		Q2		48.6		
SWITCHING CHARACTERISTICS, VGS = 4.5 V (Note 6)								
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V Q1: I_D = 20 A, V_{DD} = 13 V, R_G = 6Ω Q2: I_D = 37 A, V_{DD} = 13 V, R_G = 6Ω		Q1		11.6		ns
				Q2		21.4		
Rise Time	$t_{r(ON)}$			Q1		2.7		ns
				Q2		8.7		
Turn−Off Delay Time	$t_{d(OFF)}$			Q1		15.6		ns
				Q2		30.7		
Fall Time	t_f			Q1		3.2		ns
				Q2		8.5		
SWITCHING CHARACTERISTICS, VGS = 10 V (Note 6)								
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V Q1: I_D = 20 A, V_{DD} = 13 V, R_G = 6Ω Q2: I_D = 37 A, V_{DD} = 13 V, R_G = 6Ω		Q1		7.9		ns
				Q2		10.2		
Rise Time	$t_{r(ON)}$			Q1		1.1		ns
				Q2		3.3		
Turn−Off Delay Time	$t_{d(OFF)}$			Q1		21.3		ns
				Q2		48.9		
Fall Time	t_f			Q1		2.2		ns
				Q2		7.4		
SOURCE−TO−DRAIN DIODE CHARACTERISTICS								
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 20 A	T_J = 25°C	Q1		0.8	1.2	V
			T_J = 125°C			0.7		
		V_{GS} = 0 V, I_S = 37 A	T_J = 25°C	Q2		0.8	1.2	
			T_J = 125°C			0.65		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, Q1: I_S = 20 A, dI/dt = 100 A/μs Q2: I_S = 37 A, dI/dt = 300 A/μs		Q1		21.4		ns
				Q2		36.5		
Reverse Recovery Charge	Q_{RR}			Q1		8.3		nC
				Q2		21.9		

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
6. Switching characteristics are independent of operating junction temperatures

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS FOR Q1

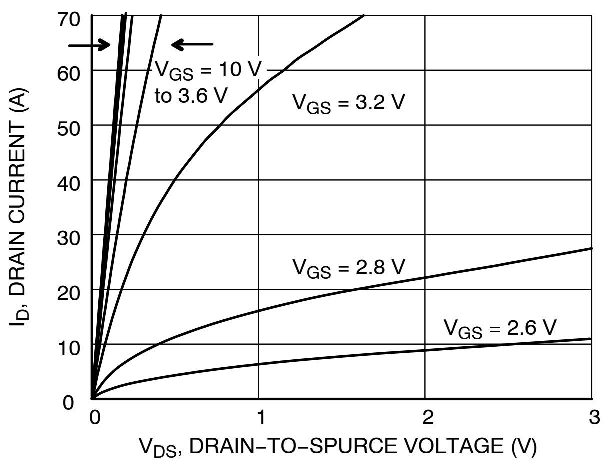


Figure 1. On−Region Characteristics

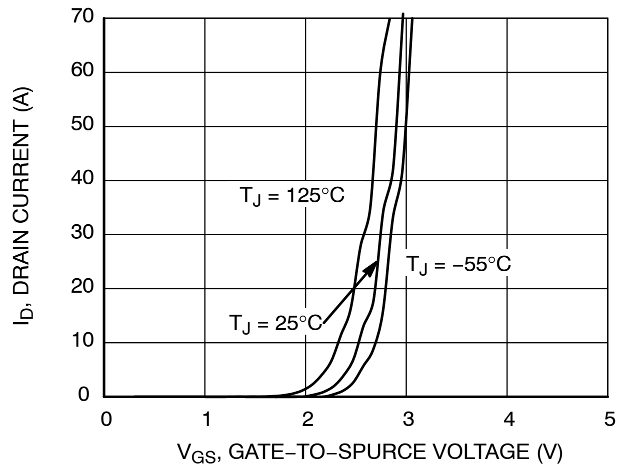


Figure 2. Transfer Characteristics

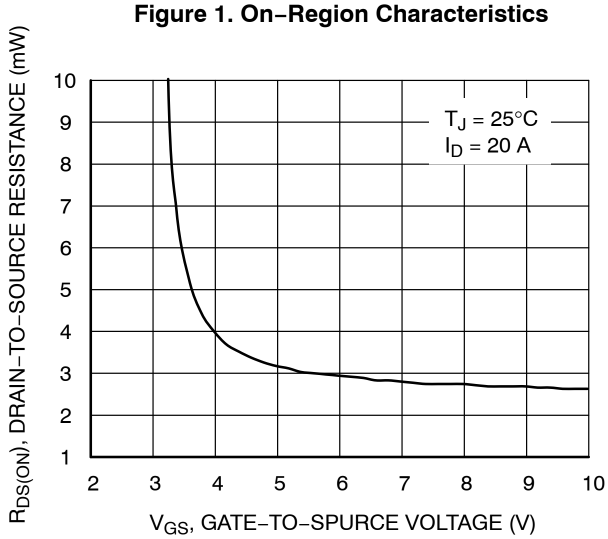


Figure 3. On−Resistance vs. Gate−to−Source Voltage

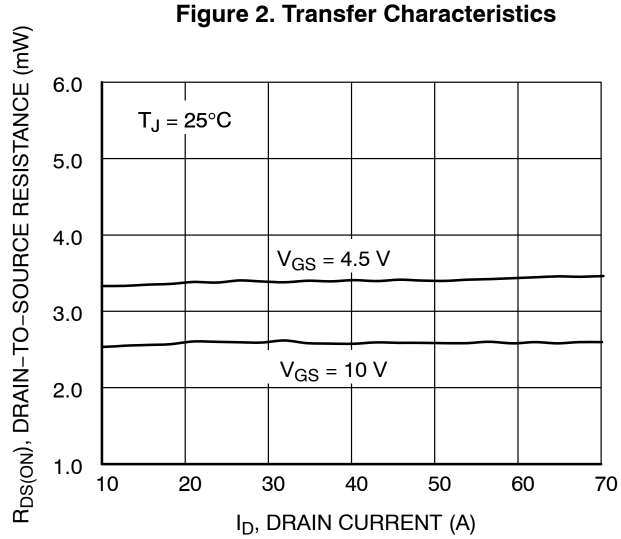


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

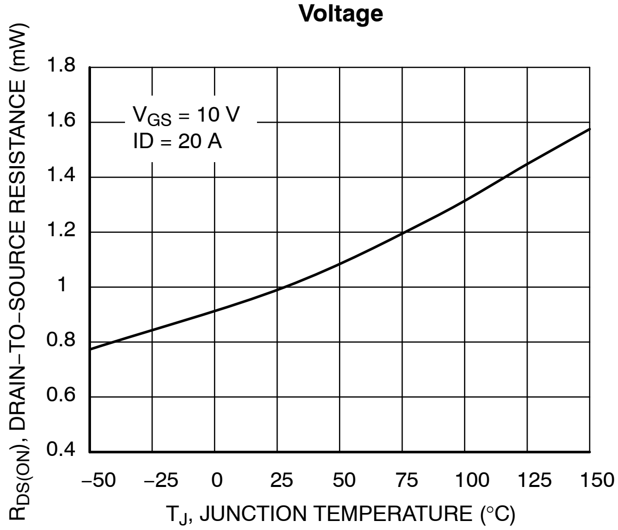


Figure 5. On−Resistance Variation with Temperature

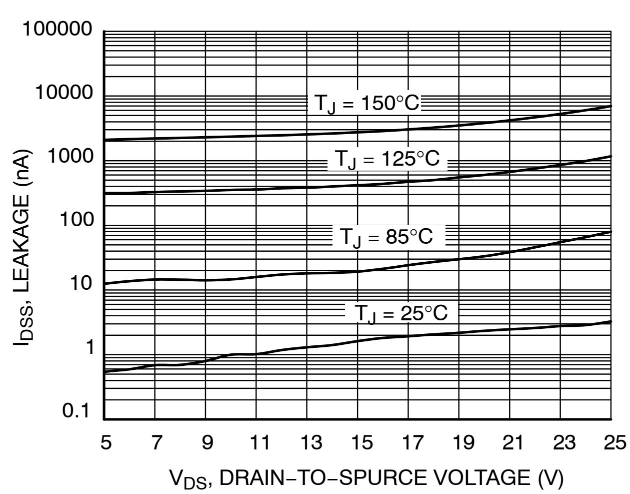


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS FOR Q1 (continued)

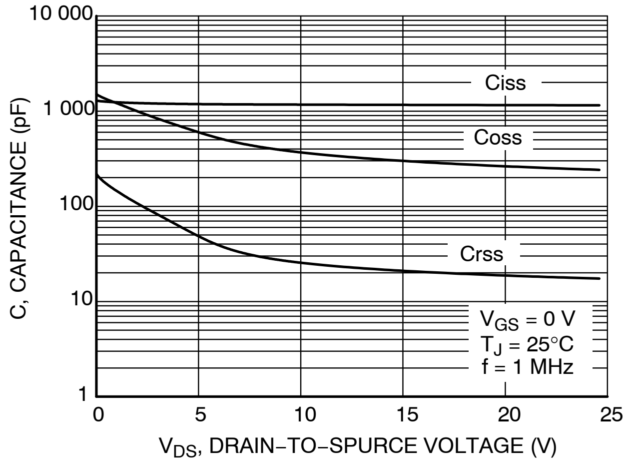


Figure 7. Capacitance Variation

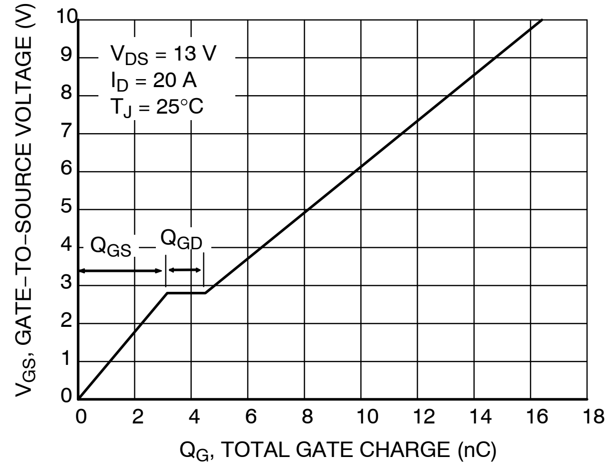


Figure 8. Gate−to−Source vs. Total Charge

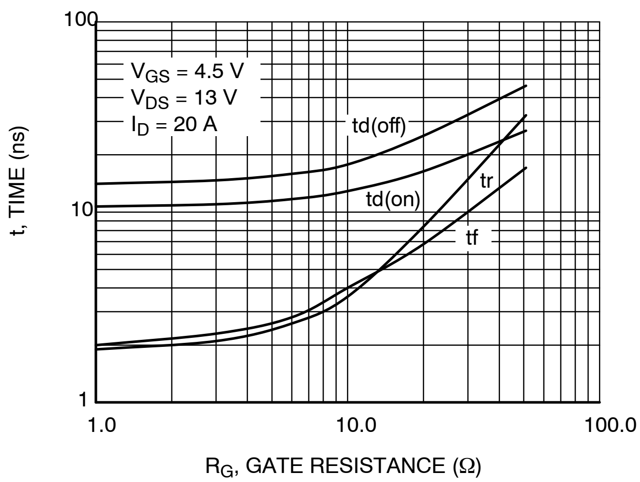


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

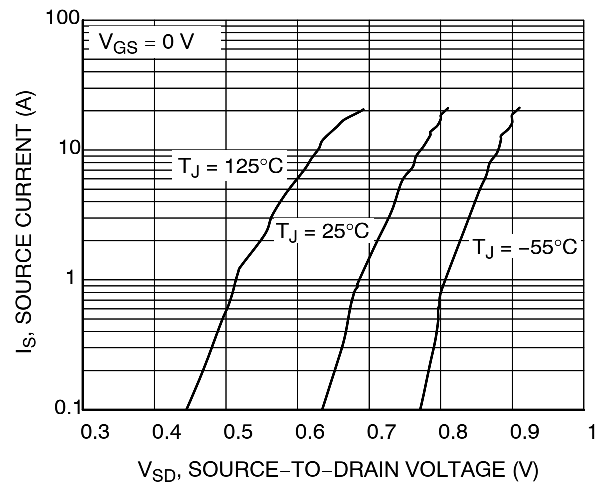


Figure 10. Diode Forward Voltage vs. Current

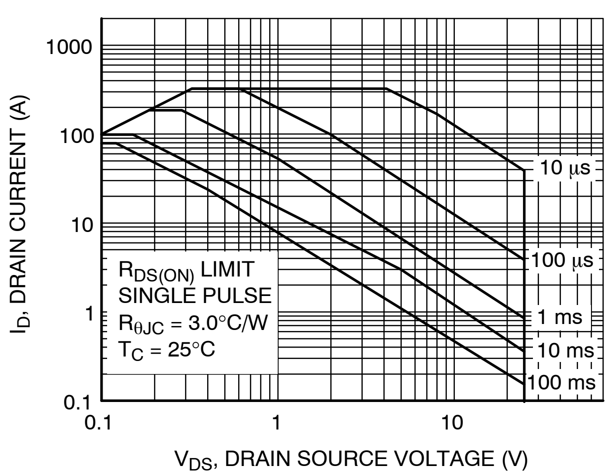


Figure 11. Maximum Rated Forward Biased Safe Operationg Area

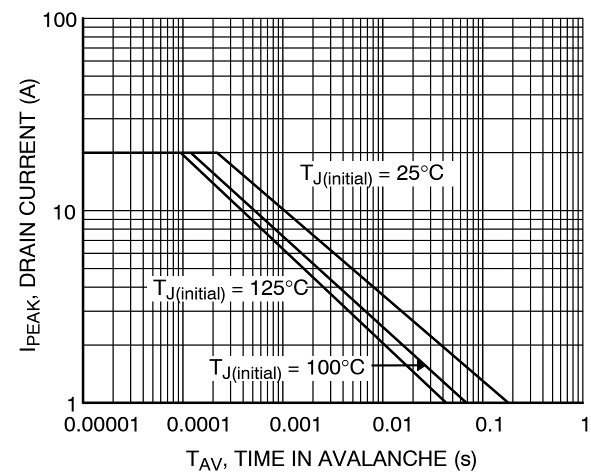


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS FOR Q1 (continued)

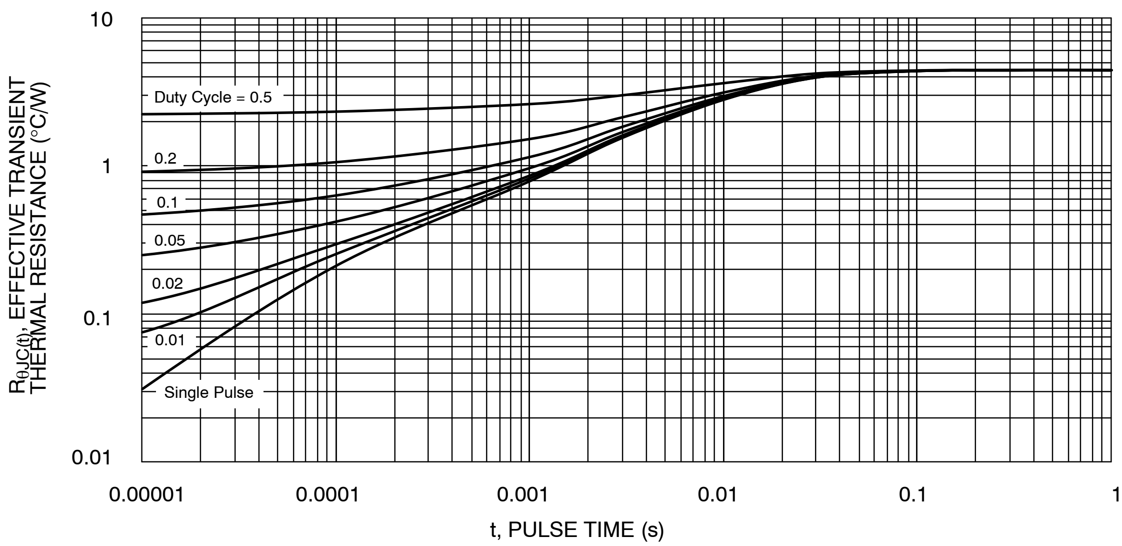


Figure 13. Thermal Response

TYPICAL CHARACTERISTICS FOR Q2

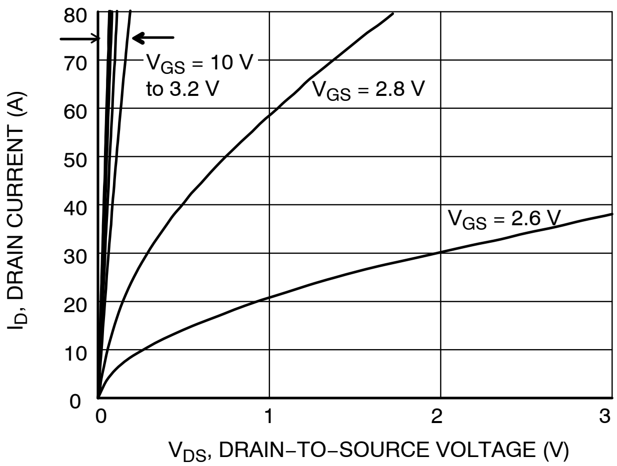


Figure 14. On−Region Characteristics

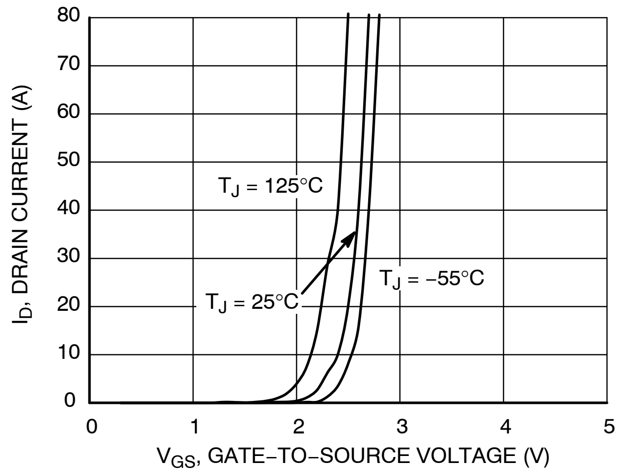


Figure 15. Transfer Characteristics

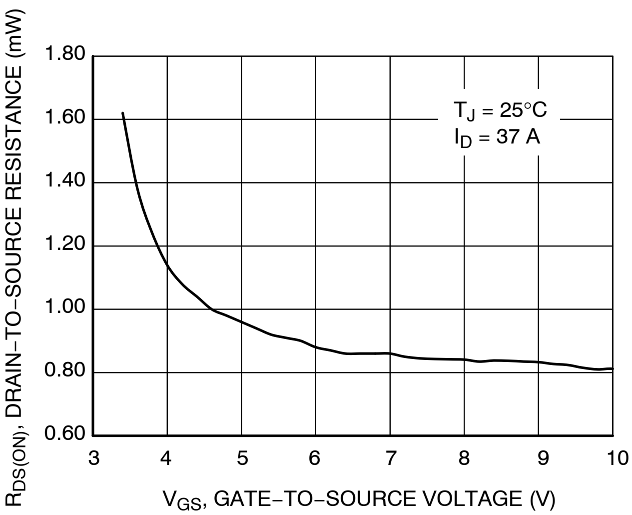


Figure 16. On−Resistance vs. Gate−to−Source Voltage

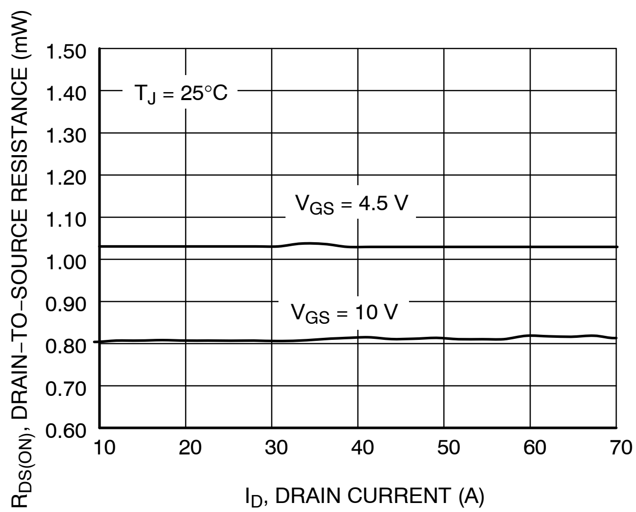


Figure 17. On−Resistance vs. Drain Current and Gate Voltage

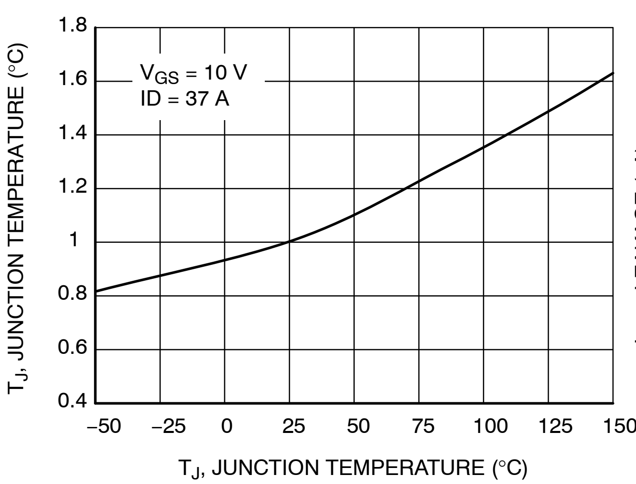


Figure 18. On−Resistance Variation with Temperature

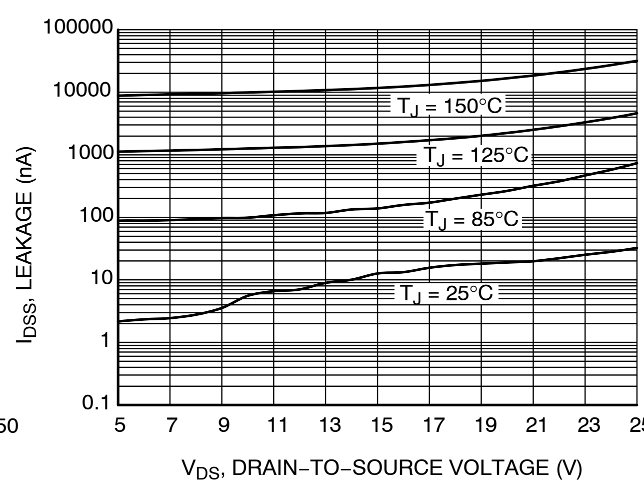


Figure 19. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS FOR Q2 (continued)

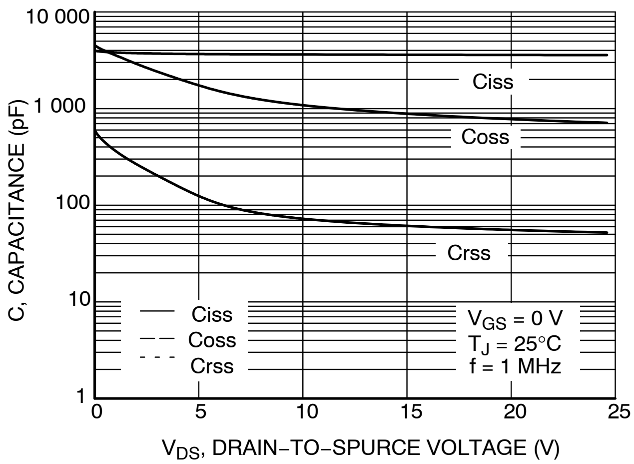


Figure 20. Capacitance Variation

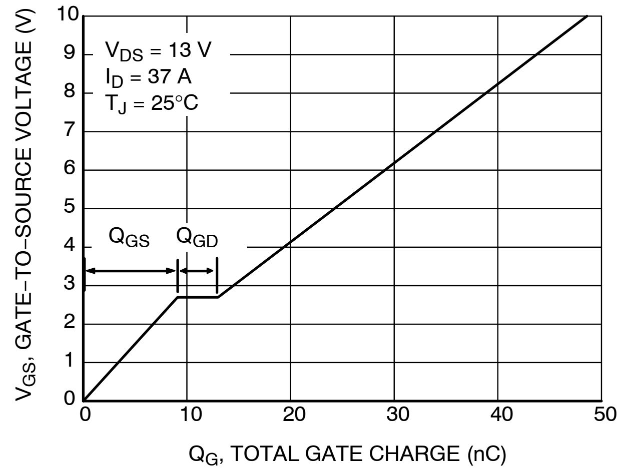


Figure 21. Gate−to−Source vs. Total Charge

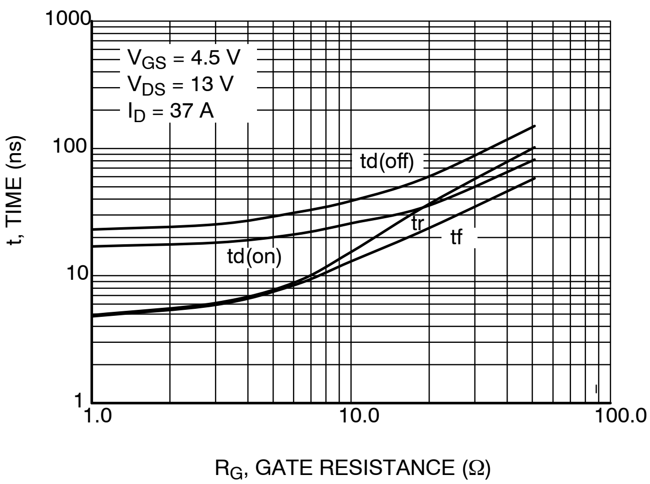


Figure 22. Resistive Switching Time Variation vs. Gate Resistance

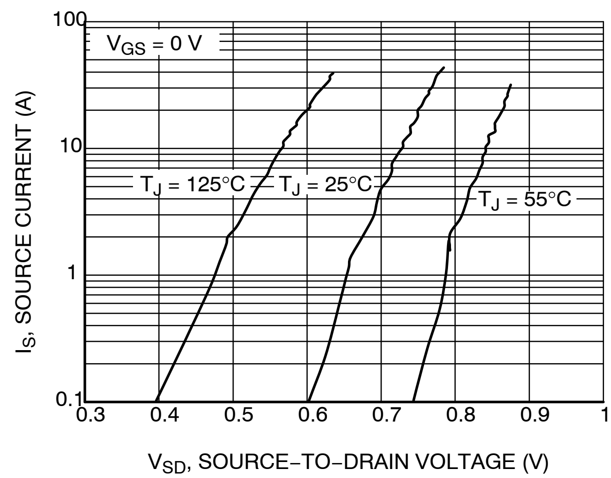


Figure 23. Diode Forward Voltage vs. Current

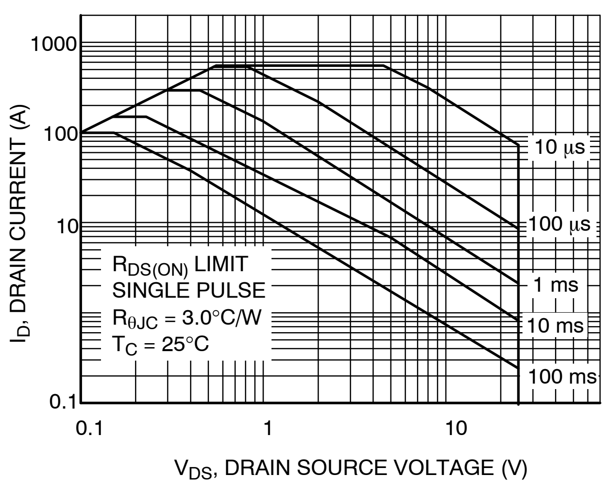


Figure 24. Maximum Rated Forward Biased Safe Operating Area

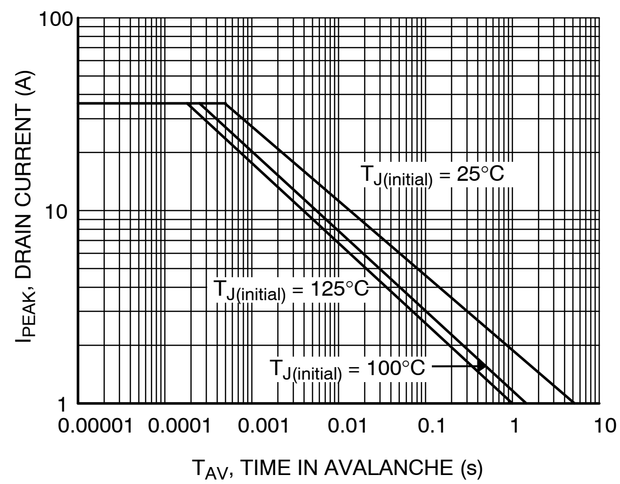


Figure 25. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS FOR Q2 (continued)

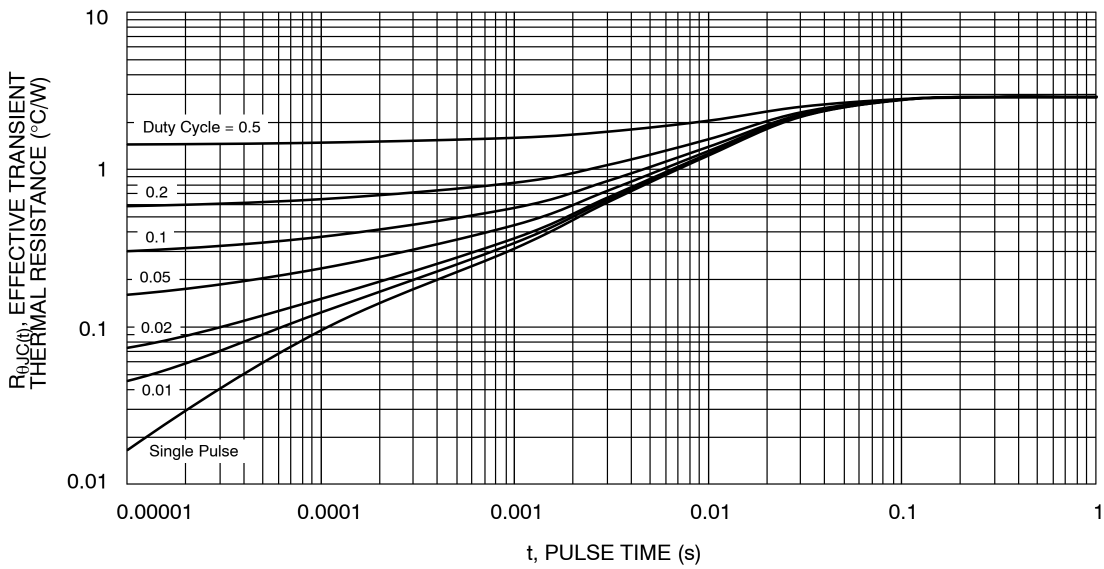
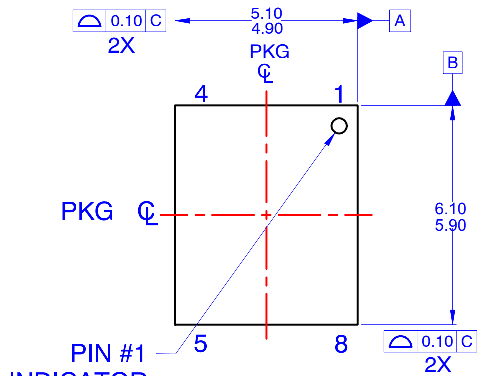


Figure 26. Thermal Response

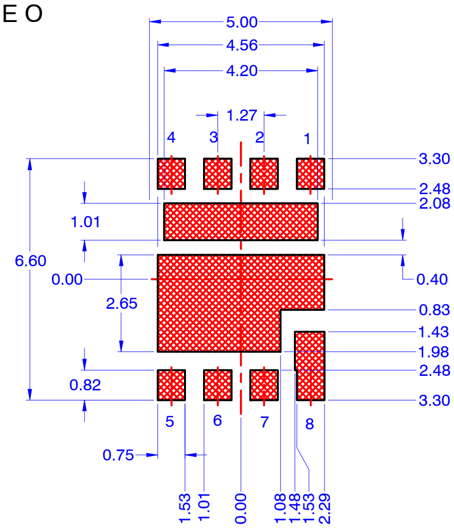
PowerTrench is a registered trademark of Semiconductor Components Industries, LLC.

PACKAGE DIMENSIONS

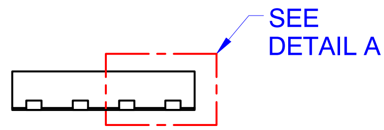
PQFN8 5X6, 1.27P
CASE 483AR
ISSUE O



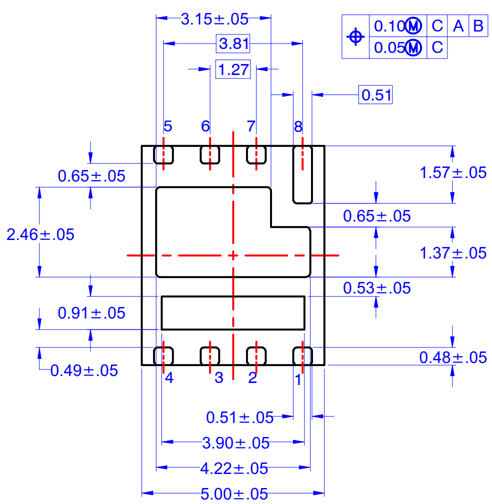
TOP VIEW



RECOMMENDED LAND PATTERN



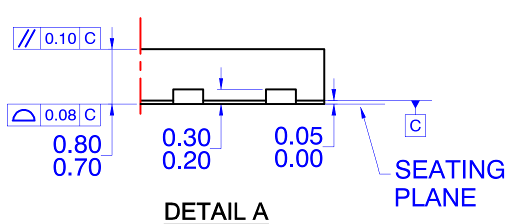
SIDE VIEW



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO−229, DATED 11/2001.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.



DETAIL A
(SCALE: 2X)

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

TECHNICAL SUPPORT
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Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
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