

MOSFET - Power, N-Channel, SUPERFET[®] V, Easy Drive 600 V, 120 mΩ, 28 A



ON Semiconductor[®]

www.onsemi.com

NTHL120N60S5Z

Description

SUPERFET V MOSFET Easy Drive series combines excellent switching performance without sacrificing ease of use and EMI issues for both hard and soft switching topologies.

Features

- 650 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 96\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 39\text{ nC}$)
- Low Time Related Output Capacitance (Typ. $C_{OSS(tr)} = 547\text{ pF}$)
- 100% Avalanche Tested
- Pb-Free, Halogen Free/BFR Free and RoHS Compliant

Applications

- Telecom / Server Power Supplies
- Industrial Power Supplies
- EV Charger
- UPS / Solar

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, Unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	600	V
V_{GSS}	Gate to Source Voltage	- DC	± 20
		- AC ($f > 1\text{ Hz}$)	± 20
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	28*
		- Continuous ($T_C = 100^\circ\text{C}$)	17*
I_{DM}	Drain Current	81*	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	191	mJ
I_{AS}	Avalanche Current (Note 2)	4.6	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	1.6	mJ
dv/dt	MOSFET dv/dt	120	V/ns
	Peak Diode Recovery dv/dt (Note 3)	50	
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	160
		- Derate Above 25°C	1.28
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

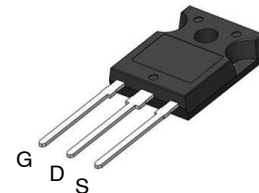
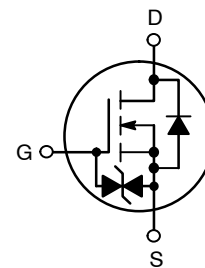
*Drain current limited by maximum junction temperature.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $I_{AS} = 4.6\text{ A}$, $R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 11.5\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq 400\text{ V}$, starting $T_J = 25^\circ\text{C}$.

THERMAL CHARACTERISTICS

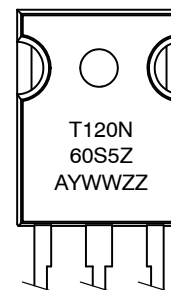
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.78	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

V_{DSS}	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
600 V	120 mΩ @ 10 V	28 A



TO-247 Long Leads
CASE 340CX

MARKING DIAGRAM



T120N60S5Z = Specific Device Code
 A = Assembly Location
 YWW = Data Code (Year & Week)
 ZZ = Assembly Lot

ORDERING INFORMATION

Device	Package	Shipping
NTHL120N60S5Z	TO-247	30 Units / Tube

NTHL120N60S5Z

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$	600	–	–	V
		$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 150^\circ\text{C}$	650	–	–	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, Referenced to 25°C	–	0.6		V/ $^\circ\text{C}$
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	–	–	1	μA
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	–	1	–	
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	–	–	± 5	μA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 2.2\text{ mA}$	2.4	–	4.0	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 11.5\text{ A}$	–	96	120	m Ω
g _{FS}	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 11.5\text{ A}$	–	17.1	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, f = 250\text{ kHz}$	–	2088	–	pF
C _{oss}	Output Capacitance		–	35	–	pF
C _{oss(tr.)}	Time Related Output Capacitance	$I_D = \text{Constant}, V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	–	547	–	pF
C _{oss(er.)}	Energy Related Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	–	59	–	pF
Q _{g(tot)}	Total Gate Charge	$V_{DD} = 400\text{ V}, I_D = 11.5\text{ A}, V_{GS} = 10\text{ V}$	–	40	–	nC
Q _{gs}	Gate to Source Charge		–	9	–	nC
Q _{gd}	Gate to Drain Charge		–	11	–	nC
ESR	Equivalent Series Resistance		$f = 1\text{ MHz}$	–	3.5	–

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	$V_{DD} = 400\text{ V}, I_D = 11.5\text{ A}, V_{GS} = 10\text{ V}, R_g = 7.5\ \Omega$	–	23	–	ns
t _r	Turn-On Rise Time		–	13	–	ns
t _{d(off)}	Turn-Off Delay Time		–	78	–	ns
t _f	Turn-Off Fall Time		–	3	–	ns

SOURCE-DRAIN DIODE CHARACTERISTICS

I _S	Maximum Continuous Source to Drain Diode Forward Current		–	–	28	A
I _{SM}	Maximum Pulsed Source to Drain Diode Forward Current		–	–	81	A
V _{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 11.5\text{ A}$	–	–	1.2	V
t _{rr}	Reverse Recovery Time	$V_{DD} = 400\text{ V}, I_{SD} = 11.5\text{ A}, di_F/dt = 100\text{ A}/\mu\text{s}$	–	227	–	ns
Q _{rr}	Reverse Recovery Charge		–	3.2	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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TYPICAL CHARACTERISTICS

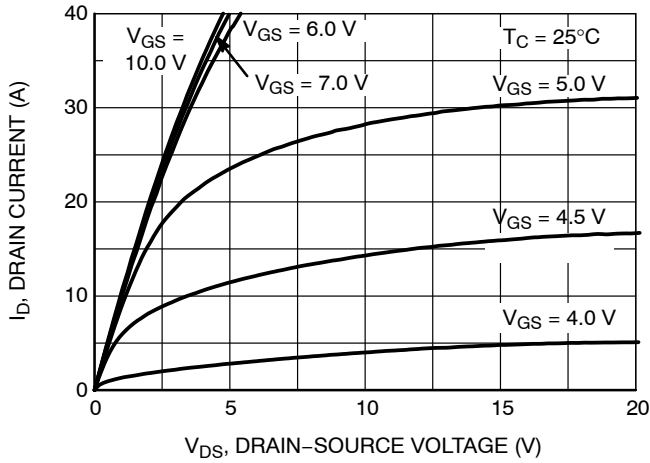


Figure 1. On-Region Characteristics

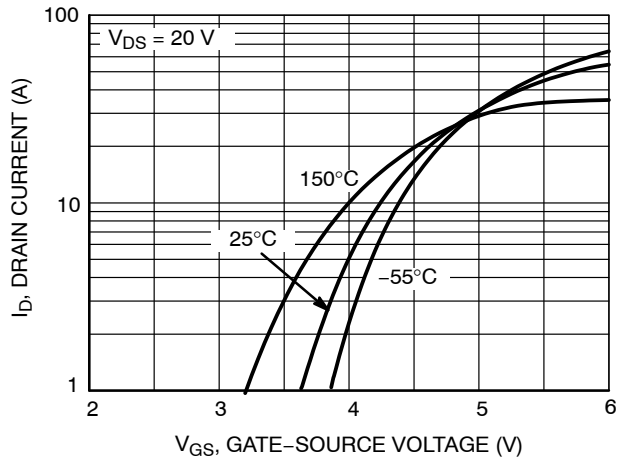


Figure 2. Transfer Characteristics

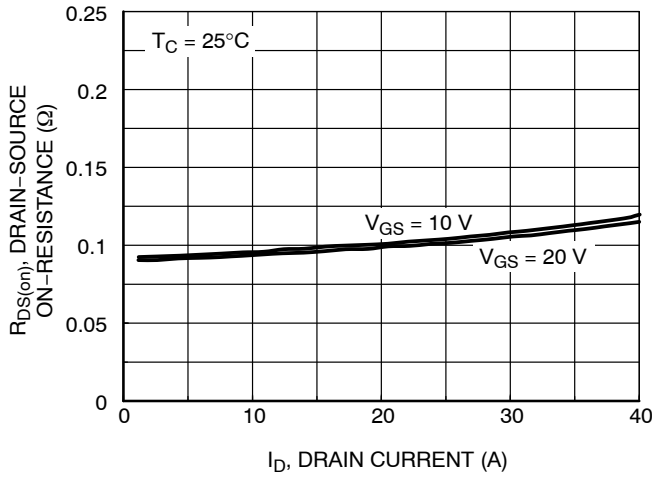


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

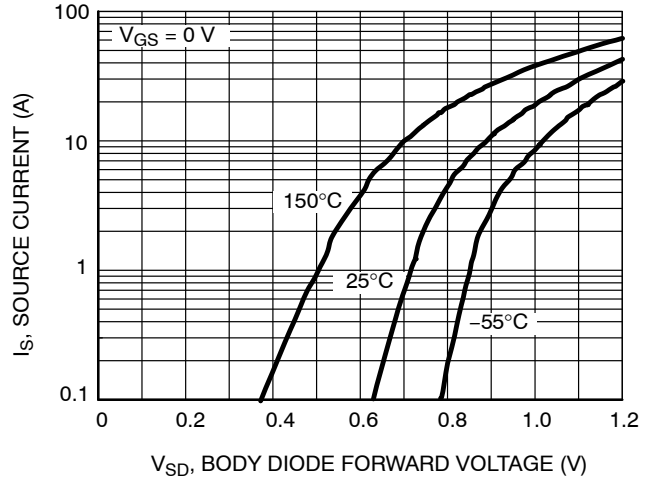


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

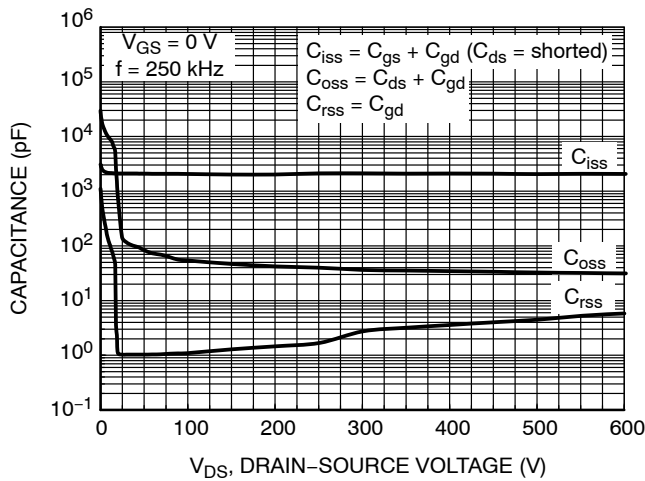


Figure 5. Capacitance Characteristics

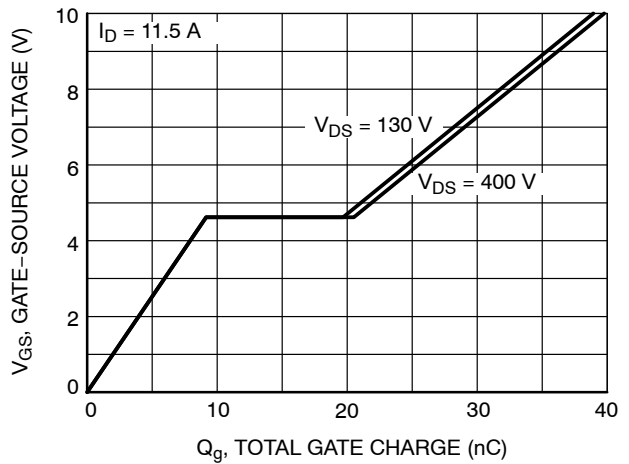


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

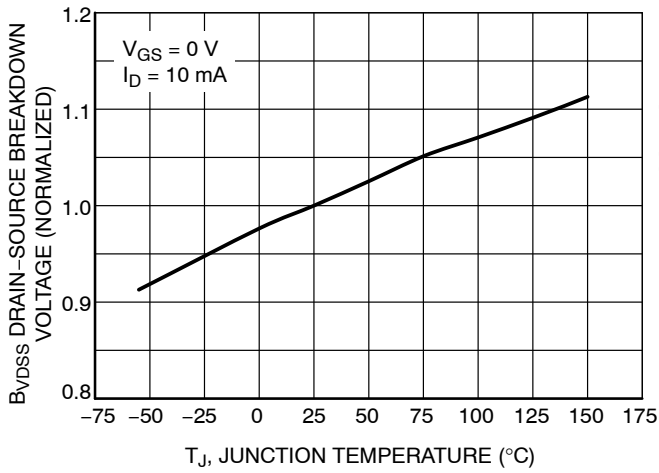


Figure 7. Breakdown Voltage Variation vs. Temperature

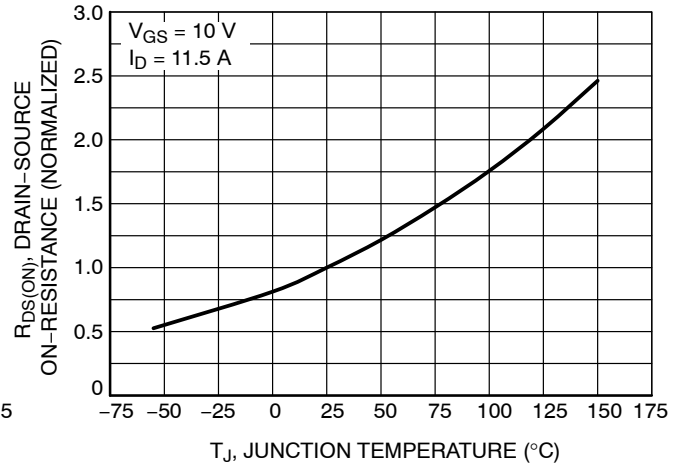


Figure 8. On-Resistance Variation vs. Temperature

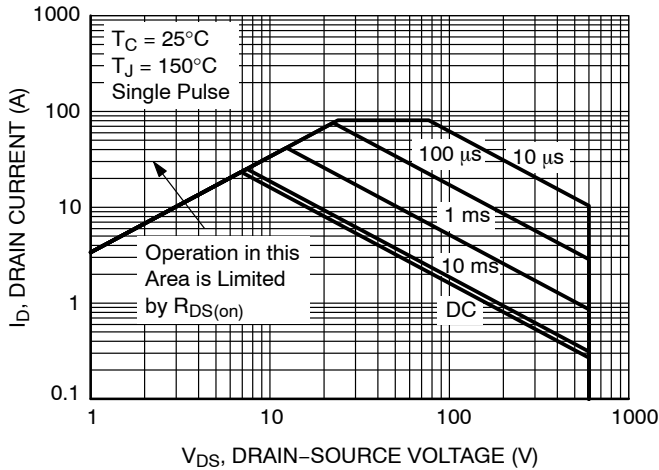


Figure 9. Maximum Safe Operating Area

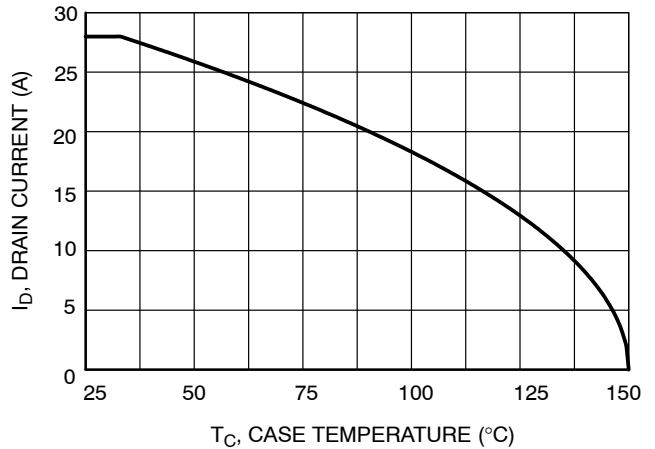


Figure 10. Maximum Drain Current vs. Case Temperature

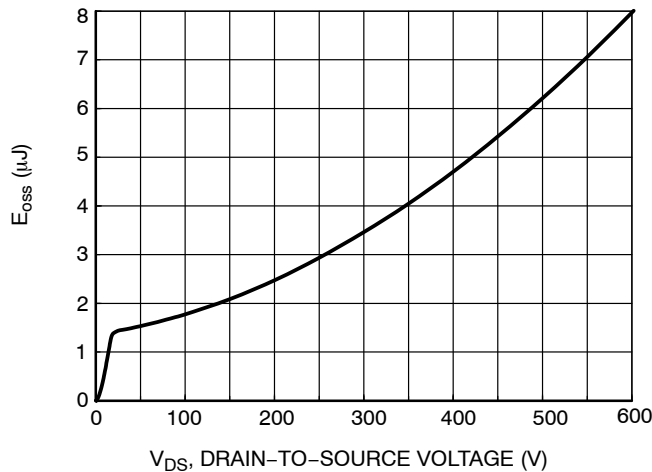


Figure 11. E_{OSS} vs. Drain to Source Voltage

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TYPICAL CHARACTERISTICS

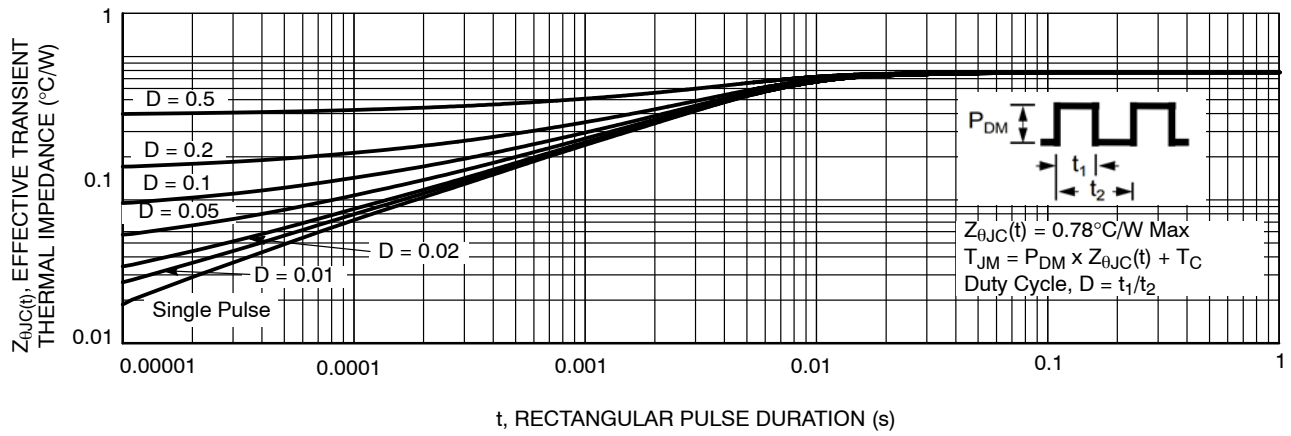


Figure 12. Thermal Response

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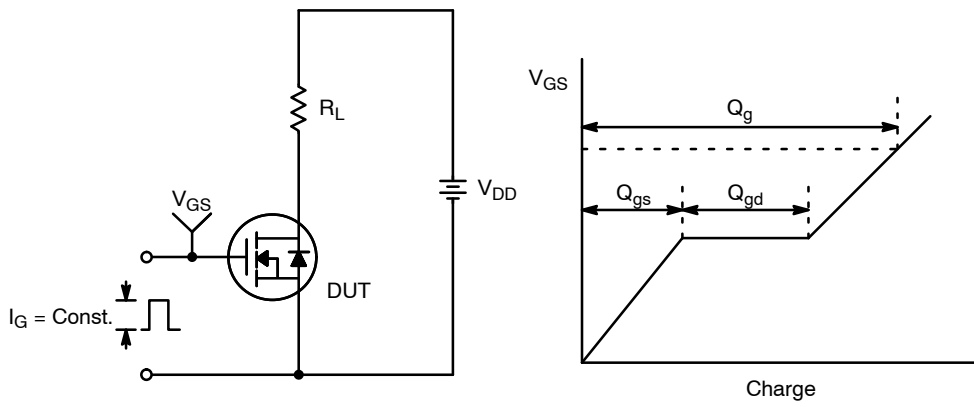


Figure 13. Gate Charge Test Circuit & Waveform

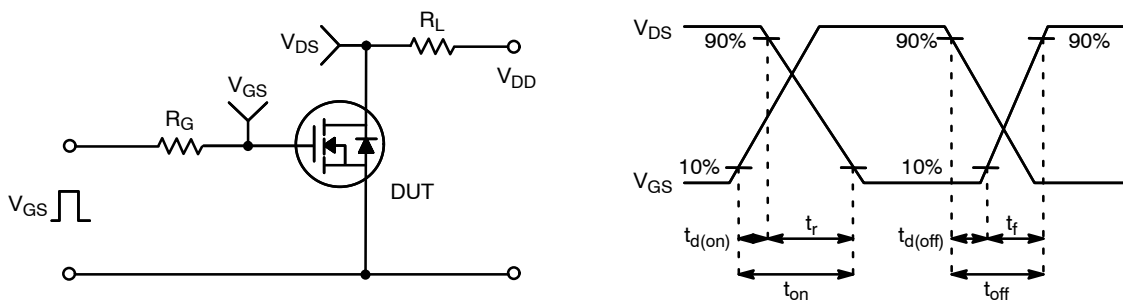


Figure 14. Resistive Switching Test Circuit & Waveforms

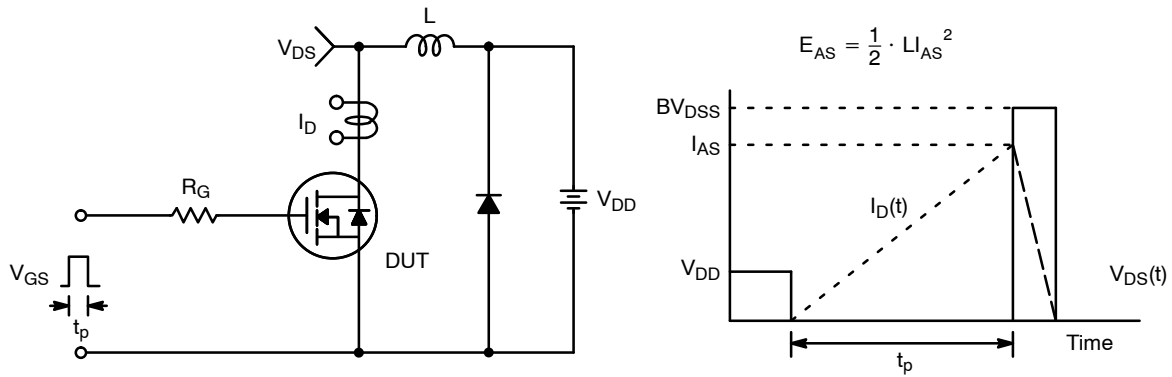


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



TO-247-3LD
CASE 340CX
ISSUE A

DATE 06 JUL 2020



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
- D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
- E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
D	20.32	20.57	20.82
E	15.37	15.62	15.87
E2	4.96	5.08	5.20
e	~	5.56	~
L	19.75	20.00	20.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
Q	5.34	5.46	5.58
S	5.34	5.46	5.58
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D1	13.08	~	~
D2	0.51	0.93	1.35
E1	12.81	~	~
ØP1	6.60	6.80	7.00

GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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