Isolated High Current IGBT Gate Driver

Product Preview

NCD57090A, NCD57090B, NCD57090C, NCD57090D, NCD57090E, NCD57090F

NCD57090A, NCD57090B, NCD57090C, NCD57090D, NCD57090E and NCD57090F are high−current single channel IGBT gate drivers with 5 kVrms internal galvanic isolation, designed for high system efficiency and reliability in high power applications. The devices accept complementary inputs and depending on the pin configuration, offer options such as Active Miller Clamp (NCD57090A/D/F), negative power supply (NCD57090B) and separate high and low (OUTH and OUTL) driver outputs (NCD57090C/E) for system design convenience. NCD57090 (A/B/C/D/E/F) accommodate wide range of input bias voltage and signal levels from 3.3 V to 20 V. NCD57090 (A/B/C/D/E/F) are available in wide−body SOIC−8 package.

Features

- High Peak Output Current (+8A/−8 A)
- Low Clamp Voltage Drop Eliminates the Need of Negative Power Supply to Prevent Spurious Gate Turn−on (NCD57090A/D/F)
- Short Propagation Delays with Accurate Matching
- IGBT Gate Clamping during Short Circuit
- IGBT Gate Active Pull Down
- Tight UVLO Thresholds for Bias Flexibility
- Wide Bias Voltage Range including Negative VEE2 (NCD57090B)
- 3.3 V, 5 V, and 15 V Logic Input
- 5 kVrms Galvanic Isolation
- High Transient Immunity
- High Electromagnetic Immunity
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Motor Control
- Uninterruptible Power Supplies (UPS)
- Industrial Power Supplies
- Solar Inverters

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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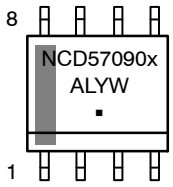
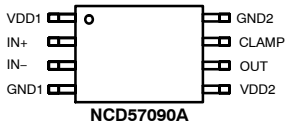
SOIC−8 WB
CASE 751−07

MARKING DIAGRAM



NCD57090	= Specific Device Code
x	= A/B/C/D/E/F
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS

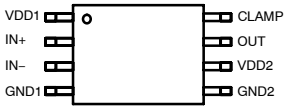


NCD57090A

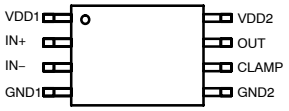
NCD57090B

NCD57090C

NCD57090D



NCD57090E



NCD57090F

ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

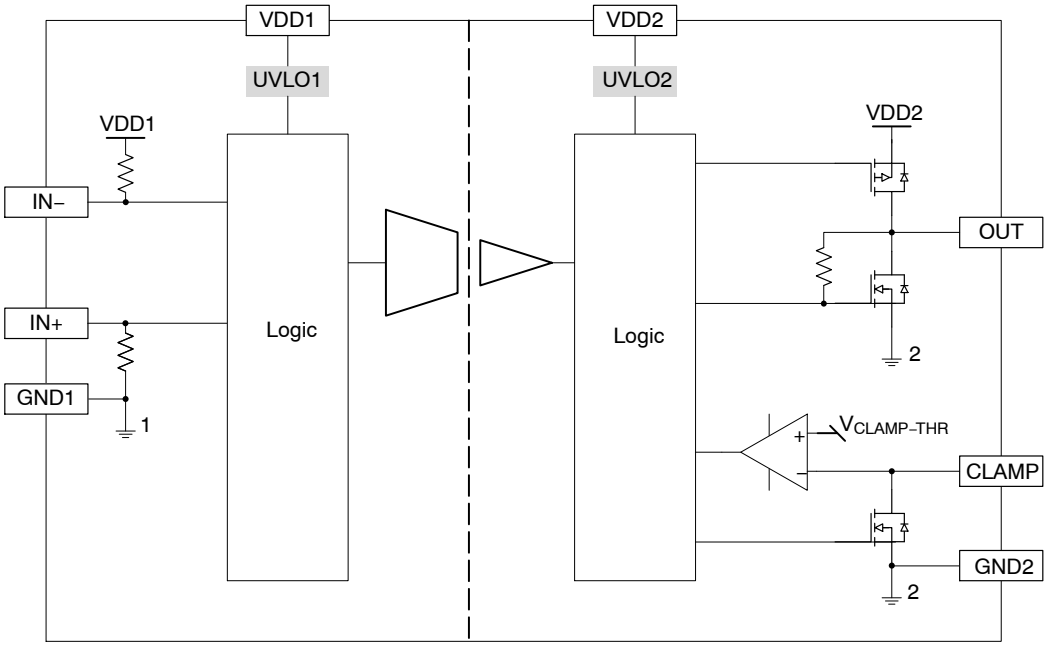


Figure 1. Simplified Block Diagram, NCD57090A/D/F

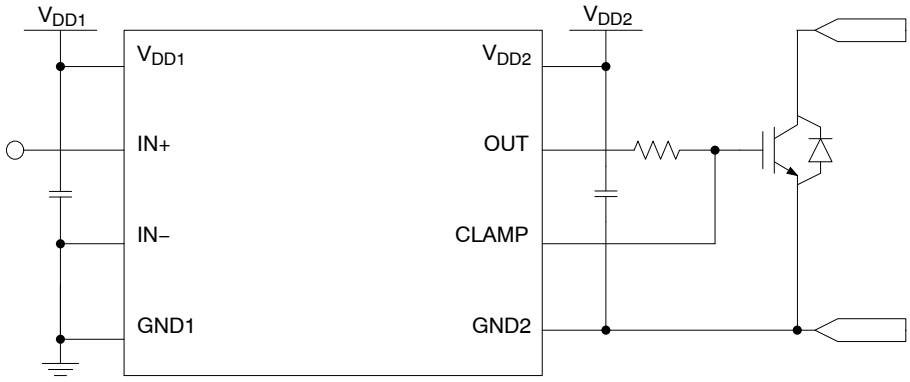


Figure 2. Simplified Application Schematics, NCD57090A/D/F

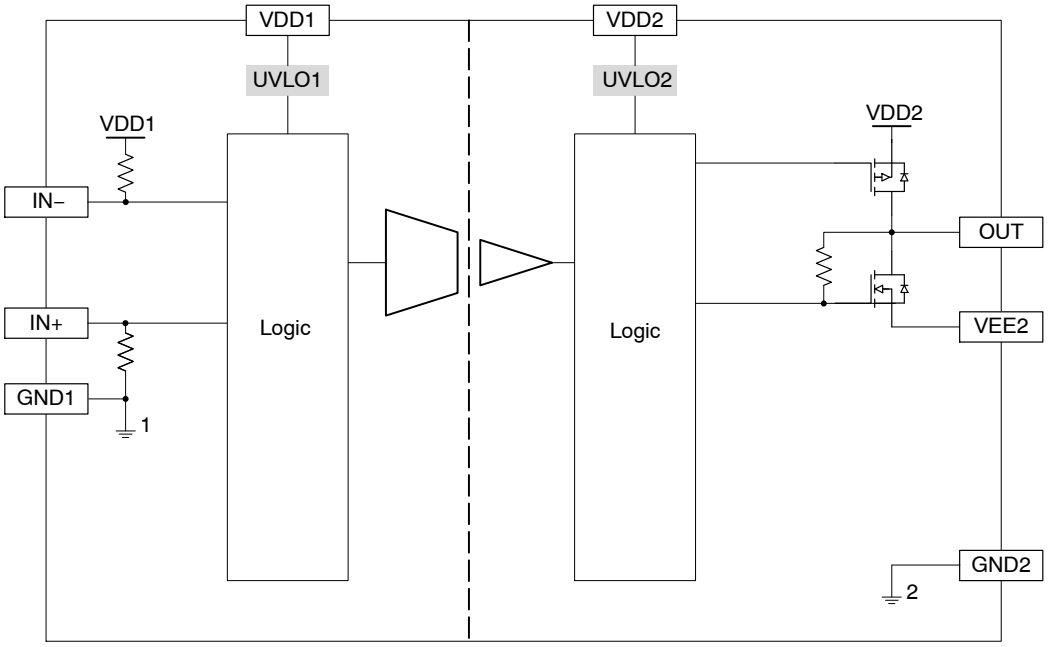


Figure 3. Simplified Block Diagram, NCD57090B

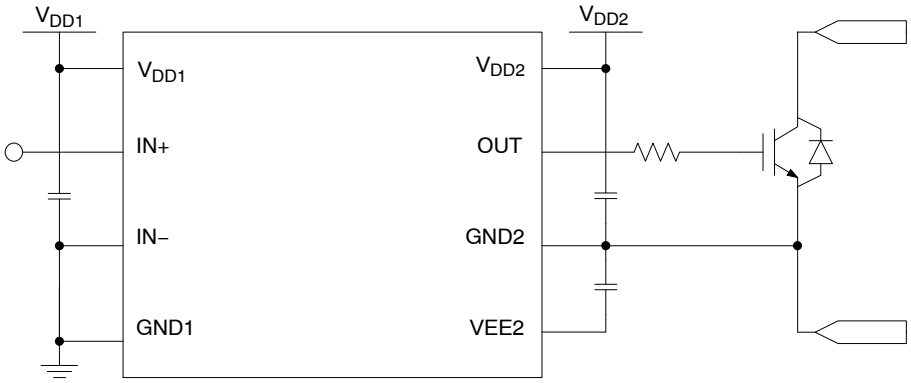


Figure 4. Simplified Application Schematics, NCD57090B

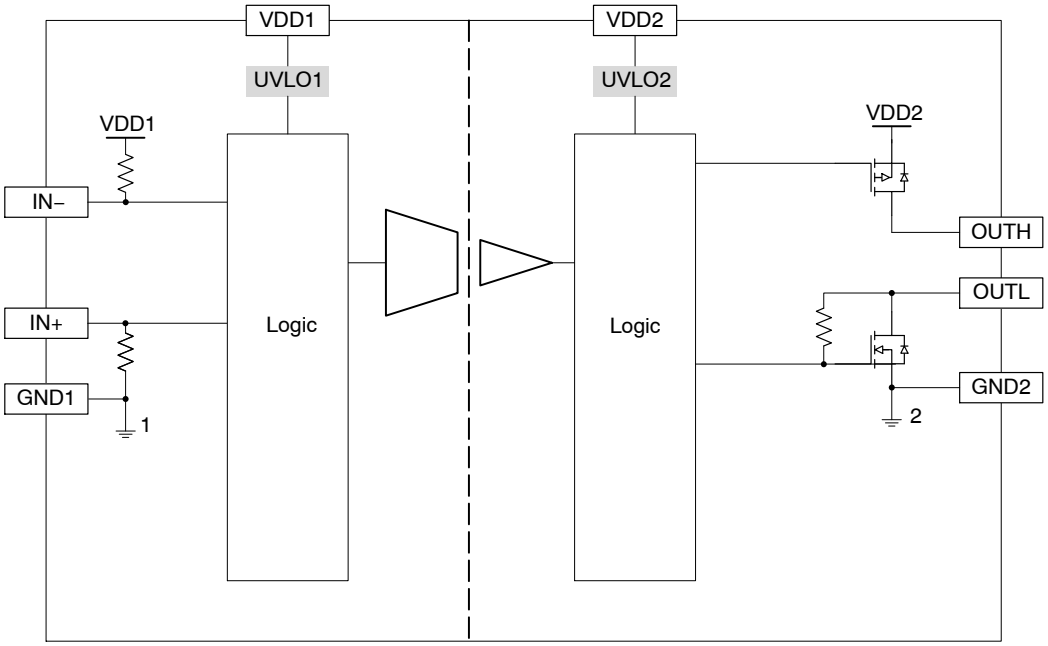


Figure 5. Simplified Block Diagram, NCD57090C/E

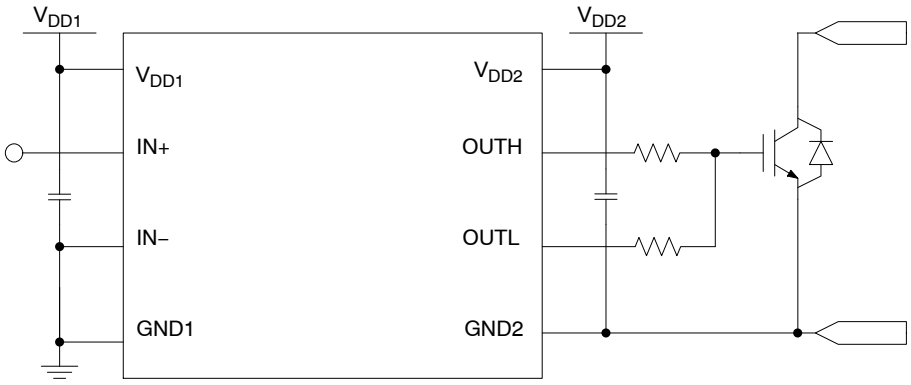


Figure 6. Simplified Application Schematics, NCD57090C/E

Table 1. FUNCTION DESCRIPTION

Pin Name	No.	I/O	Description
V_{DD1}	1	Power	Input side power supply. A good quality bypassing capacitor is required from this pin to GND1 and should be placed close to the pins for best results. The under voltage lockout (UVLO) circuit enables the device to operate at power on when a typical supply voltage higher than $V_{UVLO1-OUT-ON}$ is present. Please see Figure 7 for more details.
IN+	2	I	Non inverted gate driver input. It is internally clamped to V_{DD1} and has a pull−down resistor of 50 kΩ to ensure that output is low in the absence of an input signal. A minimum positive going pulse−width is required at IN+ before OUT or OUTH/OUTL responds.
IN−	3	I	Inverted gate driver input. It is internally clamped to V_{DD1} and has a pull−up resistor of 50 kΩ to ensure that output is low in the absence of an input signal. A minimum negative going pulse−width is required at IN− before OUT or OUTH/ OUTL responds.
GND1	4	Power	Input side ground reference.
V_{DD2}	5	Power	Output side positive power supply. The operating range for this pin is from UVLO2 to its maximum allowed value. A good quality bypassing capacitor is required from this pin to GND2 and should be placed close to the pins for best results.
GND2 (NCD57090A, NCD57090C)	8	Power	Output side gate drive reference connecting to IGBT emitter or FET source.
GND2 (NCD57090B)	7		
GND2 (NCD57090D, NCD57090E, NCD57090F)	5		
OUT (NCD57090A, NCD57090B)	6	O	Driver output that provides the appropriate drive voltage and source/sink current to the IGBT/FET gate. OUT is actively pulled low during start−up.
OUT (NCD57090D, NCD57090F)	7		
OUTH (NCD57090C)	6	O	Driver high output that provides the appropriate drive voltage and source current to the IGBT/FET gate.
OUTH (NCD57090E)	7		
OUTL (NCD57090C)	7	O	Driver low output that provides the appropriate drive voltage and sink current to the IGBT/FET gate. OUTL is actively pulled low during start−up.
OUTL (NCD57090E)	8		
CLAMP (NCD57090A)	7	O	Provides clamping for the IGBT/FET gate during the off period to protect it from parasitic turn−on. Its internal N FET is turned on when the voltage of this pin falls below $V_{CLAMP-THR}$. It is to be tied directly to IGBT/FET gate with minimum trace length for best results.
CLAMP (NCD57090D)	8		
CLAMP (NCD57090F)	6		
V_{EE2} (NCD57090B)	8	Power	Output side negative power supply. A good quality bypassing capacitor is required from this pin to GND2 and should be placed close to the pins for best results.

Table 2. ABSOLUTE MAXIMUM RATINGS (Note 1) Over operating free−air temperature range unless otherwise noted.

Parameter	Symbol	Minimum	Maximum	Unit
Supply voltage, input side	V_{DD1}−GND1	−0.3	22	V
Positive Power Supply, output side	V_{DD2}−GND2	−0.3	32	V
Negative Power Supply, output side	V_{EE2}−GND2	−18	0.3	V
Differential Power Supply, output side (NCD57090B)	V_{DD2}−V_{EE2} (V_{MAX2})	0	36	V
Gate−driver output high voltage NCD57090A/B//D/F NCD57090C/E	 V_{OUT} − GND2 V_{OUTH} − GND2		 V_{DD2} + 0.3	V
Gate−driver output low voltage NCD57090A/B//D/F NCD57090C/E	 V_{OUT} − GND2 V_{OUTL} − GND2	−0.3		V
Gate−driver output sourcing current (maximum pulse width = 10 μs, maximum duty cycle = 0.2%, V_{DD2} = 15 V, V_{EE2} = 0 V)	I_{PK-SRC}		8	A
Gate−driver output sinking current (maximum pulse width = 10 μs, maximum duty cycle = 0.2%, V_{DD2} = 15 V, V_{EE2} = 0 V)	I_{PK-SNK}		8	A
Clamp sinking current (maximum pulse width = 10 μs, maximum duty cycle = 0.2%, V_{CLAMP} = 2.5 V)	$I_{PK-CLAMP}$		2.5	A
Maximum Short Circuit Clamping Time (I_{OUT_CLAMP} = 500 mA)	t_{CLP}		10	μs
Voltage at IN+, IN−	V_{LIM}−GND1	−0.3	V_{DD1} + 0.3	V
Clamp Voltage	V_{CLAMP}−GND2	−0.3	V_{DD2} + 0.3	V
Power Dissipation (SOIC−8 wide package)	PD			mW
Input to Output Isolation Voltage	V_{ISO}	−1200	1200	V
Maximum Junction Temperature	T_J(max)	−40	150	°C
Storage Temperature Range	T_{STG}	−65	150	°C
ESD Capability, Human Body Model (Note 2)	ESDHBM		± 2	kV
ESD Capability, Charged Device Model (Note 2)	ESDCDM		± 2	kV
Moisture Sensitivity Level	MSL		1	−
Lead Temperature Soldering Reflow, Pb−Free (Note 3)	T_{SLD}		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114).
   ESD Charged Device Model tested per AEC−Q100−011 (EIA/JESD22−C101).
   Latchup Current Maximum Rating: ≤ 100 mA per JEDEC standard: JESD78, 25°C.
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 3. THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Characteristics, SOIC−8 wide body (Note 4) Thermal Resistance, Junction−to−Air (Note 5)	$R_{\theta JA}$	156 (1−Layer) 100 (4−Layer)	°C/W

4. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
5. Values based on copper area of 100 mm² (or 0.16 in²) of 1 oz copper thickness and FR4 PCB substrate.

Table 4. OPERATING RANGES (Note 6)

Parameter	Symbol	Min	Max	Unit
Supply voltage, input side	$V_{DD1-GND1}$	UVLO1	20	V
Positive Power Supply, output side	$V_{DD2-GND2}$	UVLO2	30	V
Negative Power Supply, output side (NCD57090B)	$V_{EE2-GND2}$	−15	0	V
Differential Power Supply, output side (NCD57090B)	$V_{DD2-VEE2}$ (V_{MAX2})	0	32	V
Low level input voltage at IN+, IN−	V_{IL}	0	0.3 x V_{DD1}	V
High level input voltage at IN+, IN−	V_{IH}	0.7 x V_{DD1}	V_{DD1}	V
Common Mode Transient Immunity	$\lvert dV_{ISO}/dt \rvert$	100		kV/μs
Ambient Temperature	T_A	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

Table 5. ELECTRICAL CHARACTERISTICS V_{DD1} = 5 V, V_{DD2} = 15 V, (V_{EE2} = 0 V for NCD57090B).
For typical values T_A = 25°C, for min/max values, T_A is the operating ambient temperature range that applies, unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
VOLTAGE SUPPLY						
UVLO1 Output Enabled		$V_{UVLO1-OUT-ON}$			3.1	V
UVLO1 Output Disabled		$V_{UVLO1-OUT-OFF}$	2.4			V
UVLO1 Hysteresis		$V_{UVLO1-HYST}$	0.1			V
UVLO2 Output Enabled		$V_{UVLO2-OUT-ON}$	12.4	12.9	13.4	V
UVLO2 Output Disabled		$V_{UVLO2-OUT-OFF}$	11.5	12	12.5	V
UVLO2 Hysteresis		$V_{UVLO2-HYST}$		1		V
Input Supply Quiescent Current	IN+ = Low, IN− = Low, V_{DD1} = 3.3 V	$I_{DD1-0-3.3}$			2	mA
	IN+ = Low, IN− = Low	$I_{DD1-0-5}$			2	mA
	IN+ = Low, IN− = Low, V_{DD1} = 15 V	$I_{DD1-0-15}$			2	mA
	IN+ = High, IN− = Low	$I_{DD1-100-5}$			5.5	mA
Output Positive Supply Quiescent Current	IN+ = Low, IN− = Low, no load	I_{DD2-0}			2	mA
	IN+ = High, IN− = Low, no load	$I_{DD2-100}$			2	mA
Output Negative Supply Quiescent Current (NCD57090B)	IN+ = Low, IN− = Low, no load, V_{EE2} = −8 V	I_{EE2-0}			2	mA
	IN+ = High, IN− = Low, no load, V_{EE2} = −8 V	$I_{EE2-100}$			2	mA
LOGIC INPUT AND OUTPUT						
IN+, IN−, Low Input Voltage		V_{IL}			0.3 x V_{DD1}	V
IN+, IN−, High Input Voltage		V_{IH}	0.7 x V_{DD1}			V
Input Hysteresis Voltage		$V_{IN-HYST}$		0.15 x V_{DD1}		V
IN− Input Current	V_{IN-} = 0 V, V_{DD1} = 3.3 V	$I_{IN-L-3.3}$			100	μA
	V_{IN-} = 0 V	I_{IN-L-5}			100	μA
	V_{IN-} = 0 V, V_{DD1} = 15 V	$I_{IN-L-15}$			100	μA
	V_{IN-} = 0 V, V_{DD1} = 20 V	$I_{IN-L-20}$			100	μA
IN+ Input Current	V_{IN+} = V_{DD1} = 3.3 V	$I_{IN+H-3.3}$			100	μA
	V_{IN+} = V_{DD1} = 5 V	I_{IN+H-5}			100	μA
	V_{IN+} = V_{DD1} = 15 V	$I_{IN+H-15}$			100	μA
	V_{IN+} = V_{DD1} = 20 V	$I_{IN+H-20}$			100	μA
Input Pulse Width of IN+, IN− for Guaranteed No Response at Output		$t_{ON-MIN1}$			10	ns
Input Pulse Width of IN+, IN− for Guaranteed Response at Output		$t_{ON-MIN2}$	40			ns
DRIVER OUTPUT						
Output Low State (V_{OUT} – GND2 for NCD57090A/D/F) (V_{OUT} – V_{EE2} for NCD57090B) (V_{OUTL} – GND2 for NCD57090C/E)	I_{SINK} = 200 mA	V_{OUTL1}		0.15	0.22	V
	I_{SINK} = 1.0 A, T_A = 25°C	V_{OUTL2}			0.8	

Table 5. ELECTRICAL CHARACTERISTICS V_{DD1} = 5 V, V_{DD2} = 15 V, (V_{EE2} = 0 V for NCD57090B).
For typical values T_A = 25°C, for min/max values, T_A is the operating ambient temperature range that applies, unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
DRIVER OUTPUT						
Output High State ($V_{DD2} - V_{OUT}$ for NCD57090A/B/D/F) ($V_{DD2} - V_{OUT}$ for NCD57090B) ($V_{DD2} - V_{OUTL}$ for NCD57090C/E)	I_{SRC} = 200 mA	V_{OUTH1}		0.2	0.3	V
	I_{SRC} = 1.0 A, T_A = 25°C	V_{OUTH2}			1.0	
Peak Driver Current, Sink (Note 7)		$I_{PK-SNK1}$		8		A
Peak Driver Current, Source (Note 7)		$I_{PK-SRC1}$		8		A
MILLER CLAMP (NCD57090A)						
Clamp Voltage	I_{CLAMP} = 2.5 A, T_A = 25°C	V_{CLAMP}		2		V
	I_{CLAMP} = 2.5 A, T_A = −40°C to 125°C				3.2	
Clamp Activation Threshold		$V_{CLAMP-THR}$	1.5	2	2.5	V
IGBT SHORT CIRCUIT CLAMPING						
Clamping Voltage, Sourcing (V_{OUT} / $V_{OUTH} - V_{DD2}$)	IN+ = Low, IN− = High, $I_{CLAMP-OUT/OUTH}$ = 500 mA, (pulse test, t_{CLPmax} = 10 μs)	$V_{CLAMP-OUTH}$		0.7	0.9	V
Clamping Voltage, Sinking ($V_{OUTL} - V_{DD2}$)	IN+ = High, IN− = Low, $I_{CLAMP-OUTL}$ = 500 mA, (pulse test, t_{CLPmax} = 10 μs)	$V_{CLAMP-OUTL}$		0.8	1.5	V
Clamping Voltage, Clamp ($V_{CLAMP} - V_{DD2}$) (NCD57090A/D/F)	IN+ = High, IN− = Low, $I_{CLAMP-CLAMP}$ = 500 mA (pulse test, t_{CLPmax} = 10 μs)	$V_{CLAMP-CLAMP}$		1.1	1.6	V
DYNAMIC CHARACTERISTIC						
IN+, IN− to Output High Propagation Delay	C_{LOAD} = 10 nF V_{IH} to 10% of output change Pulse Width > 150 ns.					
	$V_{DD1} = V_{IN+}$ = 3.3V, V_{IN-} = 0 V	$t_{PD-ON-3.3}$	45	60	85	ns
	$V_{DD1} = V_{IN+}$ = 5 V, V_{IN-} = 0 V	$t_{PD-ON-5}$	45	60	85	ns
	$V_{DD1} = V_{IN+}$ = 15 V, V_{IN-} = 0 V	$t_{PD-ON-15}$	45	60	85	ns
	$V_{DD1} = V_{IN+}$ = 20 V, V_{IN-} = 0 V	$t_{PD-ON-20}$	45	60	85	ns
IN+, IN− to Output Low Propagation Delay	C_{LOAD} = 10 nF V_{IH} to 10% of output change Pulse Width > 150 ns.					
	$V_{DD1} = V_{IN+}$ = 3.3 V, V_{IN-} = 0 V	$t_{PD-OFF-3.3}$	45	60	85	ns
	$V_{DD1} = V_{IN+}$ = 5 V, V_{IN-} = 0 V	$t_{PD-OFF-5}$	45	60	85	ns
	$V_{DD1} = V_{IN+}$ = 15 V, V_{IN-} = 0 V	$t_{PD-OFF-15}$	45	60	85	ns
	$V_{DD1} = V_{IN+}$ = 20 V, V_{IN-} = 0 V	$t_{PD-OFF-20}$	45	60	85	ns
Propagation Delay Distortion (= $t_{PD-ON} - t_{PD-OFF}$)	T_A = 25°C, PW > 150 ns	$t_{DISTORT}$		−6		ns
	T_A = −40°C to 125°C, PW > 150 ns		−15		15	ns
Prop Delay Distortion between Parts	PW > 150 ns	$t_{DISTORT\_TOT}$	−30	0	30	ns
Rise Time (see Fig. 3)	C_{LOAD} = 1 nF, 10% to 90% of Output Change			13		ns
Fall Time (see Fig. 3)	C_{LOAD} = 1 nF, 90% to 10% of Output Change			13		ns

Table 5. ELECTRICAL CHARACTERISTICS V_{DD1} = 5 V, V_{DD2} = 15 V, (V_{EE2} = 0 V for NCD57090B).
For typical values T_A = 25°C, for min/max values, T_A is the operating ambient temperature range that applies, unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTIC						
UVLO1 Fall Delay		t_{UV1F}		1500		ns
UVLO1 Rise Delay		t_{UV1R}		770		ns
UVLO2 Fall Delay		t_{UV2F}		1000		ns
UVLO2 Rise Delay		t_{UV2R}		1000		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
7. Values based on design and/or characterization.

ORDERING INFORMATION

Device	Package	Shipping†
NCD57090ADR2G	SOIC−8 Wide Body, (Pb−Free)	2500 / Tape & Reel
NCD57090BDR2G	SOIC−8 Wide Body, (Pb−Free)	2500 / Tape & Reel
NCD57090CDR2G	SOIC−8 Wide Body, (Pb−Free)	2500 / Tape & Reel
NCD57090DDR2G	SOIC−8 Wide Body, (Pb−Free)	2500 / Tape & Reel
NCD57090EDR2G	SOIC−8 Wide Body, (Pb−Free)	2500 / Tape & Reel
NCD57090FDR2G	SOIC−8 Wide Body, (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

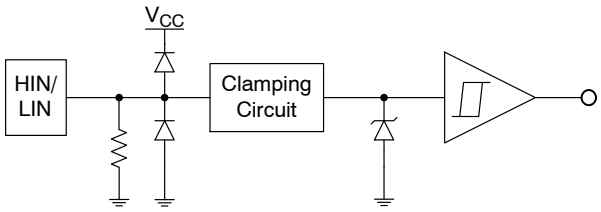


Figure 7. Input Pin Structure

TYPICAL CHARACTERISTICS

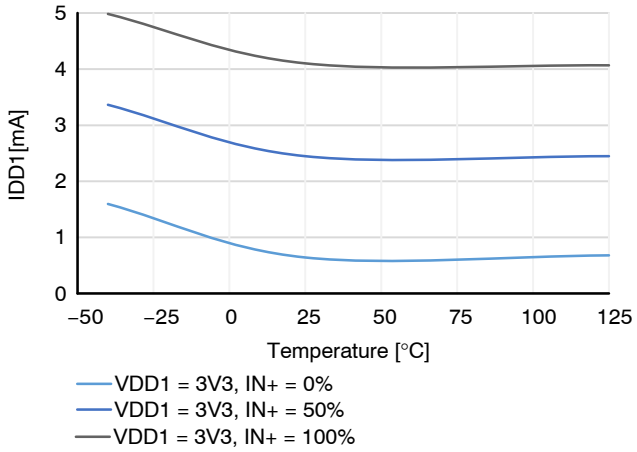


Figure 8. I_{DD1} Supply Current V_{DD1} = 3.3 V

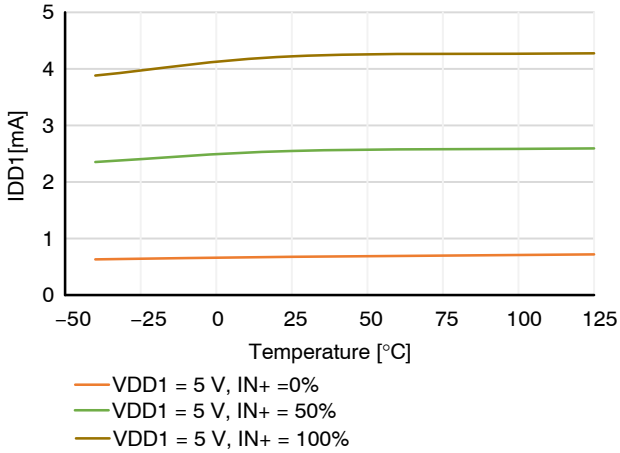


Figure 9. I_{DD1} Supply Current V_{DD1} = 5 V

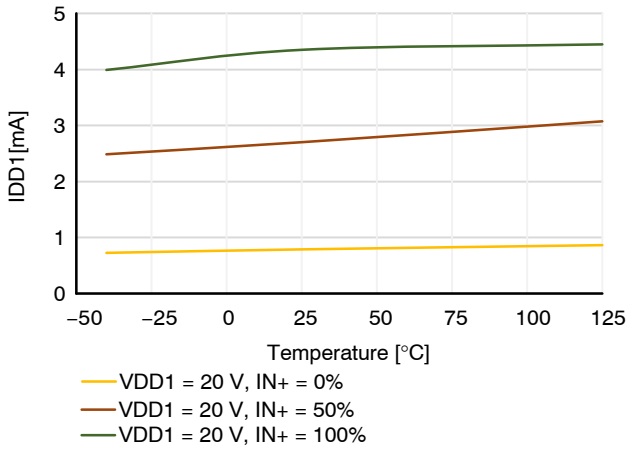


Figure 10. I_{DD1} Supply Current V_{DD1} = 20 V

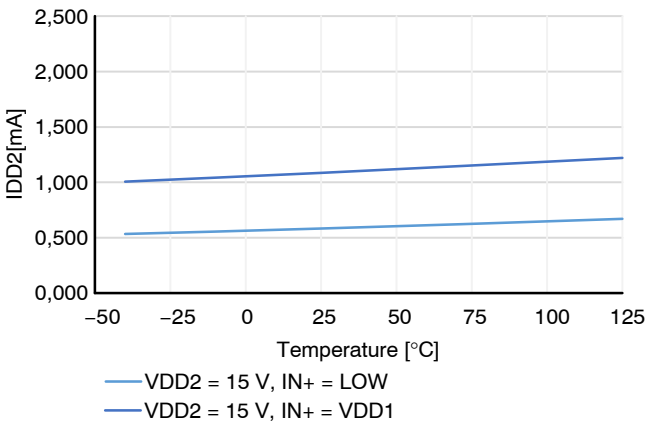


Figure 11. I_{DD2} Supply Current V_{DD2} = 15 V

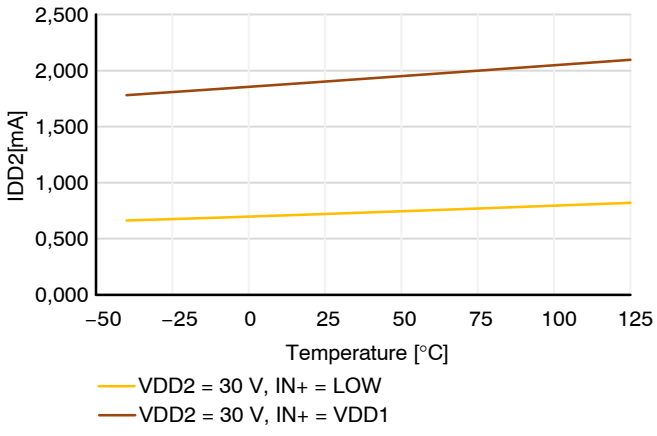


Figure 12. I_{DD2} Supply Current V_{DD2} = 30 V

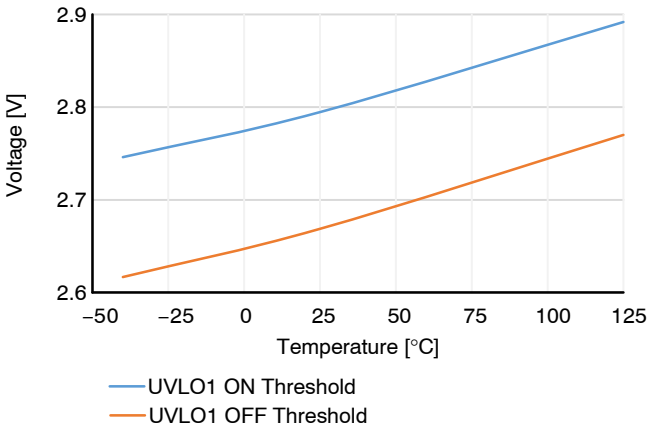


Figure 13. UVLO1 Threshold Voltage

TYPICAL CHARACTERISTICS (continued)

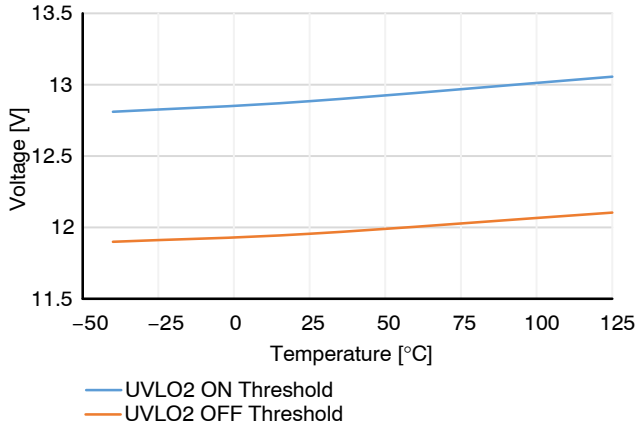


Figure 14. UVLO2 Threshold Voltage

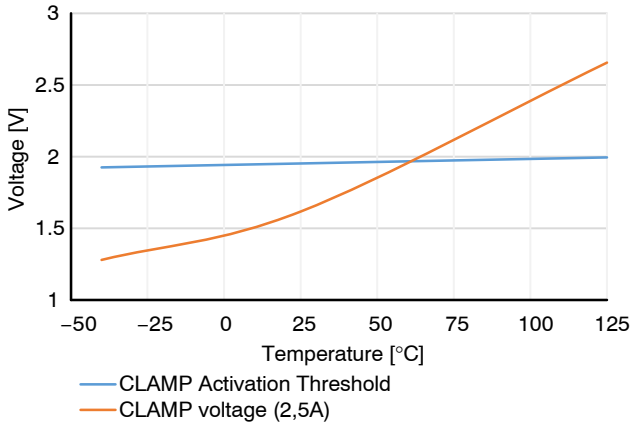


Figure 15. Output CLAMP Voltage

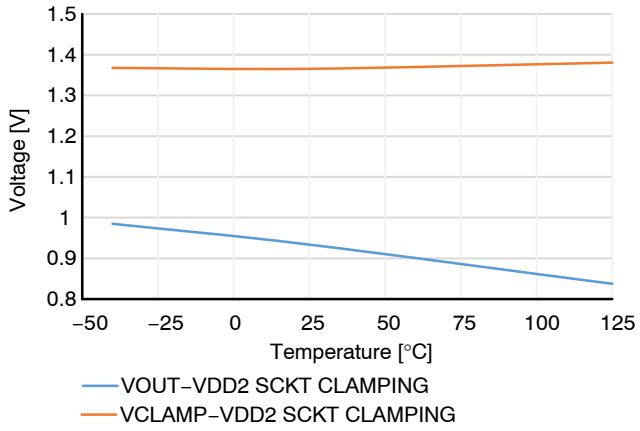


Figure 16. IGBT Short Circuit CLAMP Voltage Drop

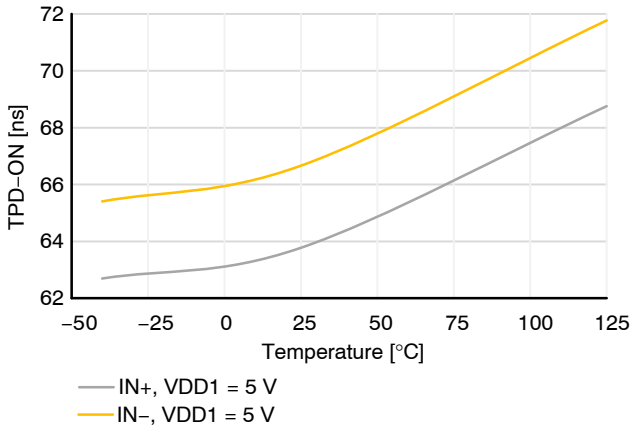


Figure 17. Propagation Delay Turn−on

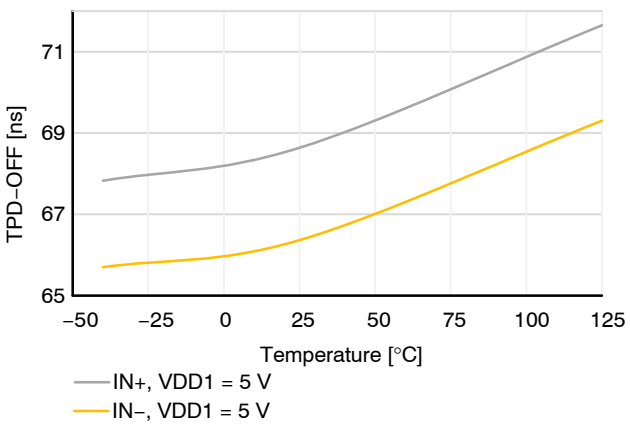


Figure 18. Propagation Delay Turn−off

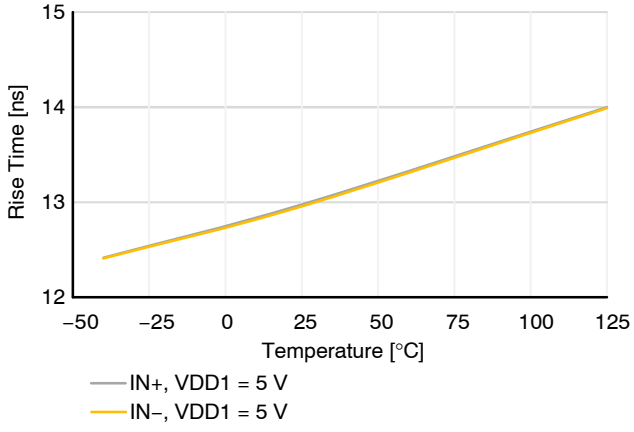


Figure 19. Rise Time

TYPICAL CHARACTERISTICS (continued)

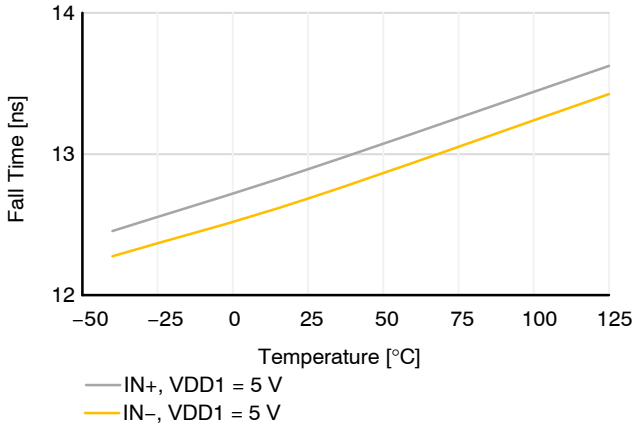


Figure 20. Fall Time

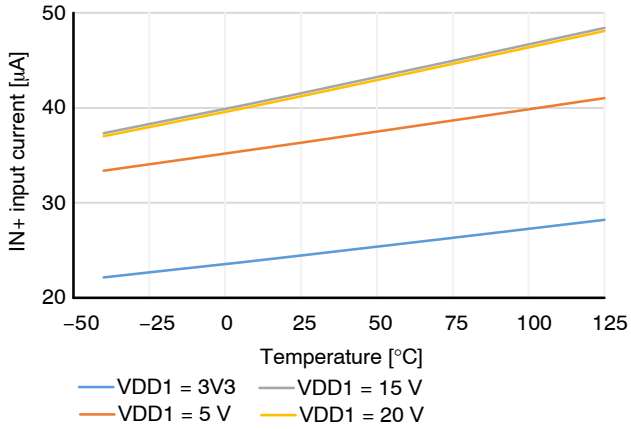


Figure 21. Input Current – Positive Input

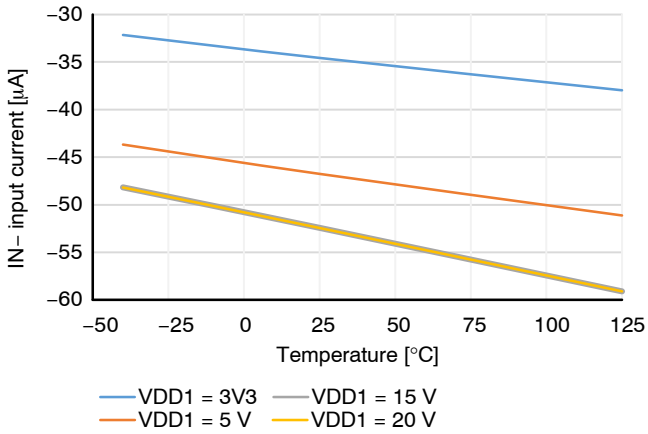


Figure 22. Input Current – Negative Input

Under Voltage Lockout (UVLO)

UVLO ensures correct switching of IGBT connected to the driver output.

- The IGBT is turned−off and the output is disabled, if the supply V_{DD1} drops below $V_{UVLO1–OUT–OFF}$ or V_{DD2} drops below $V_{UVLO2–OUT–OFF}$
- The driver output does not follow the input signal on V_{IN} until the V_{DDX} rises above the $V_{UVLOX–OUT–ON}$ and the input signal rising edge is applied to the V_{IN}
- V_{EE2} is not monitored. (NCD57090B)

With high loading gate capacitances over 10 nF it is important to follow the decoupling capacitor routing guidelines as shown on Figure 23. The decoupling capacitor value should be at least 10 μF. Also gate resistor of minimal value of 2 Ω has to be used in order to avoid interference of the high di/dt with internal circuitry (e.g. UVLO2).

After the power−on of the driver there has to be a rising edge applied to the IN+ or falling edge to the IN− in order for the output to start following the inputs. This serves as a protection against producing partial pulses at the output if the V_{DD1} or V_{DD2} is applied in the middle of the input PWM pulse.

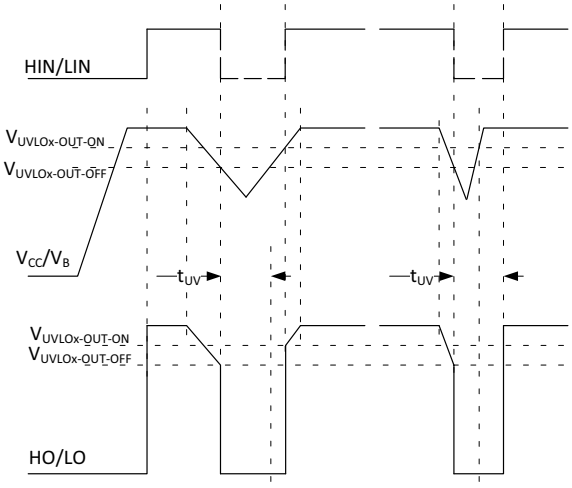


Figure 23. UVLO Waveforms

Active Miler Clamp Protection (CLAMP)

NCD57090B supports bipolar power supply to prevent unintentionally turning on.

For operation with bipolar supplies, the IGBT is turned off with a negative voltage through OUTL with respect to its emitter. This prevents the IGBT from unintentionally turning on because of current induced from its collector to its gate due to Miller effect. Typical values for bipolar operation are V_{DD2} = 15 V and V_{EE2} = −5 V with respect to GND_2.

NCD57090A/D/F supports unipolar power supply with active Miller clamp.

For operation with unipolar supply, typically, V_{DD2} = 15 V with respect to GND_2, and V_{EE2} = GND_2. In this case, the IGBT can turn on due to additional charge from IGBT Miller capacitance caused by a high voltage slew rate transition on the IGBT collector. To prevent IGBT to turn on, the CLAMP pin is connected directly to IGBT gate and Miller current is sinked through a low impedance CLAMP transistor. When the IGBT is turned−off and the gate voltage transitions below V_{CLAMP}, the CLAMP current output is activated

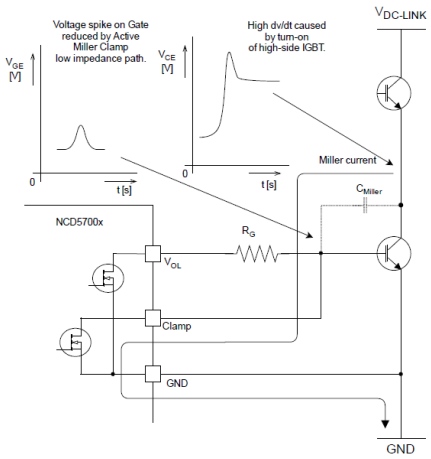


Figure 24. Current Path with Miler Clamp Protection

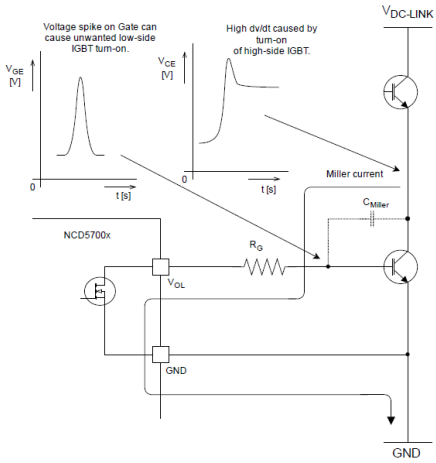


Figure 25. Current Path without Miler Clamp Protect

Non−inverting and Inverting Input Pin (IN+, IN−)

NCD57090x has two possible input modes to control IGBT. Both inputs have defined minimum input pulse width to filter occasional glitches.

- Non−inverting input IN+ controls the driver output while inverting input IN− is set to LOW
- Inverting input IN− controls the driver output while non−inverting input IN+ is set to HIGH

WARNING: When the application use an independent or separate power supply for the control unit ant the input side of the driver, all inputs should be protected by a serial resistor (In case of a power failure of the driver, the driver may be damaged due to overloading of the input protection circuits)

Power Supply (VDD1, VDD2, VEE2)

NCD57090A/C/D/E and NCD57090F is designed to support unipolar power supply.

NCD57090B is designed to support bipolar power supply.

For reliable high output current the suitable external power capacitors required. Parallel combination of 100 nF + 4.7 μF ceramic capacitors is optimal for a wide range of applications using IGBT. For reliable driving IGBT modules (containing several parallel IGBT's) is a higher capacity required (typically 100 nF + 10 μF). Capacitors should be as close as possible to the driver's power pins.

- In bipolar power supply the driver is typically supplied with a positive voltage of 15 V at VDD2 and negative voltage −5 V at VEE2 (Figure 26). Negative power supply prevents a dynamic turn on through the internal IGBT input capacitance
- In Unipolar power supply the driver is typically supplied with a positive voltage of 15 V at VDD2. Dynamic turn on through the internal IGBT input capacitance could be prevented by Active Miler Clamp function (NCD57090A/D/F). CLAMP output should be directly connected to IGBT gate (Figure 27)

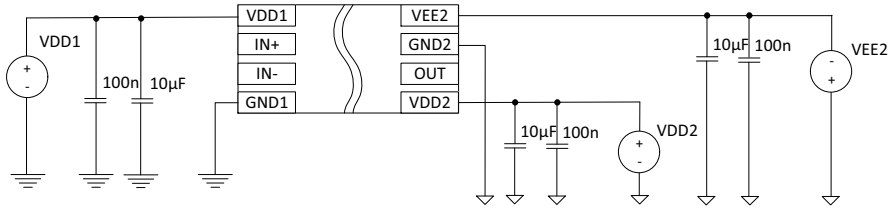


Figure 26. Bipolar Power Supply NCD57090B

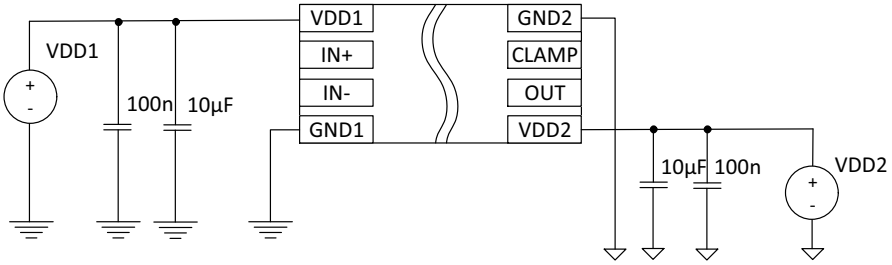


Figure 27. Unipolar Power Supply NCD57090A/D/F

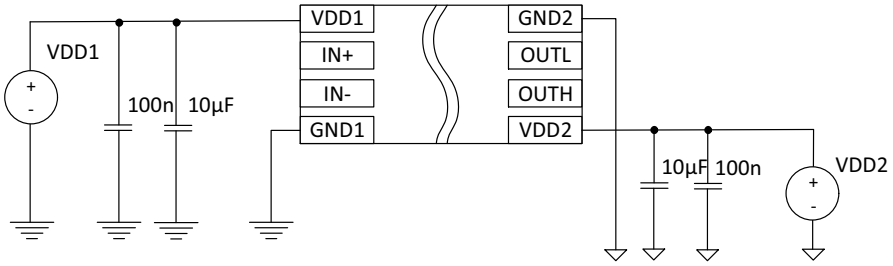


Figure 28. Unipolar Power Supply NCD57090C/E

Common Mode Transient Immunity (CMTI)

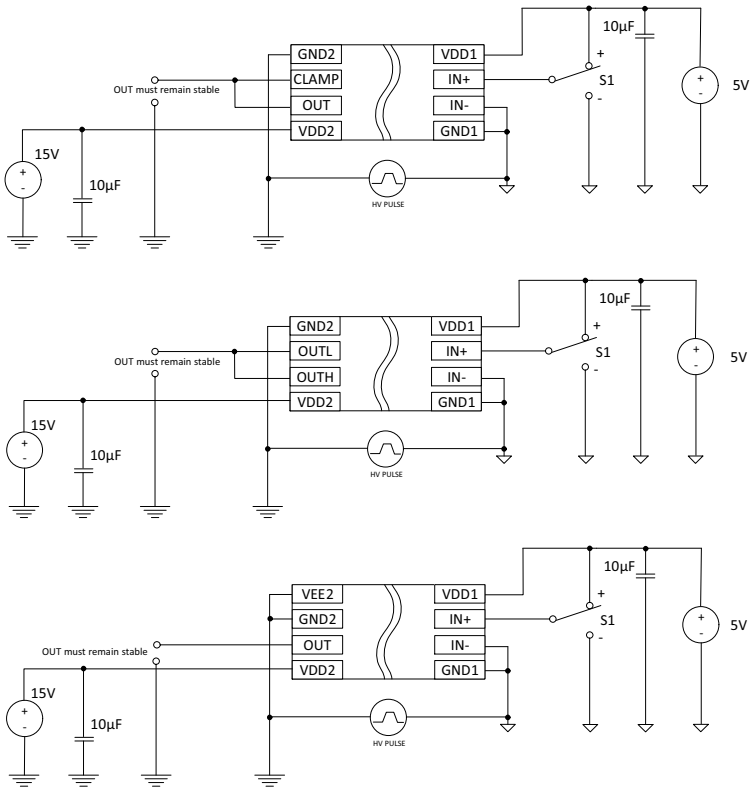


Figure 29. Common−Mode Transient Immunity Test Circuit

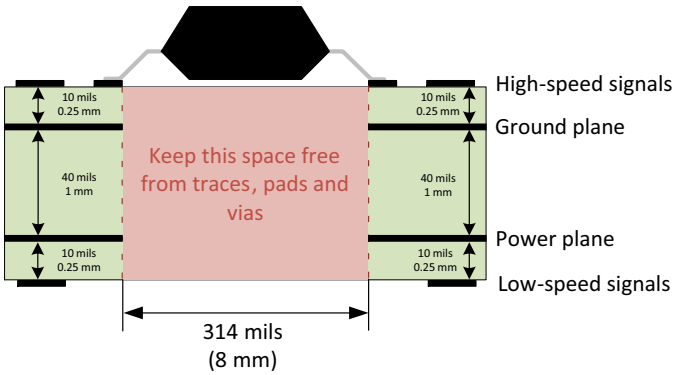


Figure 30. Common−Mode Transient Immunity Test Circuit

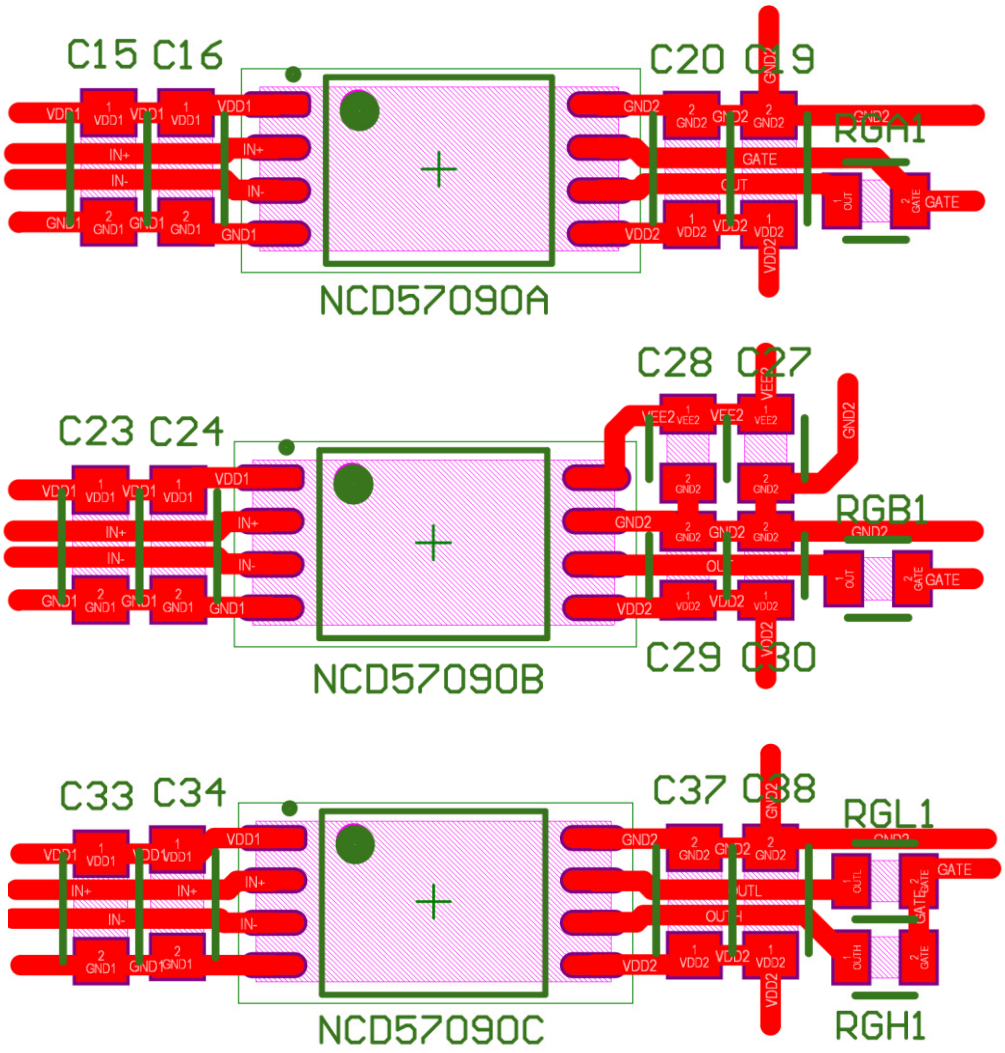


Figure 31. Recommended Layout for NCD57090A/B/C

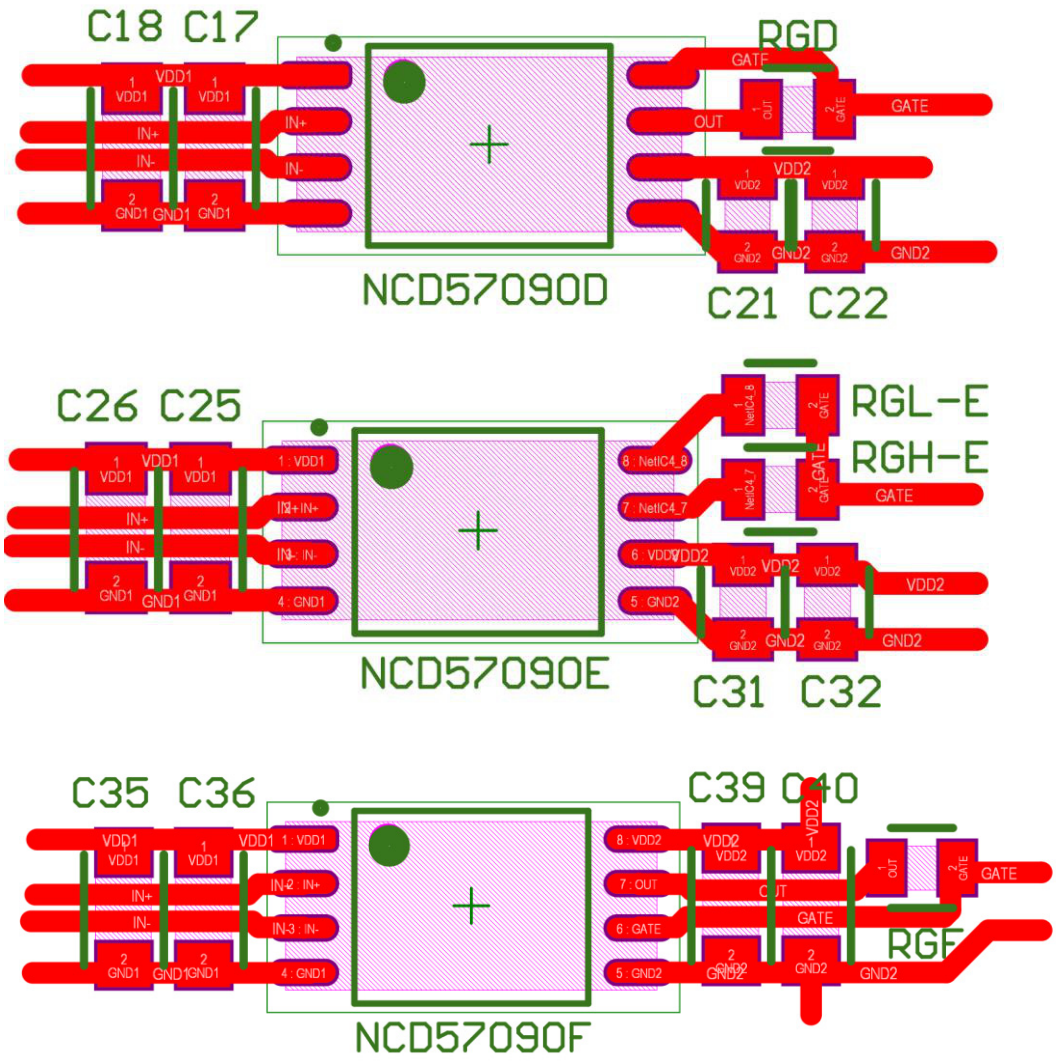
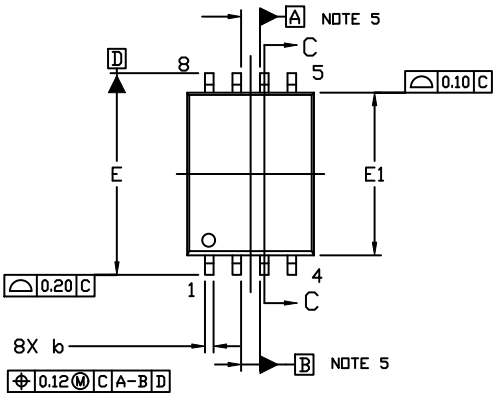


Figure 32. Recommended Layout for NCD57090D/E/F

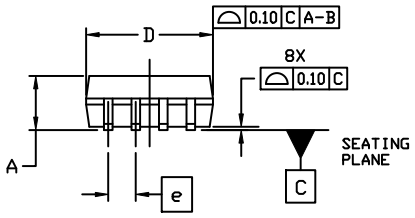
PACKAGE DIMENSIONS

SOIC8 WB
CASE 751EW
ISSUE A

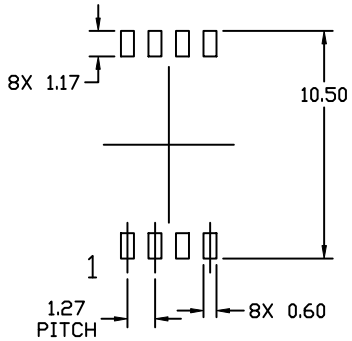
DATE 31 MAY 2019



TOP VIEW



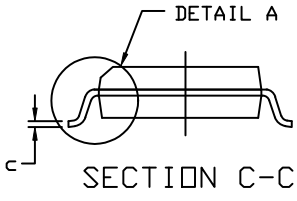
SIDE VIEW



RECOMMENDED MOUNTING FOOTPRINT

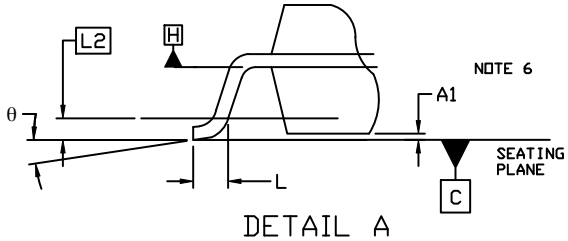
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM H.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. NO JEDEC STANDARD AT TIME OF SETUP.



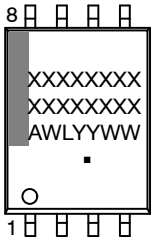
SECTION C-C

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.35	2.50	2.65
A1	0.10	0.20	0.30
b	0.31	0.41	0.51
c	0.20	0.27	0.33
D	5.65	5.85	6.05
E	10.11	10.31	10.51
E1	7.40	7.50	7.60
e	1.27 BSC		
L	0.40	0.58	0.75
L2	0.25 BSC		
θ	0°	---	8°



DETAIL A

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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