

Operational Amplifier, Zero-Drift, 10 μV Offset, 0.07 $\mu\text{V}/^\circ\text{C}$

NCS333A, NCV333A, NCS2333, NCV2333, NCS4333, NCV4333, NCS333

The NCS333/2333/4333 family of zero-drift op amps feature offset voltage as low as 10 μV over the 1.8 V to 5.5 V supply voltage range. The zero-drift architecture reduces the offset drift to as low as 0.07 $\mu\text{V}/^\circ\text{C}$ and enables high precision measurements over both time and temperature. This family has low power consumption over a wide dynamic range and is available in space saving packages. These features make it well suited for signal conditioning circuits in portable, industrial, automotive, medical and consumer markets.

Features

- Gain-Bandwidth Product:
 - ◆ 270 kHz (NCx2333)
 - ◆ 350 kHz (NCx333, NCx333A, NCx4333)
- Low Supply Current: 17 μA (typ at 3.3 V)
- Low Offset Voltage:
 - ◆ 10 μV max for NCS333, NCS333A
 - ◆ 30 μV max for NCV333A, NCx2333 and NCx4333
- Low Offset Drift: 0.07 $\mu\text{V}/^\circ\text{C}$ max for NCS333/A
- Wide Supply Range: 1.8 V to 5.5 V
- Wide Temperature Range: -40°C to $+125^\circ\text{C}$
- Rail-to-Rail Input and Output
- Available in Single, Dual and Quad Packages
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

Applications

- Automotive
- Battery Powered/ Portable Application
- Sensor Signal Conditioning
- Low Voltage Current Sensing
- Filter Circuits
- Bridge Circuits
- Medical Instrumentation



ON Semiconductor®

www.onsemi.com



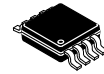
SOT23-5
SN SUFFIX
CASE 483



SC70-5
SQ SUFFIX
CASE 419A



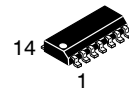
UDFN8
MU SUFFIX
CASE 517AW



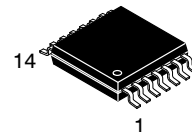
MSOP-8
DM SUFFIX
CASE 846A-02



SOIC-8
D SUFFIX
CASE 751



SOIC-14
D SUFFIX
CASE 751A



TSSOP-14 WB
DT SUFFIX
CASE 948G

DEVICE MARKING INFORMATION

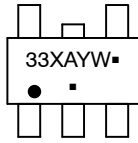
See general marking information in the device marking section on page 2 of this data sheet.

ORDERING INFORMATION

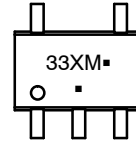
See detailed ordering and shipping information on page 3 of this data sheet.

DEVICE MARKING INFORMATION

Single Channel Configuration
NCS333, NCS333A, NCV333A

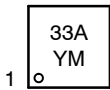


TSOP-5/SOT23-5
CASE 483

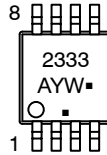


SC70-5
CASE 419A

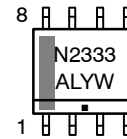
Dual Channel Configuration
NCS2333, NCV2333



UDFN8, 2x2, 0.5P
CASE 517AW

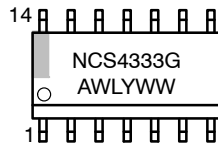


Micro8/MSOP8
CASE 846A-02

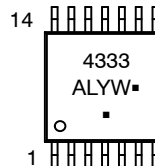


SOIC-8
CASE 751

Quad Channel Configuration
NCS4333, NCV4333



SOIC-14
CASE 751A



TSSOP-14
CASE 948G

- X = Specific Device Code
 - E = NCS333 (SOT23-5)
 - H = NCS333 (SC70-5)
 - G = NCS333A (SOT23-5)
 - K = NCS333A (SC70-5)
 - M = NCV333A (SOT23-5)
 - N = NCV333A (SC70-5)
- A = Assembly Location
- Y = Year
- W = Work Week
- M = Date Code
- G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

NCS333A, NCV333A, NCS2333, NCV2333, NCS4333, NCV4333, NCS333

PIN CONNECTIONS

Single Channel Configuration NCS333, NCS333A, NCV333A

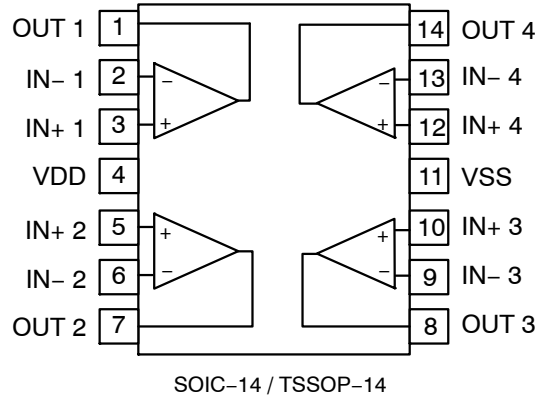


Dual Channel Configuration NCS2333, NCV2333



*The exposed pad of the UDFN8 package can be floated or connected to VSS.

Quad Channel Configuration NCS4333, NCV4333



ORDERING INFORMATION

| Channels | Device | Package | Shipping † |
|----------|---------------------------------|------------------------------|--------------------|
| Single | NCS333SN2T1G | SOT23-5 / TSOP-5 | 3000 / Tape & Reel |
| | NCS333ASN2T1G | | 3000 / Tape & Reel |
| | NCS333SQ3T2G | SC70-5 / SC-88-5 / SOT-353-5 | 3000 / Tape & Reel |
| | NCS333ASQ3T2G | | 3000 / Tape & Reel |
| Dual | NCS2333MUTBG | UDFN8 | 3000 / Tape & Reel |
| | NCS2333DR2G | SOIC-8 | 3000 / Tape & Reel |
| | NCS2333DMR2G | MICRO-8 | 4000 / Tape & Reel |
| Quad | NCS4333DR2G | SOIC-14 | 2500 / Tape & Reel |
| | NCS4333DTBR2G (In Development*) | TSSOP-14 | 2500 / Tape & Reel |

Automotive Qualified

| Channels | Device | Package | Shipping † |
|----------|---------------------------------|------------------------------|--------------------|
| Single | NCV333ASN2T1G | SOT23-5 / TSOP-5 | 3000 / Tape & Reel |
| | NCV333ASQ3T2G | SC70-5 / SC-88-5 / SOT-353-5 | 3000 / Tape & Reel |
| Dual | NCV2333DR2G | SOIC-8 | 3000 / Tape & Reel |
| | NCV2333DMR2G | MICRO-8 | 4000 / Tape & Reel |
| Quad | NCV4333DR2G | SOIC-14 | 2500 / Tape & Reel |
| | NCV4333DTBR2G (In Development*) | TSSOP-14 | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*Contact local sales office for more information.

NCS333A, NCV333A, NCS2333, NCV2333, NCS4333, NCV4333, NCS333

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature, unless otherwise stated.

| Parameter | Rating | Unit |
|----------------|--------|------|
| Supply Voltage | 7 | V |

INPUT AND OUTPUT PINS

| | | |
|---------------------------------------|----------------------------|----|
| Input Voltage (Note 1) | (VSS) – 0.3 to (VDD) + 0.3 | V |
| Input Current (Note 1) | ±10 | mA |
| Output Short Circuit Current (Note 2) | Continuous | |

TEMPERATURE

| | | |
|-----------------------------|-------------|----|
| Operating Temperature Range | –40 to +125 | °C |
| Storage Temperature Range | –65 to +150 | °C |
| Junction Temperature | +150 | °C |

ESD RATINGS (Note 3)

| | | |
|----------------------------|-------|---|
| Human Body Model (HBM) | ±4000 | V |
| Machine Model (MM) | ±200 | V |
| Charged Device Model (CDM) | ±2000 | V |

OTHER RATINGS

| | | |
|---------------------------|---------|----|
| Latch-up Current (Note 4) | 100 | mA |
| MSL | Level 1 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less
- Short-circuit to ground.
- This device series incorporates ESD protection and is tested by the following methods:
 - ESD Human Body Model tested per JEDEC standard JS-001 (AEC-Q100-002)
 - ESD Machine Model tested per JEDEC standard JESD22-A115 (AEC-Q100-003)
 - ESD Charged Device Model tested per JEDEC standard JESD22-C101 (AEC-Q100-011)
- Latch-up Current tested per JEDEC standard: JESD78.

THERMAL INFORMATION (Note 5)

| Parameter | Symbol | Package | Value | Unit |
|---|---------------|------------------------------|-------|------|
| Thermal Resistance, Junction to Ambient | θ_{JA} | SOT23-5 / TSOP5 | 290 | °C/W |
| | | SC70-5 / SC-88-5 / SOT-353-5 | 425 | |
| | | Micro8 / MSOP8 | 298 | |
| | | SOIC-8 | 250 | |
| | | UDFN8 | 228 | |
| | | SOIC-14 | 216 | |
| | | TSSOP-14 | 155 | |

- As mounted on an 80x80x1.5 mm FR4 PCB with 650 mm² and 2 oz (0.07 mm) thick copper heat spreader. Following JEDEC JESD/EIA 51.1, 51.2, 51.3 test guidelines

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Range | Unit |
|---|-------------------|--|------------|
| Supply Voltage (V _{DD} – V _{SS}) | V _S | 1.8 to 5.5 | V |
| Specified Operating Temperature Range | T _A | NCS333 | –40 to 105 |
| | | NCx333A, NCx2333, NCx4333 | –40 to 125 |
| Input Common Mode Voltage Range | V _{ICMR} | V _{SS} –0.1 to V _{DD} +0.1 | V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

NCS333A, NCV333A, NCS2333, NCV2333, NCS4333, NCV4333, NCS333

ELECTRICAL CHARACTERISTICS: $V_S = 1.8\text{ V to }5.5\text{ V}$

At $T_A = +25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

Boldface limits apply over the specified operating temperature range, guaranteed by characterization and/or design.

| Parameter | Symbol | Conditions | | Min | Typ | Max | Unit |
|--------------------------------------|----------------------------|-----------------------------|-----------------------------------|---------------------------|--------------|-----------------------------|------------------------------|
| INPUT CHARACTERISTICS | | | | | | | |
| Offset Voltage | V_{OS} | $V_S = +5\text{ V}$ | NCS333, NCS333A | | 3.5 | 10 | μV |
| | | | NCV333A, NCx2333, NCx4333 | | 6.0 | 30 | |
| Offset Voltage Drift vs Temp | $\Delta V_{OS}/\Delta T$ | NCS333, NCS333A | | | 0.03 | 0.07 | $\mu\text{V}/^\circ\text{C}$ |
| | | NCV333A, $V_S = 5\text{ V}$ | | | 0.03 | 0.14 | |
| | | NCx2333, $V_S = 5\text{ V}$ | | | 0.04 | 0.07 | |
| | | NCx4333, $V_S = 5\text{ V}$ | | | 0.095 | 0.19 | |
| Offset Voltage Drift vs Supply | $\Delta V_{OS}/\Delta V_S$ | NCS333, NCS333A | Full temperature range | | 0.32 | 5 | $\mu\text{V}/\text{V}$ |
| | | | NCV333A | $T_A = +25^\circ\text{C}$ | | 0.40 | |
| | | NCx2333, NCx4333 | Full temperature range | | | 8 | |
| | | | $T_A = +25^\circ\text{C}$ | | 0.32 | 5 | |
| | | | Full temperature range | | | 12.6 | |
| Input Bias Current (Note 6) | I_{IB} | $T_A = +25^\circ\text{C}$ | NCS333, NCx333A | | ± 60 | ± 200 | pA |
| | | | NCx2333, NCx4333 | | ± 60 | ± 400 | |
| | | Full temperature range | | | | ± 400 | |
| Input Offset Current (Note 6) | I_{OS} | $T_A = +25^\circ\text{C}$ | NCS333, NCx333A | | ± 50 | ± 400 | pA |
| | | | NCx2333, NCx4333 | | ± 50 | ± 800 | |
| Common Mode Rejection Ratio (Note 7) | CMRR | $V_S = 1.8\text{ V}$ | | | 111 | | dB |
| | | $V_S = 3.3\text{ V}$ | | | 118 | | |
| | | $V_S = 5.0\text{ V}$ | NCS333, NCS333A, NCx2333, NCx4333 | 106 | 123 | | |
| | | | NCV333A | 103 | 123 | | |
| | | $V_S = 5.5\text{ V}$ | | | 127 | | |
| Input Resistance | R_{IN} | Differential | | | 180 | | $\text{G}\Omega$ |
| | | Common Mode | | | 90 | | |
| Input Capacitance | C_{IN} | NCS333 | Differential | | 2.3 | | pF |
| | | | Common Mode | | 4.6 | | |
| | | NCx2333, NCx4333, NCx333A | Differential | | 4.1 | | |
| | | | Common Mode | | 7.9 | | |

OUTPUT CHARACTERISTICS

| | | | | | | |
|---|--------------|---|------------|-----|-----------|----------|
| Open Loop Voltage Gain (Note 6) | A_{VOL} | $V_{SS} + 100\text{ mV} < V_O < V_{DD} - 100\text{ mV}$ | 106 | 145 | | dB |
| Open Loop Output Impedance | Z_{out-OL} | $f = \text{UGBW}$, $I_O = 0\text{ mA}$ | | 300 | | Ω |
| Output Voltage High, Referenced to V_{DD} | V_{OH} | $T_A = +25^\circ\text{C}$ | | 10 | 50 | mV |
| | | Full temperature range | | | 70 | |
| Output Voltage Low, Referenced to V_{SS} | V_{OL} | $T_A = +25^\circ\text{C}$ | | 10 | 50 | mV |
| | | Full temperature range | | | 70 | |

6. Guaranteed by characterization and/or design

7. Specified over the full common mode range: $V_{SS} - 0.1 < V_{CM} < V_{DD} + 0.1$

NCS333A, NCV333A, NCS2333, NCV2333, NCS4333, NCV4333, NCS333

ELECTRICAL CHARACTERISTICS: $V_S = 1.8\text{ V to }5.5\text{ V}$

At $T_A = +25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT}$ = midsupply, unless otherwise noted.

Boldface limits apply over the specified operating temperature range, guaranteed by characterization and/or design.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-----------|--------|------------|-----|-----|-----|------|
|-----------|--------|------------|-----|-----|-----|------|

OUTPUT CHARACTERISTICS

| | | | | | | | |
|---------------------------|-------|------------------|------------------------------|---------------|-----|--|----|
| Output Current Capability | I_O | Sinking Current | NCS333 | | 25 | | mA |
| | | | NCx333A, NCx2333, NCx4333 | | 11 | | |
| | | Sourcing Current | | | 5.0 | | |
| Capacitive Load Drive | C_L | | | See Figure 13 | | | |

NOISE PERFORMANCE

| | | | | | | |
|-----------------------|-----------|--|--|-----|--|--------------------------------|
| Voltage Noise Density | e_N | $f_{IN} = 1\text{ kHz}$ | | 62 | | $\text{nV} / \sqrt{\text{Hz}}$ |
| Voltage Noise | e_{P-P} | $f_{IN} = 0.1\text{ Hz to }10\text{ Hz}$ | | 1.1 | | μV_{PP} |
| | | $f_{IN} = 0.01\text{ Hz to }1\text{ Hz}$ | | 0.5 | | |
| Current Noise Density | i_N | $f_{IN} = 10\text{ Hz}$ | | 350 | | $\text{fA} / \sqrt{\text{Hz}}$ |
| Channel Separation | | NCx2333, NCx4333 | | 135 | | dB |

DYNAMIC PERFORMANCE

| | | | | | | | |
|------------------------|----------|-----------------------|-----------------------------|--|------|--|------------------------|
| Gain Bandwidth Product | GBWP | $C_L = 100\text{ pF}$ | NCS333, NCx333A, NCx4333 | | 350 | | kHz |
| | | | NCx2333 | | 270 | | |
| Gain Margin | A_M | $C_L = 100\text{ pF}$ | | | 18 | | dB |
| Phase Margin | ϕ_M | $C_L = 100\text{ pF}$ | | | 55 | | $^\circ$ |
| Slew Rate | SR | $G = +1$ | | | 0.15 | | $\text{V}/\mu\text{s}$ |

POWER SUPPLY

| | | | | | | | |
|--|----------|--------------------------------------|---|------------|-----|----|---------------|
| Power Supply Rejection Ratio | PSRR | NCS333, NCS333A | Full temperature range | 106 | 130 | | dB |
| | | NCx2333, NCx4333, NCV333A | $T_A = +25^\circ\text{C}$ | 106 | 130 | | |
| | | | Full temperature range | 98 | | | |
| Turn-on Time | t_{ON} | $V_S = 5\text{ V}$ | | | 100 | | μs |
| Quiescent Current (Note 8) | I_Q | NCS333, NCS333A, NCx2333, NCx4333 | $1.8\text{ V} \leq V_S \leq 3.3\text{ V}$ | | 17 | 25 | μA |
| | | | | 27 | | | |
| | | | $3.3\text{ V} < V_S \leq 5.5\text{ V}$ | | 21 | 33 | |
| | | | 35 | | | | |
| | | NCV333A | $1.8\text{ V} \leq V_S \leq 3.3\text{ V}$ | | 20 | 30 | |
| | | | | 35 | | | |
| $3.3\text{ V} < V_S \leq 5.5\text{ V}$ | | | 28 | 40 | | | |
| | | | 45 | | | | |

8. No load, per channel

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

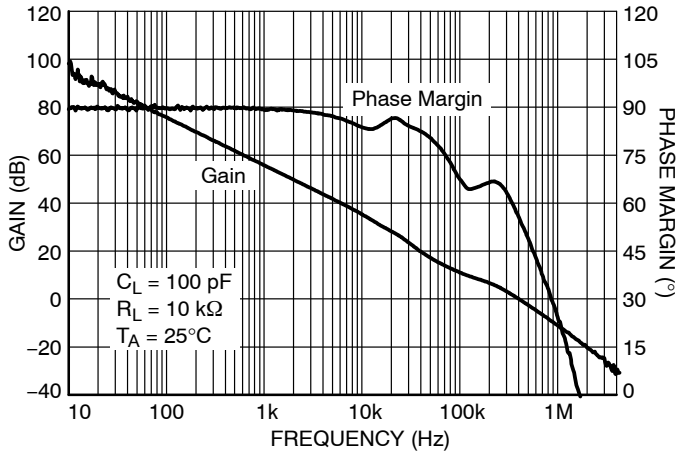


Figure 1. Open Loop Gain and Phase Margin vs. Frequency

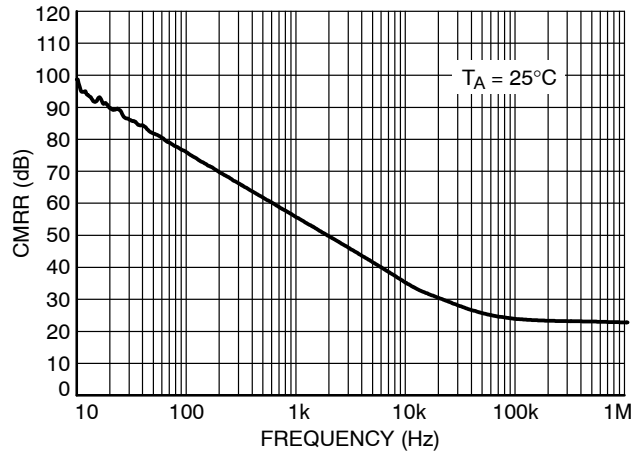


Figure 2. CMRR vs. Frequency

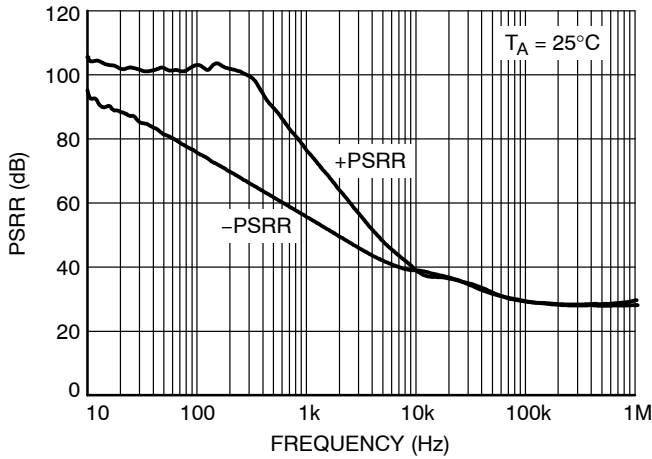


Figure 3. PSRR vs. Frequency

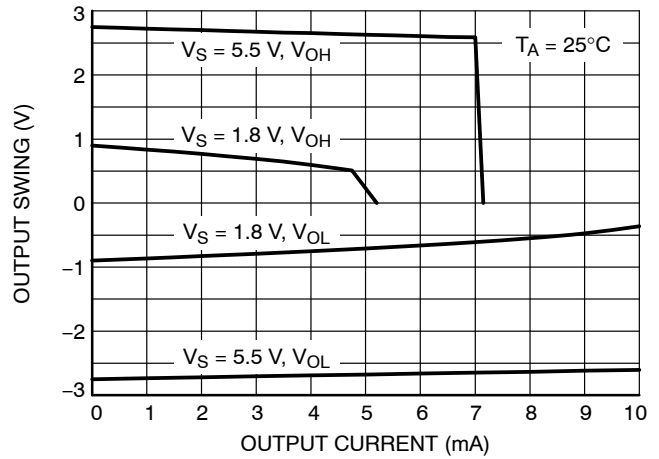


Figure 4. Output Voltage Swing vs. Output Current

TYPICAL CHARACTERISTICS



Figure 5. Input Bias Current vs. Common Mode Voltage

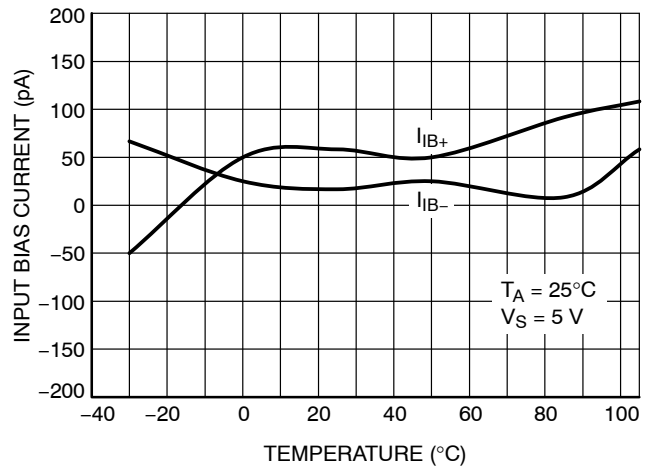


Figure 6. Input Bias Current vs. Temperature

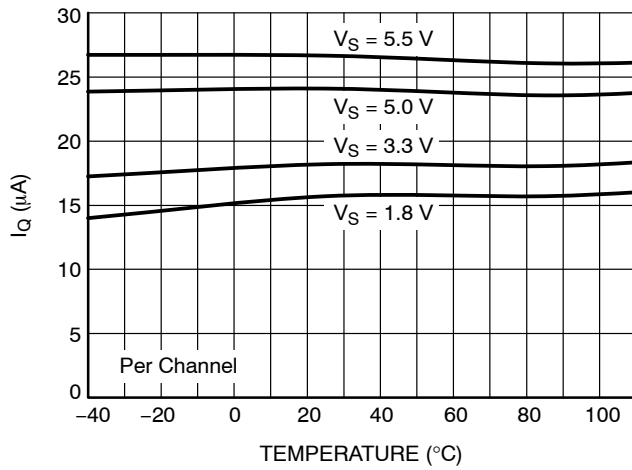


Figure 7. Quiescent Current vs. Temperature

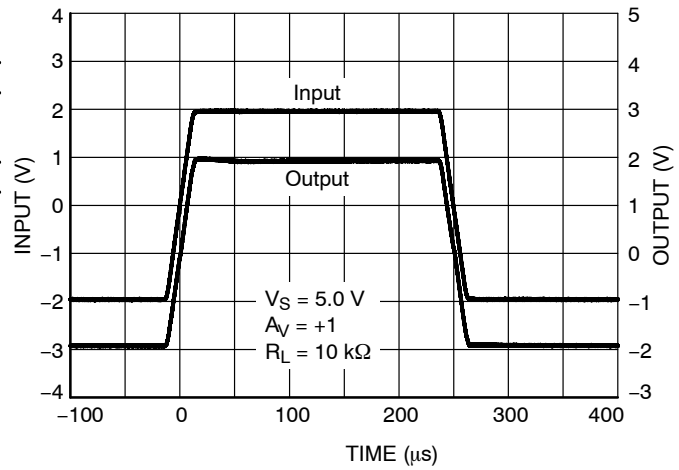


Figure 8. Large Signal Step Response



Figure 9. Small Signal Step Response

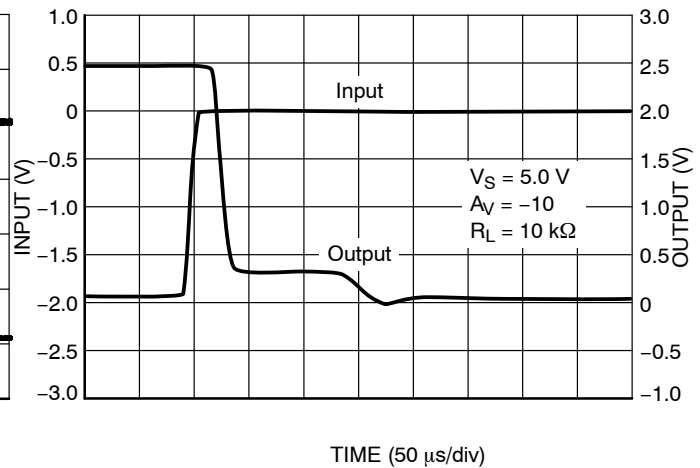


Figure 10. Positive Overtolerance Recovery

TYPICAL CHARACTERISTICS

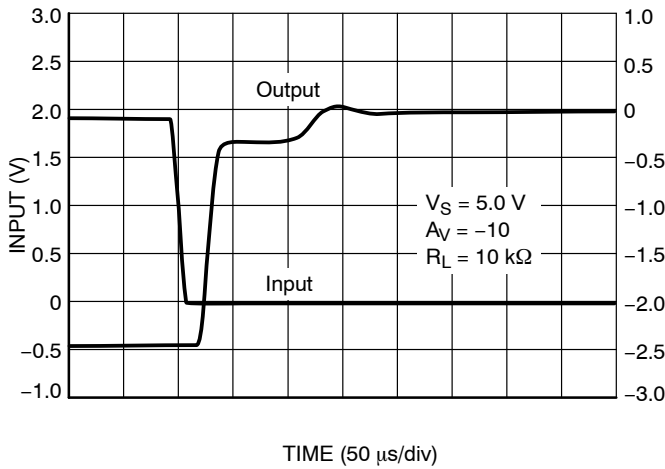


Figure 11. Negative Overtolerance Recovery

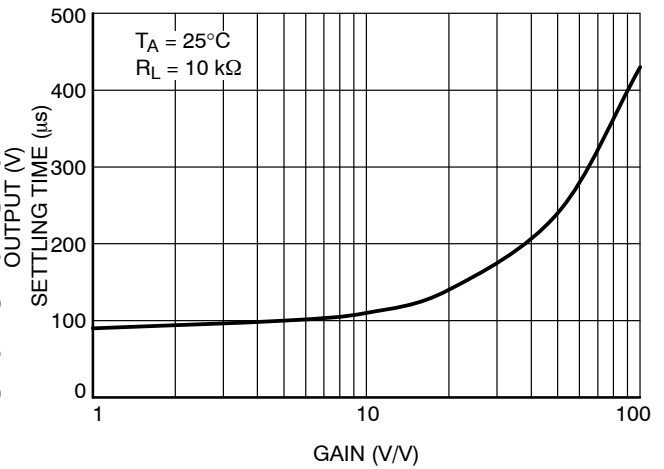


Figure 12. Settling Time to 0.1% vs. Closed-Loop Gain

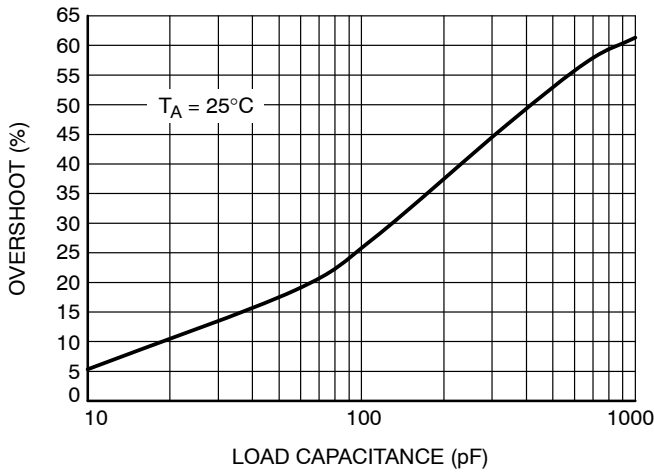


Figure 13. Small-Signal Overshoot vs. Load Capacitance

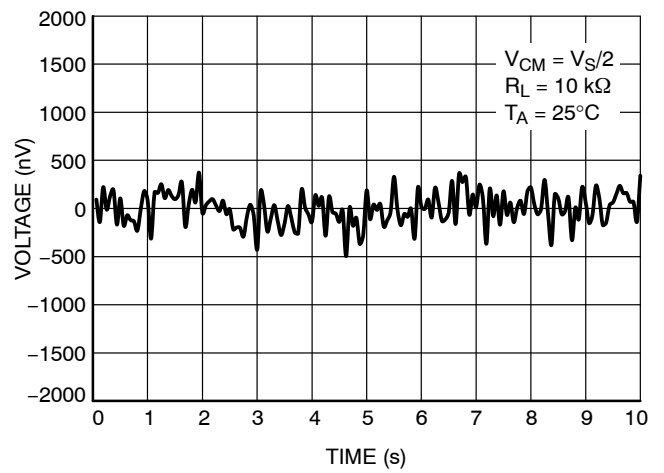


Figure 14. 0.1 Hz to 10 Hz Noise

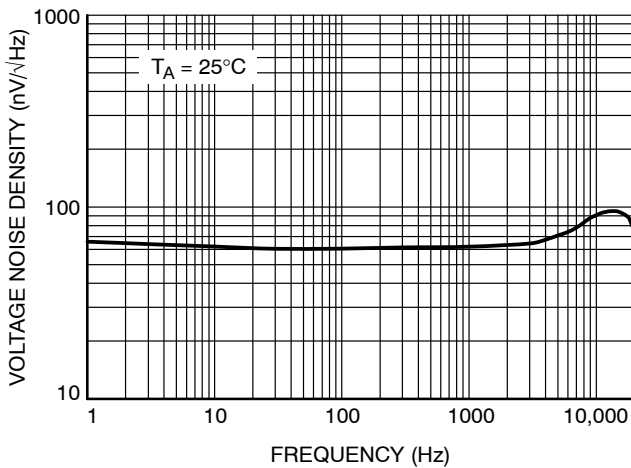


Figure 15. Voltage Noise Density vs. Frequency

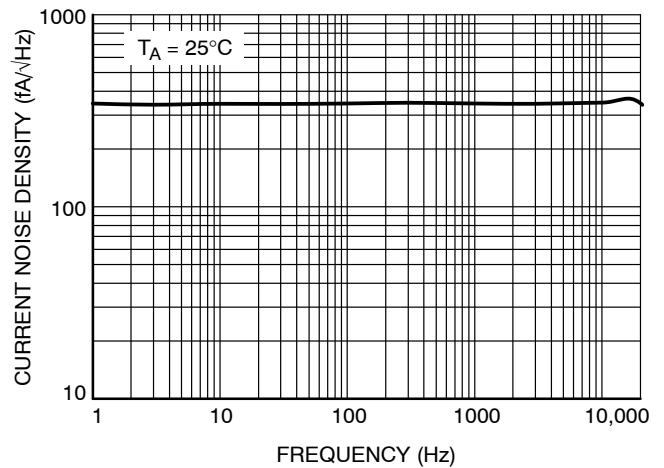


Figure 16. Current Noise Density vs. Frequency

APPLICATIONS INFORMATION

OVERVIEW

The NCS333, NCS333A, NCS2333, and NCS4333 precision op amps provide low offset voltage and zero drift over temperature. The input common mode voltage range extends 100 mV beyond the supply rails to allow for sensing near ground or VDD. These features make the NCS333 series well-suited for applications where precision is required, such as current sensing and interfacing with sensors.

NCS333 series of precision op amps uses a chopper-stabilized architecture, which provides the advantage of minimizing offset voltage drift over temperature and time. The simplified block diagram is shown in Figure 17. Unlike the classical chopper architecture, the chopper stabilized architecture has two signal paths.

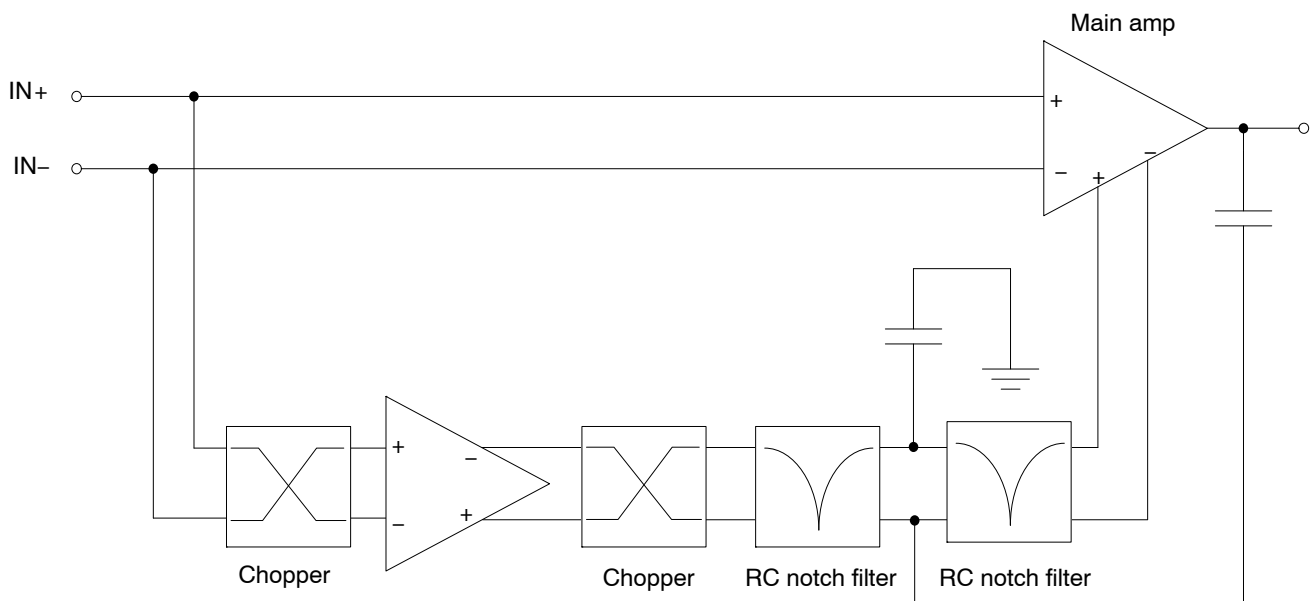


Figure 17. Simplified NCS333 Block Diagram

In Figure 17, the lower signal path is where the chopper samples the input offset voltage, which is then used to correct the offset at the output. The offset correction occurs at a frequency of 125 kHz. The chopper-stabilized architecture is optimized for best performance at frequencies up to the related Nyquist frequency (1/2 of the offset correction frequency). As the signal frequency exceeds the Nyquist frequency, 62.5 kHz, aliasing may occur at the output. This is an inherent limitation of all chopper and chopper-stabilized architectures. Nevertheless, the NCS333 op amps have minimal aliasing up to 125 kHz and low aliasing up to 190 kHz when compared to competitor parts from other manufacturers. ON Semiconductor’s patented approach utilizes two

cascaded, symmetrical, RC notch filters tuned to the chopper frequency and its fifth harmonic to reduce aliasing effects.

The chopper-stabilized architecture also benefits from the feed-forward path, which is shown as the upper signal path of the block diagram in Figure 17. This is the high speed signal path that extends the gain bandwidth up to 350 kHz. Not only does this help retain high frequency components of the input signal, but it also improves the loop gain at low frequencies. This is especially useful for low-side current sensing and sensor interface applications where the signal is low frequency and the differential voltage is relatively small.

APPLICATION CIRCUITS

Low-Side Current Sensing

Low-side current sensing is used to monitor the current through a load. This method can be used to detect over-current conditions and is often used in feedback control, as shown in Figure 18. A sense resistor is placed in series with the load to ground. Typically, the value of the

sense resistor is less than 100 mΩ to reduce power loss across the resistor. The op amp amplifies the voltage drop across the sense resistor with a gain set by external resistors R1, R2, R3, and R4 (where R1 = R2, R3 = R4). Precision resistors are required for high accuracy, and the gain is set to utilize the full scale of the ADC for the highest resolution.



Figure 18. Low-Side Current Sensing

Differential Amplifier for Bridged Circuits

Sensors to measure strain, pressure, and temperature are often configured in a Wheatstone bridge circuit as shown in Figure 19. In the measurement, the voltage change that is

produced is relatively small and needs to be amplified before going into an ADC. Precision amplifiers are recommended in these types of applications due to their high gain, low noise, and low offset voltage.

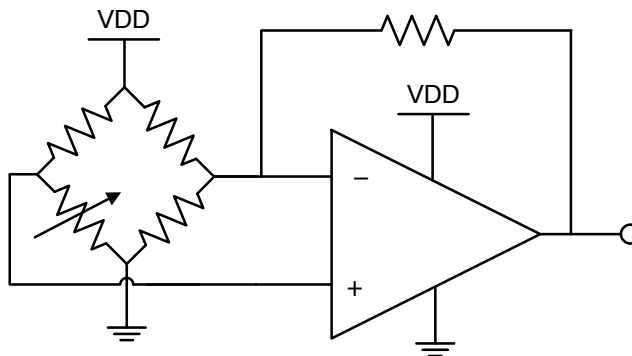


Figure 19. Bridge Circuit Amplification

EMI Susceptibility and Input Filtering

Op amps have varying amounts of EMI susceptibility. Semiconductor junctions can pick up and rectify EMI signals, creating an EMI-induced voltage offset at the output, adding another component to the total error. Input pins are the most sensitive to EMI. The NCS333 op amp family integrates low-pass filters to decrease sensitivity to EMI.

General Layout Guidelines

To ensure optimum device performance, it is important to follow good PCB design practices. Place 0.1 μF decoupling capacitors as close as possible to the supply pins. Keep traces short, utilize a ground plane, choose surface-mount components, and place components as close as possible to the device pins. These techniques will reduce susceptibility to electromagnetic interference (EMI). Thermoelectric effects can create an additional temperature dependent offset voltage at the input pins. To reduce these effects, use metals with low thermoelectric-coefficients and prevent temperature gradients from heat sources or cooling fans.

NCS333A, NCV333A, NCS2333, NCV2333, NCS4333, NCV4333, NCS333

UDFN8 Package Guidelines

The UDFN8 package has an exposed leadframe die pad on the underside of the package. This pad should be soldered to the PCB, as shown in the recommended soldering footprint in the Package Dimensions section of this datasheet. The

center pad can be electrically connected to VSS or it may be left floating. When connected to VSS, the center pad acts as a heat sink, improving the thermal resistance of the part.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



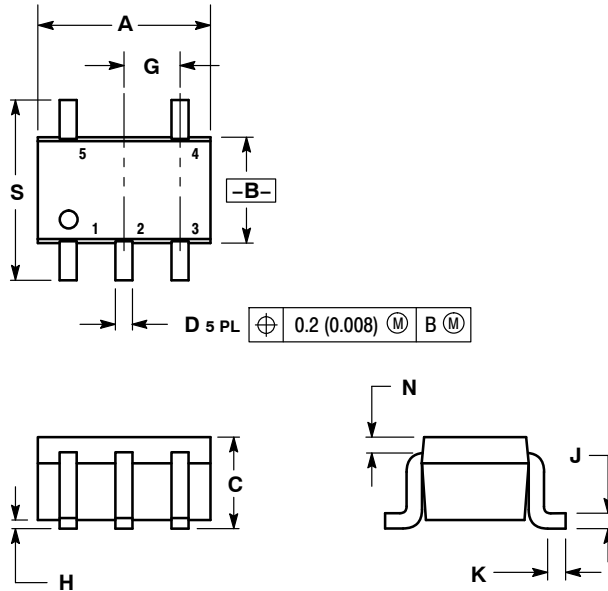
SC-88A (SC-70-5/SOT-353)

CASE 419A-02

ISSUE L

SCALE 2:1

DATE 17 JAN 2013

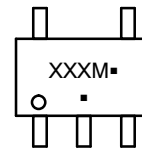


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.071 | 0.087 | 1.80 | 2.20 |
| B | 0.045 | 0.053 | 1.15 | 1.35 |
| C | 0.031 | 0.043 | 0.80 | 1.10 |
| D | 0.004 | 0.012 | 0.10 | 0.30 |
| G | 0.026 BSC | | 0.65 BSC | |
| H | --- | 0.004 | --- | 0.10 |
| J | 0.004 | 0.010 | 0.10 | 0.25 |
| K | 0.004 | 0.012 | 0.10 | 0.30 |
| N | 0.008 REF | | 0.20 REF | |
| S | 0.079 | 0.087 | 2.00 | 2.20 |

GENERIC MARKING DIAGRAM*

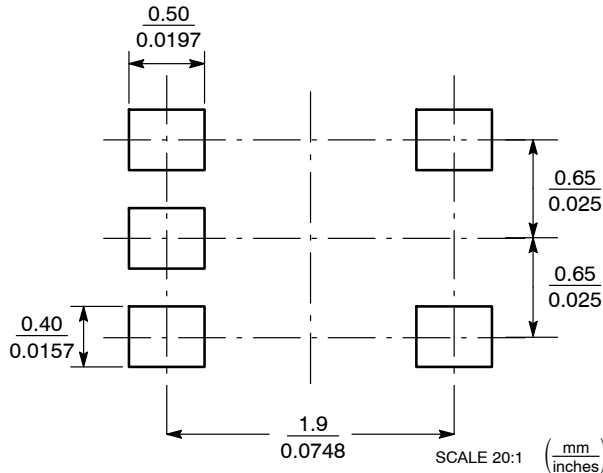


- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.

SOLDER FOOTPRINT



- STYLE 1:
 PIN 1. BASE
 2. EMITTER
 3. BASE
 4. COLLECTOR
 5. COLLECTOR

- STYLE 2:
 PIN 1. ANODE
 2. EMITTER
 3. BASE
 4. COLLECTOR
 5. CATHODE

- STYLE 3:
 PIN 1. ANODE 1
 2. N/C
 3. ANODE 2
 4. CATHODE 2
 5. CATHODE 1

- STYLE 4:
 PIN 1. SOURCE 1
 2. DRAIN 1/2
 3. SOURCE 1
 4. GATE 1
 5. GATE 2

- STYLE 5:
 PIN 1. CATHODE
 2. COMMON ANODE
 3. CATHODE 2
 4. CATHODE 3
 5. CATHODE 4

- STYLE 6:
 PIN 1. EMITTER 2
 2. BASE 2
 3. EMITTER 1
 4. COLLECTOR
 5. COLLECTOR 2/BASE 1

- STYLE 7:
 PIN 1. BASE
 2. EMITTER
 3. BASE
 4. COLLECTOR
 5. COLLECTOR

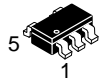
- STYLE 8:
 PIN 1. CATHODE
 2. COLLECTOR
 3. N/C
 4. BASE
 5. EMITTER

- STYLE 9:
 PIN 1. ANODE
 2. CATHODE
 3. ANODE
 4. ANODE
 5. ANODE

| | | |
|-------------------------|----------------------------------|--|
| DOCUMENT NUMBER: | 98ASB42984B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| STATUS: | ON SEMICONDUCTOR STANDARD | |
| NEW STANDARD: | | |
| DESCRIPTION: | SC-88A (SC-70-5/SOT-353) | PAGE 1 OF 2 |

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

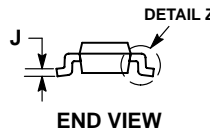
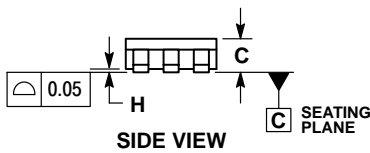
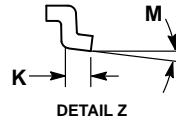
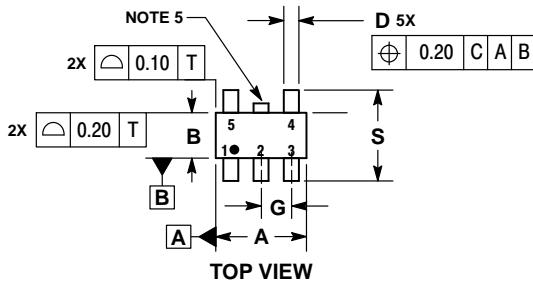
ON Semiconductor®



SCALE 2:1

TSOP-5 CASE 483 ISSUE M

DATE 17 MAY 2016

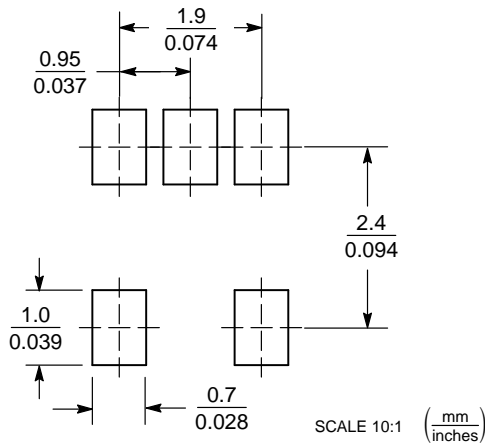


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

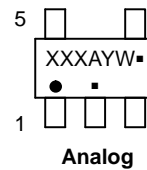
| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 2.85 | 3.15 |
| B | 1.35 | 1.65 |
| C | 0.90 | 1.10 |
| D | 0.25 | 0.50 |
| G | 0.95 BSC | |
| H | 0.01 | 0.10 |
| J | 0.10 | 0.26 |
| K | 0.20 | 0.60 |
| M | 0° | 10° |
| S | 2.50 | 3.00 |

SOLDERING FOOTPRINT*

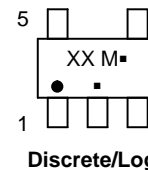


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



Analog



Discrete/Logic

- XXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package
- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package


(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

| | | |
|------------------|---------------------------|--|
| DOCUMENT NUMBER: | 98ARB18753C | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| STATUS: | ON SEMICONDUCTOR STANDARD | |
| NEW STANDARD: | | |
| DESCRIPTION: | TSOP-5 | PAGE 1 OF 2 |



| ISSUE | REVISION | DATE |
|-------|---|-------------|
| O | INITIATED NEW MECHANICAL OUTLINE #483. REQ BY WL CHIN/L. RENNICK. | 28 OCT 1998 |
| A | UPDATE OUTLINE DRAWING TO CORRECT DIN "C" (SHOULD BE FROM TIP OF LID TO TOP OF PKG). DIM IN TABLE INCORRECTLY LISTED TO G, F TO H, H TO J, N TO L & R TO M. REQ BY F. PADILLA | 13 NOV 1998 |
| B | CHANGE OF LEGAL ONWERSHIP FROM MOTOROLA TO ON SEMICONDUCTOR. REQ BY A. GARLINGTON | 20 APR 2001 |
| C | ADDED NOTE "4". REQ BY S. RIGGS | 27 JUN 2003 |
| D | ADDED FOOTPRINT INFORMATION. UPDATED MARKING. REQ. BY D. JOERSZ | 07 APR 2005 |
| E | CHANGED DEVICE MARKING FROM AWW TO AYW. REQ. BY J. MANES. | 14 SEP 2005 |
| F | UPDATED DRAWINGS TO LATEST JEDEC STANDARDS. ADDED NOTE 5. REQ. BY T. GURNETT. | 07 JUN 2006 |
| G | ADDED MARKING DIAGRAM FOR IC OPTION. REQ. BY J. MILLER. | 21 FEB 2007 |
| H | CORRECTED MARKING DIAGRAM ERROR BY REVERSING ANALOG AND DISCRETE LABELS. REQ. BY GK SUA. | 18 MAY 2007 |
| J | CHANGED NOTE 4. REQ. BY A. GARLINGTON. | 13 MAR 2013 |
| K | REMOVED DIMENSION L AND ADDED DATUMS A AND B TO TOP VIEW. REQ. BY A. GARLINGTON. | 19 APR 2013 |
| L | REMOVED -02 FROM CASE CODE VARIANT. REQ. BY N. CALZADA. | 23 SEP 2015 |
| M | CHANGED DIMENSIONS A & B FROM BASIC TO MIN AND MAX VALUES. REQ. BY A. GARLINGTON. | 17 MAY 2016 |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

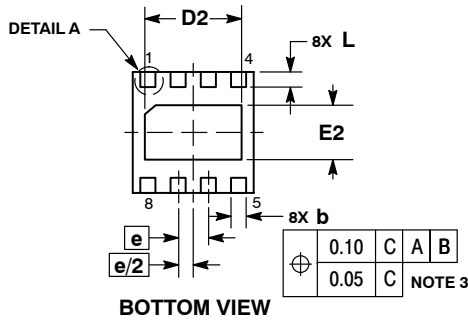
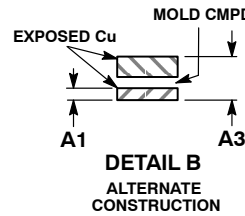
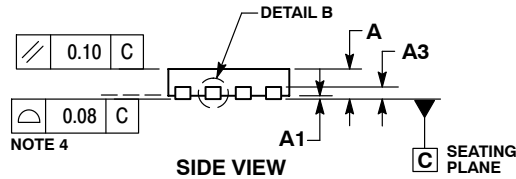
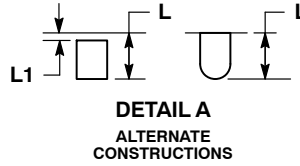
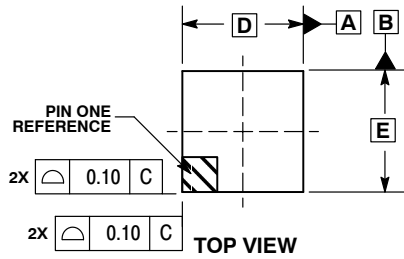
ON Semiconductor®



SCALE 2:1

UDFN8, 2x2
CASE 517AW
ISSUE A

DATE 13 NOV 2015

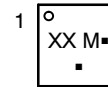


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. FOR DEVICE OPN CONTAINING W OPTION, DETAIL B ALTERNATE CONSTRUCTION IS NOT APPLICABLE.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.45 | 0.55 |
| A1 | 0.00 | 0.05 |
| A3 | 0.13 REF | |
| b | 0.18 | 0.30 |
| D | 2.00 BSC | |
| D2 | 1.50 | 1.70 |
| E | 2.00 BSC | |
| E2 | 0.80 | 1.00 |
| e | 0.50 BSC | |
| L | 0.20 | 0.45 |
| L1 | --- | 0.15 |

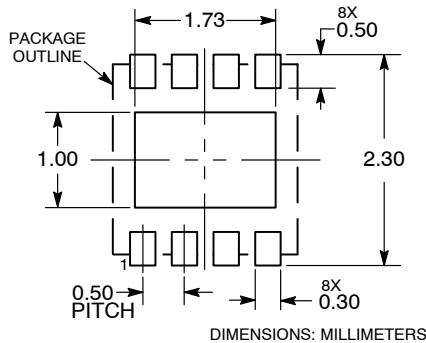
GENERIC MARKING DIAGRAM*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|------------------|-------------|--|
| DOCUMENT NUMBER: | 98AON34462E | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | UDFN8, 2X2 | PAGE 1 OF 1 |

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 W = Work Week
 ■ = Pb-Free Package

XXXXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

| | | |
|------------------|-------------|--|
| DOCUMENT NUMBER: | 98ASB42564B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | SOIC-8 NB | PAGE 1 OF 2 |

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|--|---|---|---|
| <p>STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER</p> | <p>STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1</p> | <p>STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1</p> | <p>STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE</p> |
| <p>STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE</p> | <p>STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE</p> | <p>STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd</p> | <p>STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1</p> |
| <p>STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON</p> | <p>STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND</p> | <p>STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1</p> | <p>STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> |
| <p>STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> | <p>STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN</p> | <p>STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON</p> | <p>STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC</p> | <p>STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE</p> | <p>STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1</p> | <p>STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN</p> |
| <p>STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6</p> | <p>STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND</p> | <p>STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT</p> | <p>STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT</p> | <p>STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC</p> | <p>STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN</p> | <p>STYLE 28: PIN 1. SW_TO_GND 2. DASIC OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN</p> |
| <p>STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1</p> | <p>STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1</p> | | |

| | | |
|-------------------------|--------------------|---|
| DOCUMENT NUMBER: | 98ASB42564B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | SOIC-8 NB | PAGE 2 OF 2 |

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

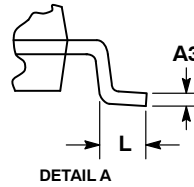
ON Semiconductor®



SCALE 1:1

SOIC-14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0° | 7° | 0° | 7° |

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLES ON PAGE 2

| | | |
|------------------|-------------|--|
| DOCUMENT NUMBER: | 98ASB42565B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | SOIC-14 NB | PAGE 1 OF 2 |

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. NO CONNECTION
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 2:
 CANCELLED

STYLE 3:
 PIN 1. NO CONNECTION
 2. ANODE
 3. ANODE
 4. NO CONNECTION
 5. ANODE
 6. NO CONNECTION
 7. ANODE
 8. ANODE
 9. ANODE
 10. NO CONNECTION
 11. ANODE
 12. ANODE
 13. NO CONNECTION
 14. COMMON CATHODE

STYLE 4:
 PIN 1. NO CONNECTION
 2. CATHODE
 3. CATHODE
 4. NO CONNECTION
 5. CATHODE
 6. NO CONNECTION
 7. CATHODE
 8. CATHODE
 9. CATHODE
 10. NO CONNECTION
 11. CATHODE
 12. CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 5:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. COMMON ANODE
 8. COMMON CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 6:
 PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. ANODE
 9. ANODE
 10. ANODE
 11. ANODE
 12. ANODE
 13. ANODE
 14. ANODE

STYLE 7:
 PIN 1. ANODE/CATHODE
 2. COMMON ANODE
 3. COMMON CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. COMMON CATHODE
 12. COMMON ANODE
 13. ANODE/CATHODE
 14. ANODE/CATHODE

STYLE 8:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. COMMON ANODE
 8. COMMON ANODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. NO CONNECTION
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. COMMON CATHODE

| | | |
|-------------------------|--------------------|---|
| DOCUMENT NUMBER: | 98ASB42565B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | SOIC-14 NB | PAGE 2 OF 2 |

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

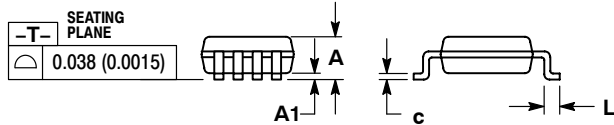
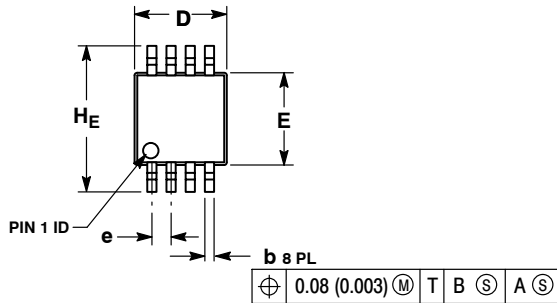
ON Semiconductor®



Micro8™
CASE 846A-02
ISSUE J

SCALE 2:1

DATE 02 JUL 2013

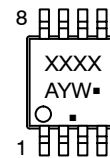


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A-01 OBSOLETE, NEW STANDARD 846A-02.

| DIM | MILLIMETERS | | | INCHES | | |
|-----|-------------|------|------|-----------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | --- | --- | 1.10 | --- | --- | 0.043 |
| A1 | 0.05 | 0.08 | 0.15 | 0.002 | 0.003 | 0.006 |
| b | 0.25 | 0.33 | 0.40 | 0.010 | 0.013 | 0.016 |
| c | 0.13 | 0.18 | 0.23 | 0.005 | 0.007 | 0.009 |
| D | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| E | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| e | 0.65 BSC | | | 0.026 BSC | | |
| L | 0.40 | 0.55 | 0.70 | 0.016 | 0.021 | 0.028 |
| HE | 4.75 | 4.90 | 5.05 | 0.187 | 0.193 | 0.199 |

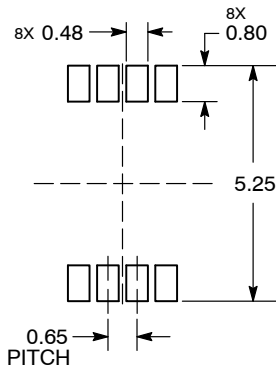
GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
 - A = Assembly Location
 - Y = Year
 - W = Work Week
 - = Pb-Free Package
- (Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLE 1:

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:

1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:

1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

| | | |
|------------------|-------------|--|
| DOCUMENT NUMBER: | 98ASB14087C | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | MICRO8 | PAGE 1 OF 1 |

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:
Voice Mail: 1 800-282-9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative