LDO Regulator, 150 mA, 38 V, Low Noise, ADJ/FIX, with PG

Product Preview

NCP731

The NCP731 device is based on unique combination of features – very low noise, low quiescent current, fast transient response and high input and output voltage ranges. The NCP731 is CMOS LDO regulator designed for up to 38 V input voltage and 150 mA output current. Very low noise (10 μV_{RMS}) makes this device an ideal solution for application where clean voltage rails are critical for system performance (power operational amplifiers, analog−to−digital / digital−to−analog converters and other precision analog circuitry).

The device version B (available on request) implements power good circuit (PG) which indicates that output voltage is in regulation. This signal could be used for power sequencing or as a microcontroller reset signal.

Internal short circuit and over temperature protections saves the device against overload conditions.

Features

- Operating Input Voltage Range: 2.7 V to 38 V
- Output Voltage Adjustable Range: 1.2 V to 35 V
- Fixed Output Voltage Versions: 3.3 V and 5.0 V (other voltage versions on request)
- Very Low Noise: 10 μV_{RMS} (10 Hz to 100 kHz)
- Low Quiescent Current: 50 μA typ.
- Low Shutdown Current: 100 nA typ.
- Low Dropout: 290 mV typ. at 150 mA
- Output Voltage Accuracy ±0.6% (25°C)
- Programmable Soft Start Circuit
- Power Good Output with Programmable Delay Time (device version B – available on request)
- Stable with Small 1 μF Ceramic Capacitors
- Over−Current and Thermal Shutdown Protections
- Available in Micro−8 EP Package
- Device is Pb−Free and RoHS Compliant

Typical Applications

- Supply Rails for OpAmps, ADCs, DACs and other Precision Analog Circuitry and Audio
- Post DC−DC Converter Regulation and Ripple Filtering
- Test and Measurement
- Industrial Instrumentation
- Metering
- Battery Powered Devices

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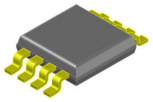
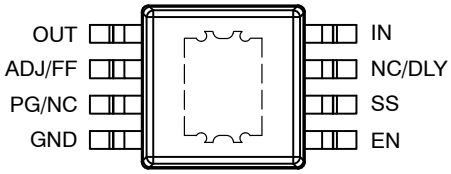


Micro8 EP
CASE 846AT

MARKING DIAGRAM

XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Code

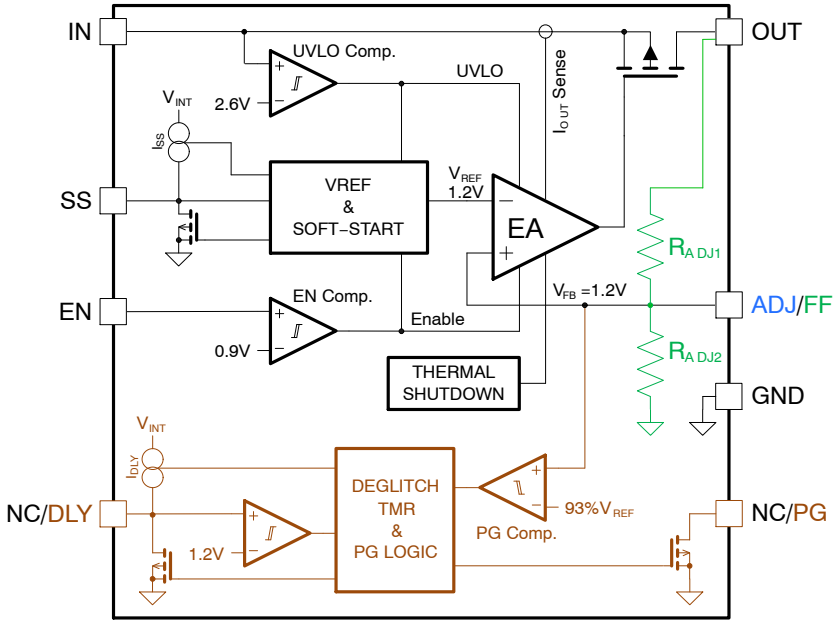
PIN ASSIGNMENTS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.



Notes:
Blue objects are valid for ADJ version only
Green objects are valid for FIX version only
Brown objects are valid for B version (with PG) only
Black objects are common for all version

Figure 1. Internal Block Diagram

PIN DESCRIPTION

Pin Number	Pin Name	Description
8	IN	Power supply input pin.
4	GND	Ground pin.
1	OUT	LDO output pin.
5	EN	Enable input pin (high = enable, low = disable). If this pin is not needed it should be conned to IN pin. No internal pull−up or pull−down circuit is present.
2	ADJ/FF	ADJ version − pin is ADJ • Adjust input pin. Could be connected directly or by the resistor divider to the output pin. FIX versions − pin is FF • Feed forward capacitor pin. Could be connected by C_{FF} capacitor to OUT pin for better dynamic performance & lower noise or left unconnected.
3	NC/PG	Device version A (without PG) − pin is NC • Not internally connected. Could be left unconnected or connected to GND. Device version B (with PG) − pin is PG • Power good output pin. High impedance for power ok, low level for fail. Could be left unconnected or connected to GND if not used.
7	NC/DLY	Device version A (without PG) − pin is NC • Not internally connected. Could be left unconnected or connected to GND. Device version B (with PG) − pin is DLY • Power good delay pin. Connect a C_{DLY} capacitor to set delay time. Could be left floating if not used.
6	SS	Soft−start input pin. Connect a C_{SS} capacitor to set soft−start time. Could be left floating if not used.
EP	EPAD	Exposed pad, must be connected to GND.

TYPICAL APPLICATION SCHEMATICS

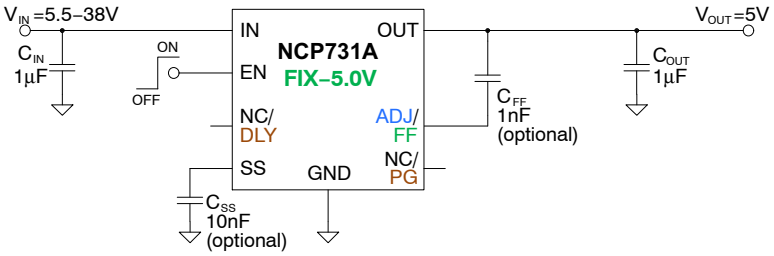


Figure 2. Fixed Output Voltage Application, 5 V, Device Version−A (without PG)

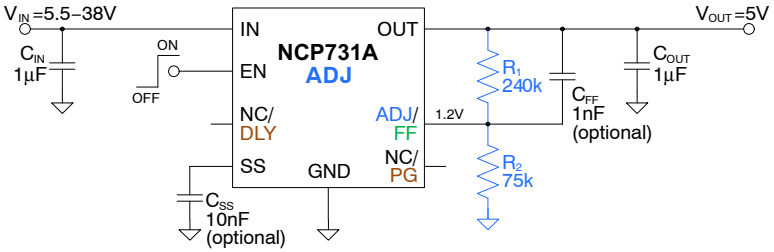


Figure 3. Adjustable Output Voltage Application, 5 V, Device Version−A (without PG)

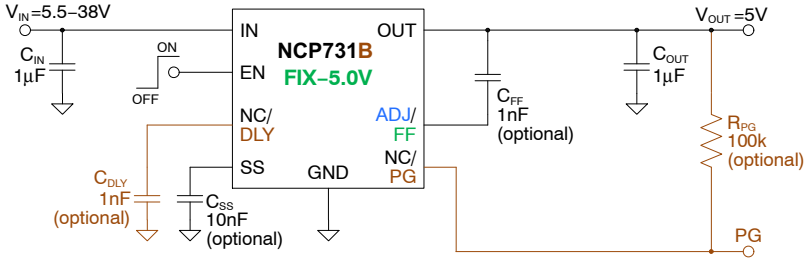


Figure 4. Fixed Output Voltage Application, 5 V, Device Version−B (with PG)

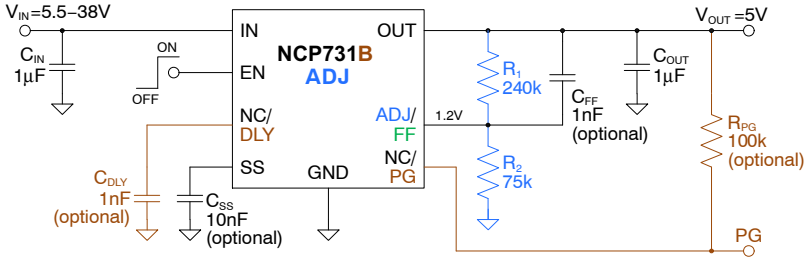


Figure 5. Adjustable Output Voltage Application, 5 V, Device Version−B (with PG)

Notes:
Blue objects are valid for ADJ version only
Green objects are valid for FIX version only
Brown objects are valid for B version (with PG) only
Black objects are common for all version

Table 1. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IN Voltage (Note 1)	V_{IN}	−0.3 to 40	V
OUT Voltage	V_{OUT}	−0.3 to [(V_{IN} + 0.3) or 40 V; whichever is lower]	V
EN Voltage	V_{EN}	−0.3 to (V_{IN} + 0.3)	V
ADJ/FF Voltage	V_{ADJ}	−0.3 to 5.5	V
SS Voltage	V_{SS}	−0.3 to 5.5	V
PG Voltage	V_{PG}	−0.3 to (V_{IN} + 0.3)	V
DLY Voltage	V_{DLY}	−0.3 to 5.5	V
Output Current	I_{OUT}	Internally limited	mA
PG Current	I_{PG}	3	mA
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Charged Device Model (Note 2)	ESD_{CDM}	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per ANSI/ESDA/JEDEC JS−001, EIA/JESD22−A114
   ESD Charged Device Model tested per ANSI/ESDA/JEDEC JS−002, EIA/JESD22−C101

Table 2. THERMAL CHARACTERISTICS (Note 3)

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	47	°C/W
Thermal Resistance, Junction−to−Case (top)	$R_{\theta JCt}$	TBD	°C/W
Thermal Resistance, Junction−to−Case (bottom)	$R_{\theta JCb}$	TBD	°C/W
Thermal Resistance, Junction−to−Board (top)	$R_{\theta JBt}$	TBD	°C/W
Thermal Characterization Parameter, Junction−to−Case (top)	Ψ_{JCt}	TBD	°C/W
Thermal Characterization Parameter, Junction−to−Board [FEM]	Ψ_{JB}	TBD	°C/W

3. Measured according to JEDEC board specification (board 1S2P, Cu layer thickness 1 oz, Cu area 650 mm^2, no airflow). Detailed description of the board can be found in JESD51−7.

Table 3. ELECTRICAL CHARACTERISTICS $V_{IN} = V_{OUT-NOM}$ + 1 V and $V_{IN} \geq$ 2.7 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 1.0 μF (Note 4), C_{SS} = 0 nF, C_{FF} = 0 nF, T_J = −40°C to 125°C, ADJ tied to OUT, unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Recommended Input Voltage		V_{IN}	2.7	–	38	V
Output Voltage Accuracy	T_J = +25°C	V_{OUT}	−0.6	–	0.6	%
	$V_{IN} = V_{OUT-NOM}$ + 1 V to 38 V I_{OUT} = 0.1 mA to 150 mA T_J = −40°C to +125°C		−1.5	–	1.5	
Output Voltage Range		V_{OUT}	V_{ADJ}	–	35	V
ADJ Reference Voltage		V_{ADJ}	–	1.2	–	V
ADJ Input Current	V_{ADJ} = 1.2 V	I_{ADJ}	−0.1	0.01	0.1	μA
Quiescent Current	$V_{IN} = V_{OUT-NOM}$ + 1 V to 38 V, I_{OUT} = 0 mA	I_Q	–	48	100	μA
Ground Current	I_{OUT} = 150 mA	I_{GND}	–	500	–	μA
Shutdown Current	V_{EN} = 0 V, V_{IN} = 38 V	I_{SHDN}	–	0.2	1.5	μA
Output Current Limit	$V_{OUT} = V_{OUT-NOM}$ − 100 mV	I_{OLIM}	210	280	450	mA
Short Circuit Current	V_{OUT} = 0 V	I_{OSC}	210	280	450	mA

Table 3. ELECTRICAL CHARACTERISTICS $V_{IN} = V_{OUT-NOM} + 1$ V and $V_{IN} \geq 2.7$ V, $V_{EN} = 1.2$ V, $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 1.0$ μF (Note 4), $C_{SS} = 0$ nF, $C_{FF} = 0$ nF, $T_J = -40°C$ to 125°C, ADJ tied to OUT, unless otherwise specified.

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Dropout Voltage (Note 5)	I_{OUT} = 150 mA		V_{DO}	–	290	480	mV
Power Supply Ripple Rejection	$V_{IN} = V_{OUT-NOM} + 2$ V, I_{OUT} = 10 mA	10 Hz	PSRR	–	80	–	dB
		10 kHz		–	70	–	
		100 kHz		–	42	–	
		1 MHz		–	48	–	
Output Noise Voltage	f = 10 Hz to 100 kHz, ADJ version, $V_{OUT} = V_{ADJ}$, C_{FF} = 1 nF		V_N	–	10	–	μVRMS
	f = 10 Hz to 100 kHz, FIX version, V_{OUT} = 5 V, C_{FF} = 1 nF			–	TBD	–	
EN Threshold	V_{EN} rising		V_{EN-TH}	0.7	0.9	1.1	V
EN Hysteresis	V_{EN} falling		V_{EN-HY}	0.02	0.1	0.2	V
EN Input Current	V_{EN} = 30 V, V_{IN} = 30 V		I_{EN}	–1	0.05	1	μA
Internal UVLO Threshold	V_{IN} voltage rising		$V_{UVLO-TH}$	2.51	2.6	2.69	V
Internal UVLO Hysteresis	V_{IN} voltage falling		$V_{UVLO-HY}$	0.01	0.05	0.09	V
SS Charging Current	V_{SS} = 0 V		I_{SS}	765	850	935	nA
SS High Voltage	SS pin floating		V_{SS-HI}	–	2.4	–	V
SS Time (Note 6)	C_{SS} = 10 nF		$t_{SS-10nF}$	–	14	–	ms
	C_{SS} not connected		t_{SS-0nF}	–	TBD	–	μs
DLY Charging Current (Note 7)	V_{DLY} = 0 V		I_{DLY}	–	1.2	–	μA
DLY High Voltage (Note 7)	DLY pin floating		V_{DLY-HI}	–	2.4	–	V
DLY Threshold Voltage (Note 7)	DLY voltage rising		V_{SS-TH}	1.1	1.2	1.3	V
DLY Hysteresis (Note 7)	DLY voltage falling		V_{SS-HY}	0.05	0.1	0.15	V
DLY Time (Note 7)	C_{DLY} = 10 nF		$t_{DLY-10nF}$	8	10	12	ms
	C_{DLY} not connected		$t_{DLY-0nF}$		TBD		μs
PG Threshold (Note 7)	V_{OUT} falling		V_{PG-TH}	90	93	96	%
PG Hysteresis (Note 7)	V_{OUT} rising		V_{PG-HY}	0.5	2	3.5	%
PG Deglitch Time (Note 7)			t_{PG-DG}	100	200	300	μs
PG Output Low Level Voltage (Note 7)	I_{PG} = 1 mA		V_{PG-LO}	–	0.2	0.4	V
PG Output Leakage Current (Note 7)	V_{PG} = 30 V		I_{PG-LK}	–	0.01	1	μA
Thermal Shutdown Temperature	Temperature rising from T_J = +25°C		T_{TSD}	–	170	–	°C
Thermal Shutdown Hysteresis	Temperature falling from TSD		T_{TSDH}	–	10	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

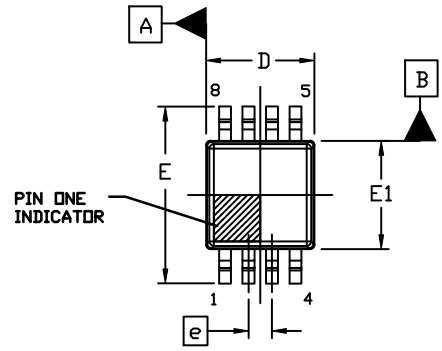
4. Effective capacitance, including the effect of DC bias, tolerance and temperature. See the Application Information section for more information.
5. Dropout measured when the output voltage falls 100 mV below the nominal output voltage. Limits are valid for all voltage versions.
6. Startup time is the time from EN assertion to point when output voltage is equal to 95% of $V_{OUT-NOM}$.
7. Applicable only to device version B (option with power good output). PG threshold and PG hysteresis are expressed in percentage of nominal output voltage.

ORDERING INFORMATION

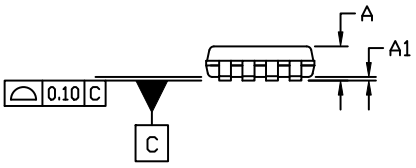
Part Number	Marking	Voltage Option ($V_{OUT-NOM}$)	Version	Package	Shipping
NCP731ADN330R2G	731A33	3.3 V	Without PG	Micro–8 EP (Pb–Free)	TBD
NCP731ADN500R2G	731A50	5.0 V			
NCP731ADNADJR2G	731AAD	ADJ			

PACKAGE DIMENSIONS

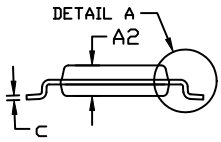
MSOP8 EP 3x3
CASE 846AT
ISSUE O



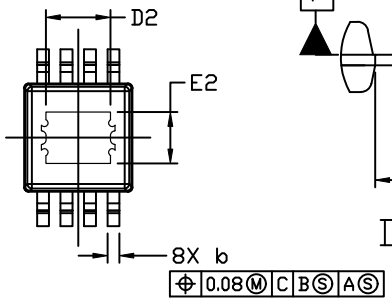
TOP VIEW



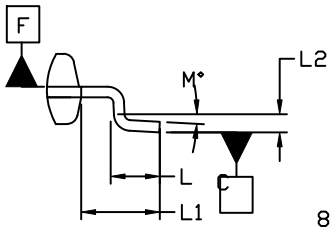
SIDE VIEW



END VIEW



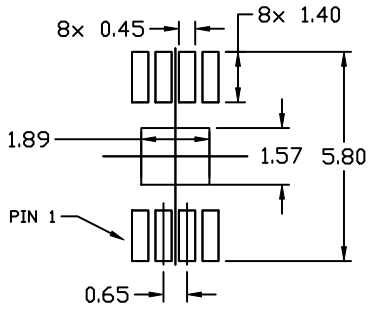
BOTTOM VIEW NOTE 3



DETAIL A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS b AND c APPLY TO THE PLATED LEADS.
5. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. PIN 1 INDICATOR IS LOCATED HERE. MAY APPEAR AS A LASER MARKED, OR A MOLDED (CIRCLE OR HALF MOON), INDENT.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.10	0.15
A2	0.813	0.863	0.914
b	0.28	---	0.38
c	0.139	---	0.23
D	2.90	3.00	3.10
D2	1.50	1.70	1.80
E	4.775	4.876	4.978
E1	2.90	3.00	3.10
E2	1.14	1.40	1.50
e	0.65 BSC		
L	0.40	---	---
L1	0.94 REF		
L2	0.25 REF		
M	0°	---	8°



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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