

LDO Regulator, 150 mA, 38 V, 1 μ A I_Q , with PG

Product Preview NCP730

The NCP730 device is based on unique combination of features – very low quiescent current, fast transient response and high input and output voltage ranges. The NCP730 is CMOS LDO regulator designed for up to 38 V input voltage and 150 mA output current. Quiescent current of only 1 μ A makes this device ideal solution for battery-powered, always-on systems. Several fixed output voltage versions are available as well as the adjustable version.

The device (version B) implements power good circuit (PG) which indicates that output voltage is in regulation. This signal could be used for power sequencing or as a microcontroller reset.

Internal short circuit and over temperature protections saves the device against overload conditions.

Features

- Operating Input Voltage Range: 2.7 V to 38 V
- Output Voltage: 1.2 V to 24 V
- Capable of Sourcing 200 mA Peak Output Current
- Low Shutdown Current: 100 nA typ.
- Very Low Quiescent Current: 1 μ A typ.
- Low Dropout: 290 mV typ. at 150 mA, 3.3 V Version
- Output Voltage Accuracy $\pm 1\%$
- Power Good Output (Version B)
- Stable with Small 1 μ F Ceramic Capacitors
- Built-in Soft Start Circuit to Suppress Inrush Current
- Over-Current and Thermal Shutdown Protections
- Available in Small TSOP-5 and WDFN6 (2x2) Packages
- These Devices are Pb-Free and are RoHS Compliant

Typical Applications

- Battery Power Tools and Equipment
- Home Automation
- RF Devices
- Metering
- Remote Control Devices
- White Goods

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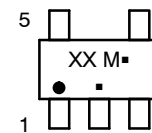


TSOP-5
CASE 483



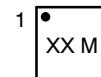
WDFN6 (2x2)
CASE 511BR

MARKING DIAGRAMS



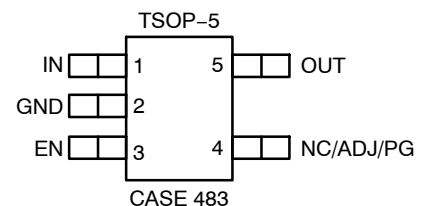
XX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

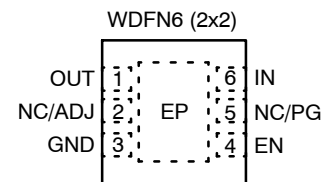


XX = Specific Device Code
M = Date Code

PIN ASSIGNMENTS



CASE 483



CASE511BR

(Top Views)

ORDERING INFORMATION

See detailed ordering and shipping information on page 24 of this data sheet.

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TYPICAL APPLICATION SCHEMATICS

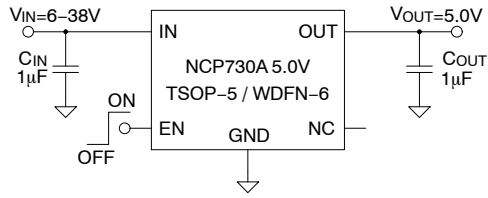


Figure 1. Fixed Output Voltage Application (No PG)

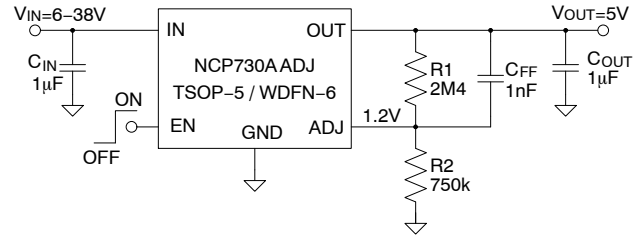


Figure 2. Adjustable Output Voltage Application (No PG)

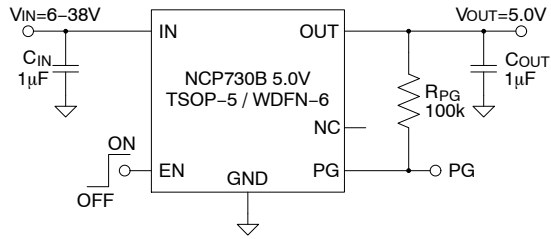


Figure 3. Fixed Output Voltage Application with PG

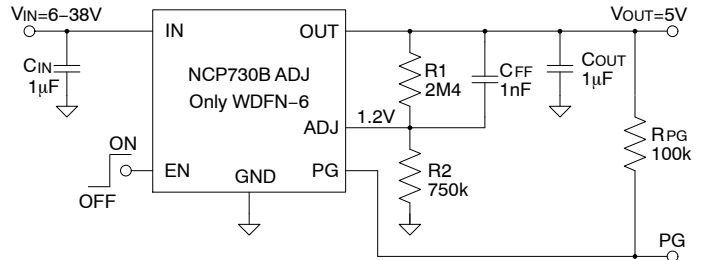
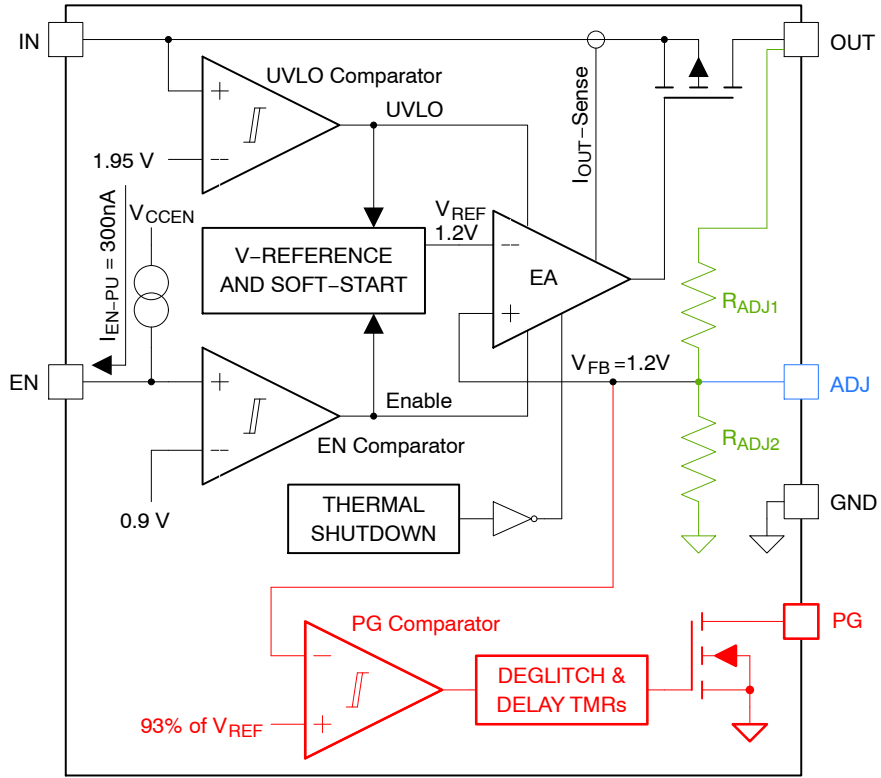


Figure 4. Adjustable Output Voltage Application with PG

$$V_{OUT} = V_{ADJ} \cdot \left(1 + \frac{R_1}{R_2} \right) + I_{ADJ} \cdot R_1$$

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SIMPLIFIED BLOCK DIAGRAMS



Note: Blue objects are valid for ADJ version
 Green objects are valid for FIX version
 Red objects are valid for B version (with PG)

Figure 5. Internal Block Diagram

PIN DESCRIPTION

Pin No. TSOP-5	Pin No. WDFN-6	Pin Name	Description
1	6	IN	Power supply input pin.
2	3	GND	Ground pin.
5	1	OUT	LDO output pin.
3	4	EN	Enable input pin (high – enabled, low – disabled). If this pin is connected to IN pin or if it is left unconnected (pull-up resistor is not required) the device is enabled.
4 (Note 1)	2	ADJ	Adjust input pin, could be connected to the resistor divider to the OUT pin.
4 (Note 1)	5	PG	Power good output pin. Could be left unconnected or could be connected to GND if not needed. High level for power ok, low level for fail.
4 (Note 1)	2, 5	NC	Not internally connected. This pin can be tied to the ground plane to improve thermal dissipation.
NA	EP	EPAD	Connect the exposed pad to GND.

1. Pin function depends on device version.

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
VIN Voltage (Note 2)	V _{IN}	-0.3 to 40	V
VOU _T Voltage	V _{OUT}	-0.3 to [(V _{IN} + 0.3) or 40 V; whichever is lower]	V
EN Voltage	V _{EN}	-0.3 to (V _{IN} + 0.3)	V
ADJ Voltage	V _{FB/ADJ}	-0.3 to 5.5	V
PG Voltage	V _{PG}	-0.3 to (V _{IN} + 0.3)	V
Output Current	I _{OUT}	Internally limited	mA
PG Current	I _{PG}	3	mA
Maximum Junction Temperature	T _{J(MAX)}	150	°C
Storage Temperature	T _{STG}	-55 to 150	°C
ESD Capability, Human Body Model (Note 3)	ESD _{HBM}	2000	V
ESD Capability, Charged Device Model (Note 3)	ESD _{CDM}	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

3. This device series incorporates ESD protection and is tested by the following methods:

ESD Human Body Model tested per ANSI/ESDA/JEDEC JS-001, EIA/JESD22-A114 (AEC-Q100-002)

ESD Charged Device Model tested per ANSI/ESDA/JEDEC JS-002, EIA/JESD22-C101 (AEC Q100-011D)

THERMAL CHARACTERISTICS (Note 4)

Characteristic	Symbol	WDFN6 2x2	TSOP-5	Unit
Thermal Resistance, Junction-to-Air	R _{thJA}	61	142	°C/W
Thermal Resistance, Junction-to-Case (top)	R _{thJCt}	200	80	°C/W
Thermal Resistance, Junction-to-Case (bottom)	R _{thJCb}	14	N/A	°C/W
Thermal Resistance, Junction-to-Board (top)	R _{thJBt}	46	110	°C/W
Thermal Characterization Parameter, Junction-to-Case (top)	Ψ _{iJCt}	3	21	°C/W
Thermal Characterization Parameter, Junction-to-Board [FEM]	Ψ _{iJB}	46	113	°C/W

4. Measured according to JEDEC board specification (board 1S2P, Cu layer thickness 1 oz, Cu area 650 mm², no airflow). Detailed description of the board can be found in JESD51-7.

ELECTRICAL CHARACTERISTICS (V_{IN} = V_{OUT-NOM} + 1 V and V_{IN} ≥ 2.7 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF (effective capacitance – Note 5), T_J = -40°C to 125°C, ADJ tied to OUT, unless otherwise specified) (Note 6)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Recommended Input Voltage		V _{IN}	2.7	-	38	V
Output Voltage Accuracy	T _J = -40°C to +85°C	V _{OUT}	-1	-	1	%
	T _J = -40°C to +125°C		-1	-	2	
ADJ Reference Voltage	ADJ version only	V _{ADJ}	-	1.2	-	V
ADJ Input Current	V _{ADJ} = 1.2 V	I _{ADJ}	-0.1	0.01	0.1	μA
Line Regulation	V _{IN} = V _{OUT-NOM} + 1 V to 38 V and V _{IN} ≥ 2.7 V	ΔV _{O(ΔVI)}	-	-	0.2	%V _{OUT}
Load Regulation	I _{OUT} = 0.1 mA to 150 mA	ΔV _{O(ΔIO)}	-	-	0.4	%V _{OUT}
Quiescent Current (version A)	V _{IN} = V _{OUT-NOM} + 1 V to 38 V, I _{OUT} = 0 mA	I _Q	-	1.3	2.5	μA
Quiescent Current (version B)	V _{IN} = V _{OUT-NOM} + 1 V to 38 V, I _{OUT} = 0 mA		-	1.8	3.0	
Ground Current	I _{OUT} = 150 mA	I _{GND}	-	325	450	μA
Shutdown Current (Note 10)	V _{EN} = 0 V, I _{OUT} = 0 mA, V _{IN} = 38 V	I _{SHDN}	-	0.35	1.5	μA
Output Current Limit	V _{OUT} = V _{OUT-NOM} - 100 mV	I _{OLIM}	200	280	450	mA
Short Circuit Current	V _{OUT} = 0 V	I _{OSC}	200	280	450	mA
Dropout Voltage (Note 7)	I _{OUT} = 150 mA	V _{DO}	-	290	480	mV

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ELECTRICAL CHARACTERISTICS ($V_{IN} = V_{OUT-NOM} + 1$ V and $V_{IN} \geq 2.7$ V, $V_{EN} = 1.2$ V, $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 1.0$ μ F (effective capacitance – Note 5), $T_J = -40^\circ\text{C}$ to 125°C , ADJ tied to OUT, unless otherwise specified) (Note 6) (continued)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit	
Power Supply Ripple Rejection	$V_{IN} = V_{OUT-NOM} + 2$ V $I_{OUT} = 10$ mA	10 Hz	PSRR	-	80	-	dB
		10 kHz		-	70	-	
		100 kHz		-	42	-	
		1 MHz		-	48	-	
Output Noise	$f = 10$ Hz to 100 kHz	V_N	-	100* V_{OUT}	-	μV_{RMS}	
EN Threshold	V_{EN} rising	V_{EN-TH}	0.7	0.9	1.05	V	
EN Hysteresis	V_{EN} falling	V_{EN-HY}	0.01	0.1	0.2	V	
EN Internal Pull-up Current	$V_{EN} = 1$ V, $V_{IN} = 5.5$ V	I_{EN-PU}	0.01	0.3	1	μA	
EN Input Leakage Current	$V_{EN} = 30$ V, $V_{IN} = 30$ V	I_{EN-LK}	-1	0.05	1	μA	
Start-up time (Note 8)	$V_{OUT-NOM} \leq 3.3$ V	t_{START}	100	250	500	μs	
	$V_{OUT-NOM} > 3.3$ V		300	600	1000		
Internal UVLO Threshold	Ramp V_{IN} up until output is turned on	V_{IUL-TH}	1.6	1.95	2.6	V	
Internal UVLO Hysteresis	Ramp V_{IN} down until output is turned off	V_{IUL-HY}	0.05	0.2	0.3	V	
PG Threshold (Note 9)	V_{OUT} falling	V_{PG-TH}	90	93	96	%	
PG Hysteresis (Note 9)	V_{OUT} rising	V_{PG-HY}	0.1	2	3.5	%	
PG Deglitch Time (Note 9)		t_{PG-DG}	75	160	270	μs	
PG Delay Time (Note 9)		t_{PG-DLY}	120	320	600	μs	
PG Output Low Level Voltage (Note 9)	$I_{PG} = 1$ mA	V_{PG-OL}	-	0.2	0.4	V	
PG Output Leakage Current (Note 9)	$V_{PG} = 30$ V	I_{PG-LK}	-	0.01	1	μA	
Thermal Shutdown Temperature	Temperature rising from $T_J = +25^\circ\text{C}$	T_{SD}	-	165	-	$^\circ\text{C}$	
Thermal Shutdown Hysteresis	Temperature falling from T_{SD}	T_{SDH}	-	20	-	$^\circ\text{C}$	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Effective capacitance, including the effect of DC bias, tolerance and temperature. See the Application Information section for more information.
6. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_A = 25^\circ\text{C}$. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
7. Dropout measured when the output voltage falls 100 mV below the nominal output voltage. Limits are valid for all voltage versions.
8. Startup time is the time from EN assertion to point when output voltage is equal to 95% of $V_{OUT-NOM}$.
9. Applicable only to version B (device option with power good output). PG threshold and PG hysteresis are expressed in percentage of nominal output voltage.
10. Shutdown current includes EN Internal Pull-up Current.

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TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM} + 1\text{ V}$ and $V_{IN} \geq 2.7\text{ V}$, $V_{EN} = 1.2\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$, ADJ tied to OUT, $T_J = 25^\circ\text{C}$, unless otherwise specified

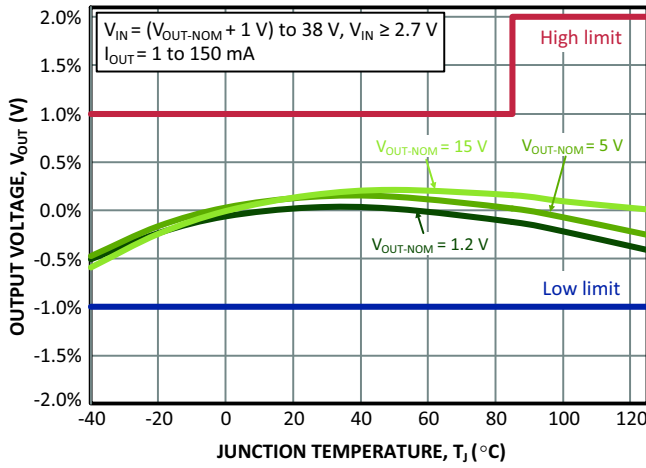


Figure 6. Output Voltage vs. Temperature

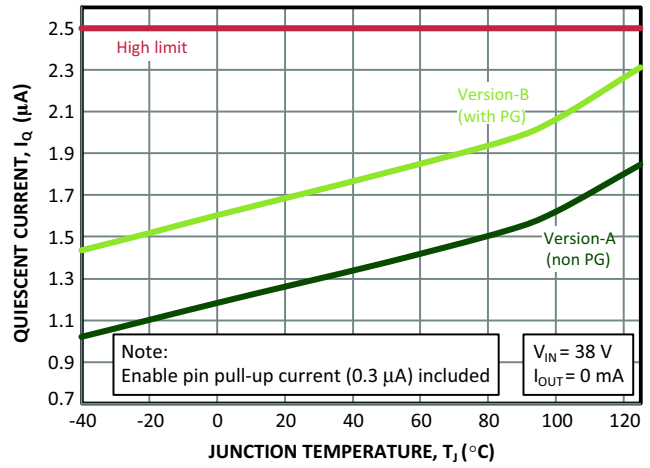


Figure 7. Quiescent Current vs. Temperature

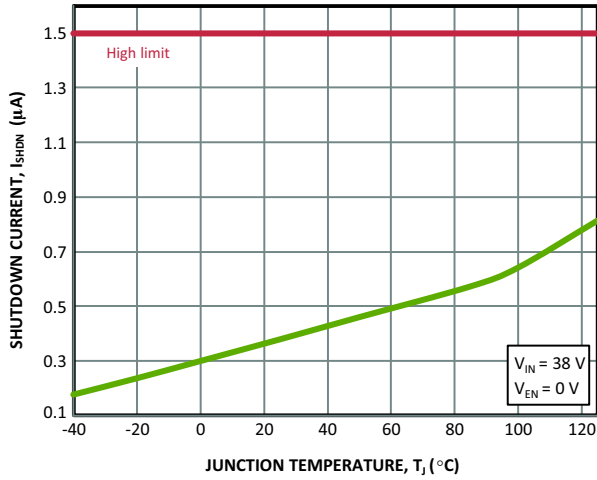


Figure 8. Shutdown Current vs. Temperature

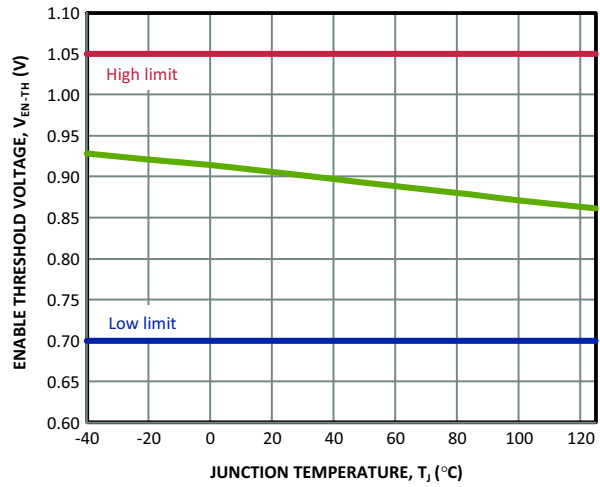


Figure 9. Enable Threshold Voltage vs. Temperature

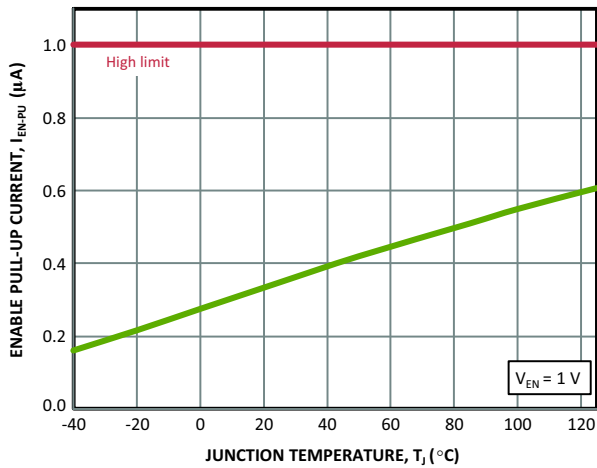


Figure 10. Enable Internal Pull-Up Current vs. Temperature

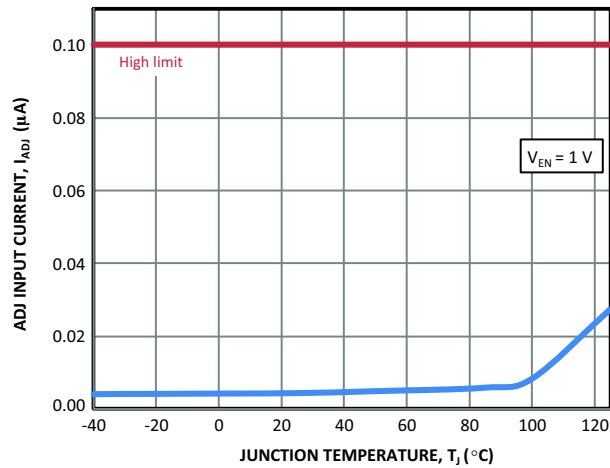


Figure 11. ADJ Input Current vs. Temperature

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TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM} + 1\text{ V}$ and $V_{IN} \geq 2.7\text{ V}$, $V_{EN} = 1.2\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$, ADJ tied to OUT, $T_J = 25^\circ\text{C}$, unless otherwise specified

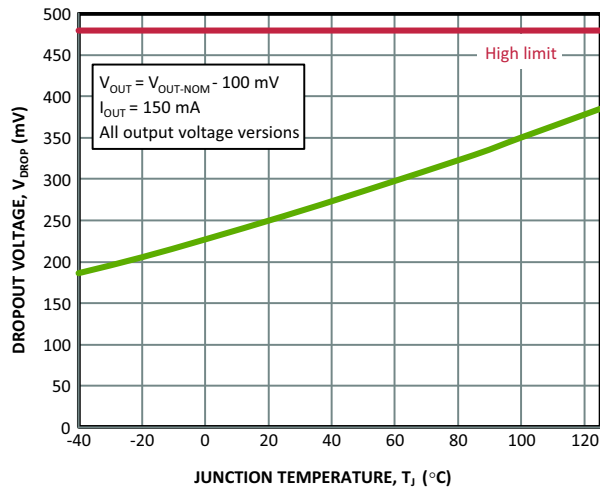


Figure 12. Dropout Voltage vs. Temperature

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TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM} + 1\text{ V}$ and $V_{IN} \geq 2.7\text{ V}$, $V_{EN} = 1.2\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$, ADJ tied to OUT, $T_J = 25^\circ\text{C}$, unless otherwise specified

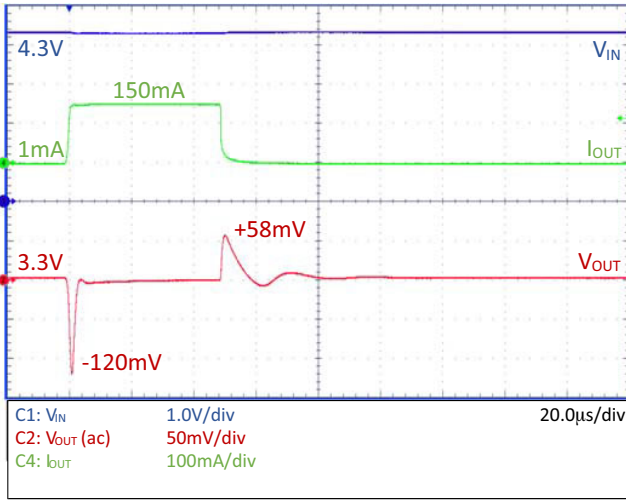


Figure 13. NCP730–3.3 V, $C_{OUT} = 1\text{ }\mu\text{F}$

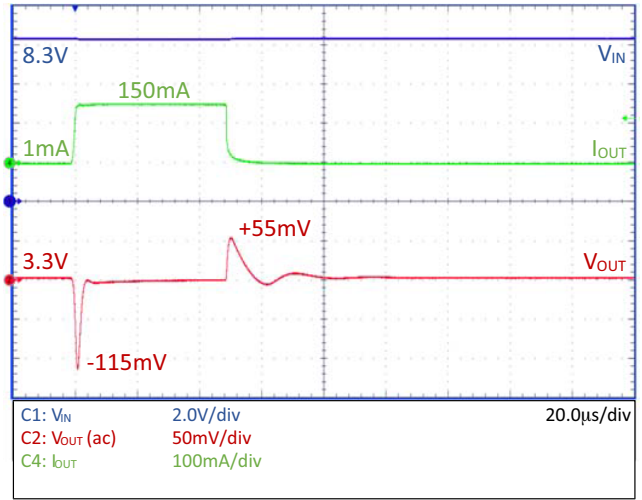


Figure 14. NCP730–3.3 V, $C_{OUT} = 1\text{ }\mu\text{F}$

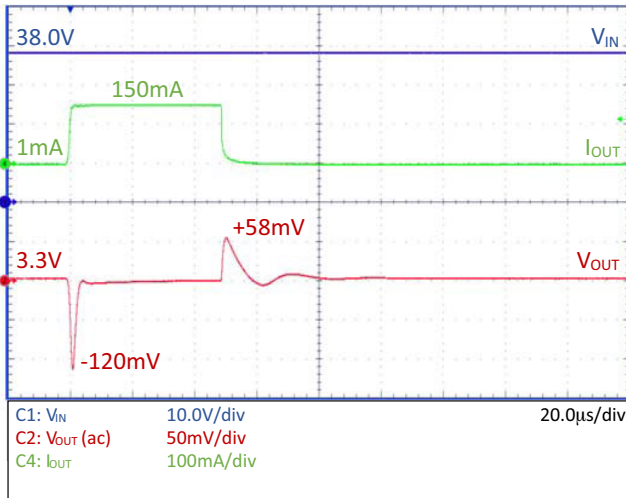


Figure 15. NCP730–3.3 V, $C_{OUT} = 1\text{ }\mu\text{F}$

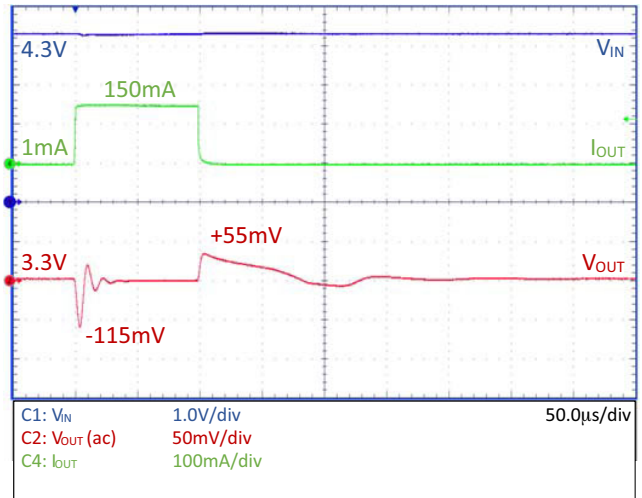


Figure 16. NCP730–3.3 V, $C_{OUT} = 10\text{ }\mu\text{F}$

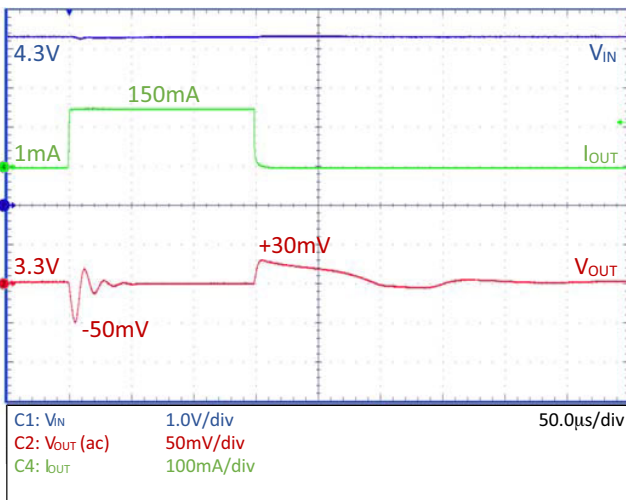


Figure 17. NCP730–3.3 V, $C_{OUT} = 22\text{ }\mu\text{F}$

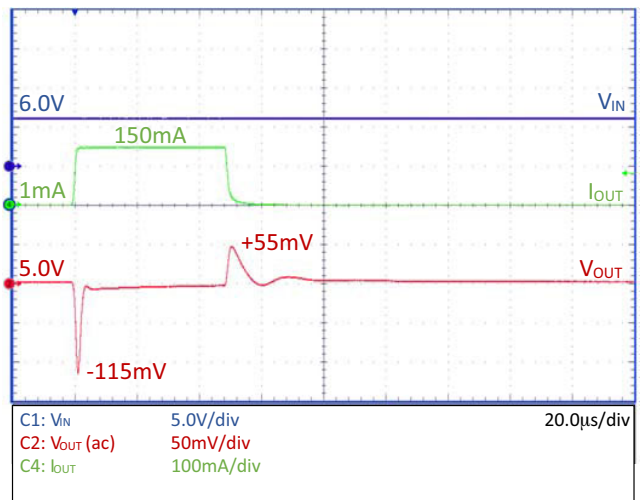


Figure 18. NCP730–5.0 V, $C_{OUT} = 1\text{ }\mu\text{F}$

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TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM} + 1\text{ V}$ and $V_{IN} \geq 2.7\text{ V}$, $V_{EN} = 1.2\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$, ADJ tied to OUT, $T_J = 25^\circ\text{C}$, unless otherwise specified

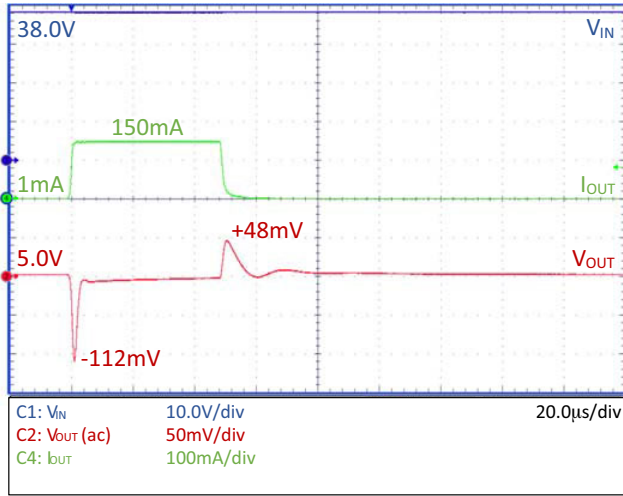


Figure 19. NCP730–5.0 V, $C_{OUT} = 1\text{ }\mu\text{F}$

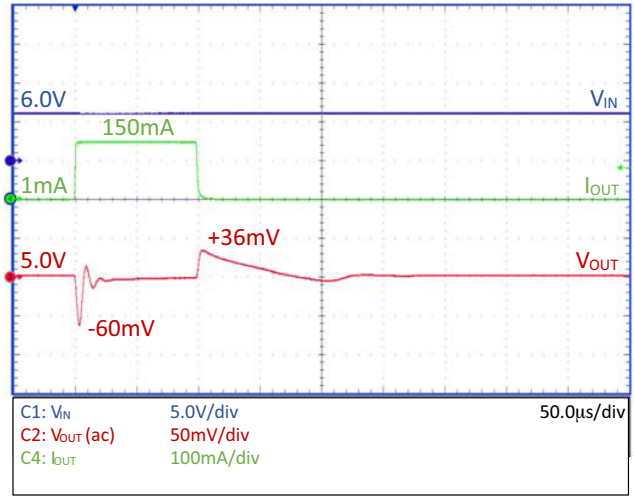


Figure 20. NCP730–5.0 V, $C_{OUT} = 10\text{ }\mu\text{F}$

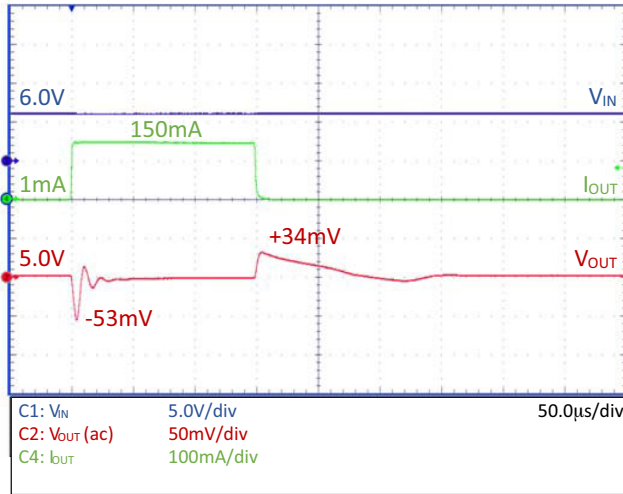


Figure 21. NCP730–5.0 V, $C_{OUT} = 22\text{ }\mu\text{F}$

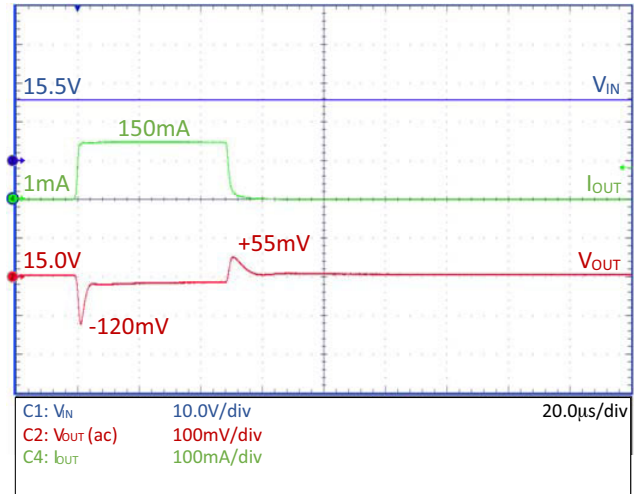


Figure 22. NCP730–15.0 V, $C_{OUT} = 1\text{ }\mu\text{F}$

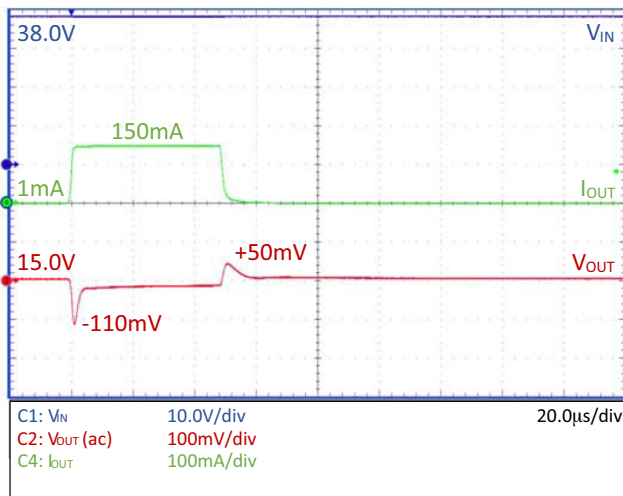


Figure 23. NCP730–15.0 V, $C_{OUT} = 1\text{ }\mu\text{F}$

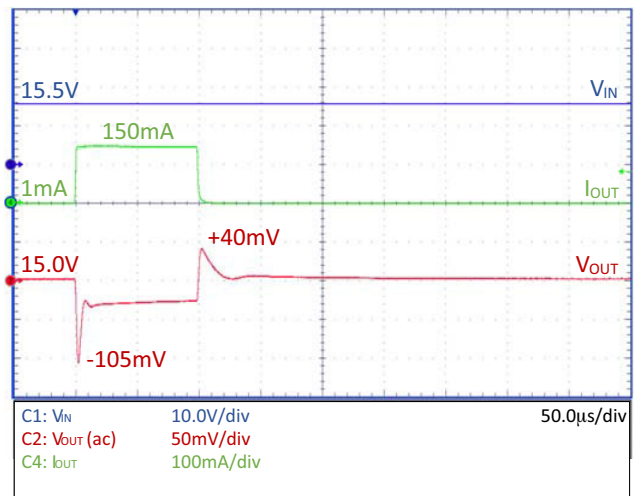


Figure 24. NCP730–15.0 V, $C_{OUT} = 10\text{ }\mu\text{F}$

NCP730

TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM} + 1\text{ V}$ and $V_{IN} \geq 2.7\text{ V}$, $V_{EN} = 1.2\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$, ADJ tied to OUT, $T_J = 25^\circ\text{C}$, unless otherwise specified

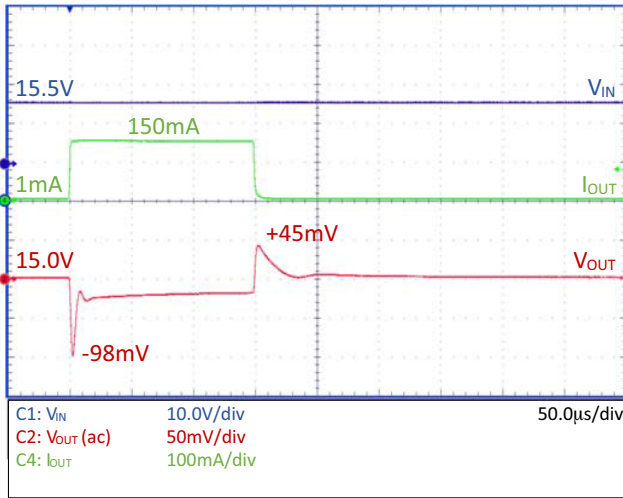


Figure 25. NCP730–15.0 V, $C_{OUT} = 22\text{ }\mu\text{F}$

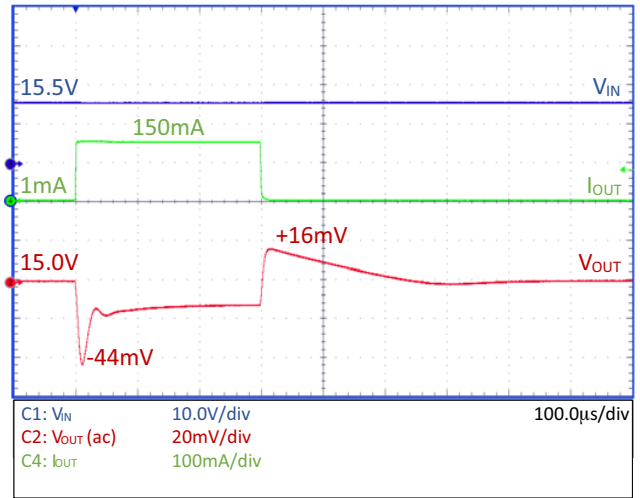


Figure 26. NCP730–15.0 V, $C_{OUT} = 50\text{ }\mu\text{F}$

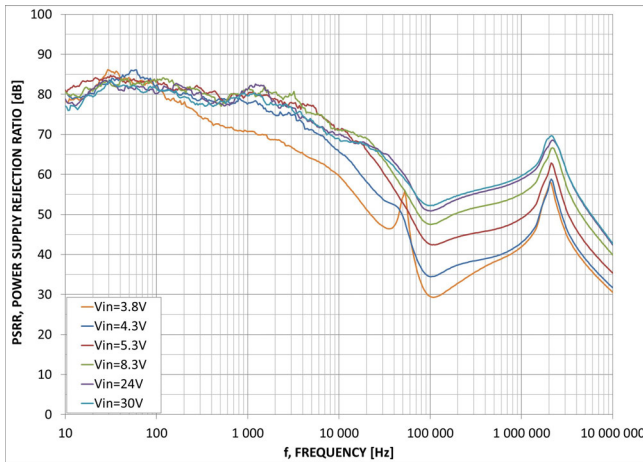


Figure 27. PSRR – NCP730–3.3 V, $C_{OUT} = 1\text{ }\mu\text{F}$, $I_{OUT} = 10\text{ mA}$

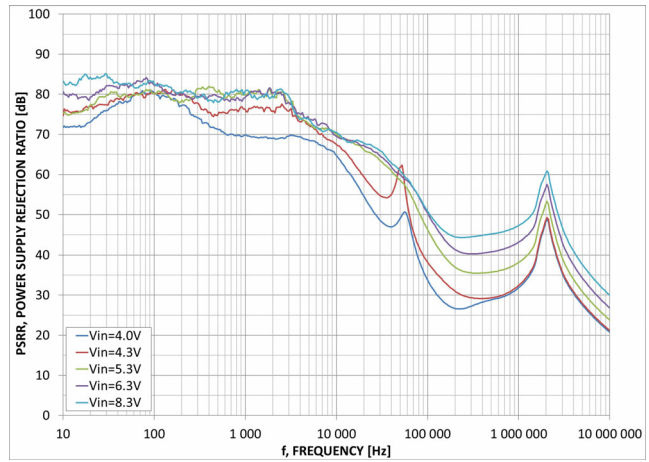


Figure 28. PSRR – NCP730–3.3 V, $C_{OUT} = 1\text{ }\mu\text{F}$, $I_{OUT} = 100\text{ mA}$

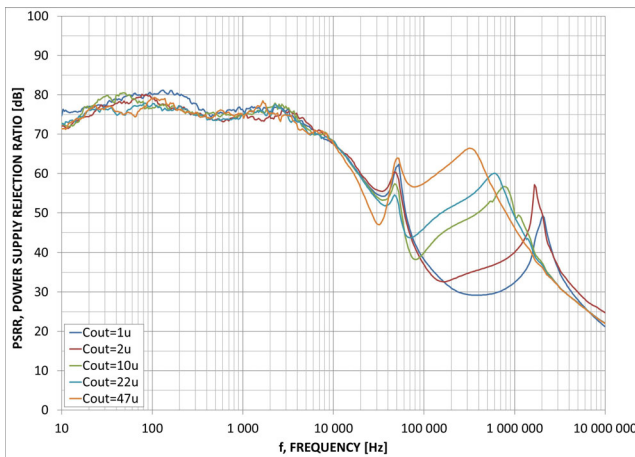


Figure 29. PSRR – NCP730–3.3 V, $V_{IN} = 4.3\text{ V}$, $I_{OUT} = 100\text{ mA}$

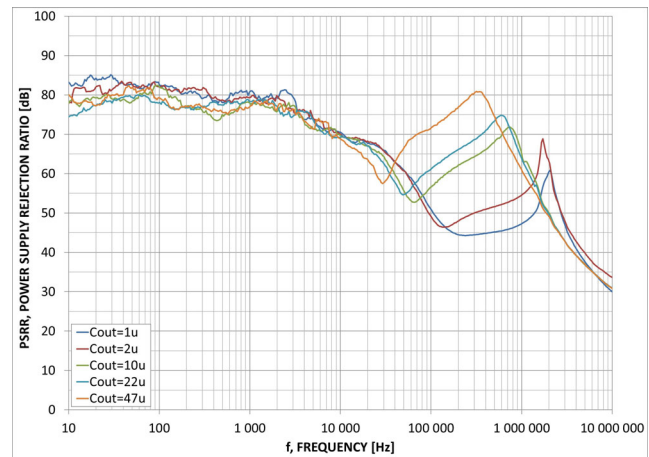


Figure 30. PSRR – NCP730–3.3 V, $V_{IN} = 8.3\text{ V}$, $I_{OUT} = 100\text{ mA}$

APPLICATIONS INFORMATION

Input Capacitor Selection (C_{IN})

Input capacitor connected as close as possible is necessary to ensure device stability. The X7R or X5R capacitor should be used for reliable performance over temperature range. The value of the input capacitor should be 1 μF or greater (max. value is not limited). This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto the input voltage. There is no requirement for the ESR of the input capacitor but it is recommended to use ceramic capacitor for its low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during load current changes. When a large load transients (like 1 mA to 150 mA) happens in the application the input power source of the LDO needs to provide enough power and the input voltage must not go below the level defined by this equation: $V_{IN} = V_{OUT-NOM} + V_{DO}$ otherwise the output voltage drop will be significantly higher (because LDO will enter the dropout state). In some cases when power supply powering the LDO has a poor load transient response or when there is a long connection between LDO and its power source then capacitance of input capacitor needs to be high enough to cover the LDO’s input voltage drop caused by load transient and maintains its value above the $V_{IN} = V_{OUT-NOM} + V_{DO}$ level (then C_{IN} could be in range of hundreds of μF).

Output Capacitor Selection (C_{OUT})

The LDO requires the output capacitor connected as close as possible to the output and ground pins. The LDO is designed to remain stable with output capacitor’s effective capacitance in range from 1 μF to 100 μF and ESR from 1 mΩ to 200 mΩ. The ceramic X7R or X5R type is recommended due to its low capacitance variations over the specified temperature range and low ESR. When selecting the output capacitor the changes with temperature and DC bias voltage needs to be taken into account. Especially for small package size capacitors such as 0402 or smaller the effective capacitance drops rapidly with the applied DC bias voltage (refer the capacitor’s datasheet for details). Larger capacitance and lower ESR improves the load transient response and PSRR.

Output Voltage

NCP730 is available in two version from output voltage point of view. One is fixed output voltage version (FIX version) and the other one is adjustable output voltage version (ADJ version).

The ADJ version has ADJ pin, which could be connected to the OUT pin directly, just to compensate voltage drop across the internal bond wiring and PCB traces or could be

connected to the middle point of the output voltage resistor divider for adjustment. When it is connected to the OUT pin the output voltage of the circuit is simply the same as the nominal output voltage of the LDO. When connected to the resistor divider the output voltage could be computed as the ADJ reference voltage (1.2 V) multiplied by the resistors divider ratio, see following equation.

$$V_{OUT} = V_{ADJ} \cdot \left(1 + \frac{R_1}{R_2}\right) + I_{ADJ} \cdot R_1 \quad (\text{eq. 1})$$

Where:

V_{OUT} is output voltage of the circuit with resistor divider.

V_{ADJ} is the LDO’s ADJ reference voltage.

I_{ADJ} is the LDO’s ADJ pin input current.

R₁ and R₂ are resistors of output resistor divider.

At the classical “old style” regulators like LM317 etc. the resistors where small (100 Ω – 10 kΩ) to make regulator stable at light loads (divider was also a pre-load function). On NCP730, which is very low quiescent current LDO regulator (1 μA), we need to care about current consumption of surrounding circuitry so we need to set the current through resistor divider flowing from V_{OUT} through R₁ and R₂ to GND, as low as possible.

On the other hand, the parasitic leakage current flowing into ADJ pin (I_{ADJ}) causes V_{OUT} voltage error (given by I_{ADJ} · R₁). The I_{ADJ} is temperature dependent so it is changing and we cannot compensate it in application, we just can minimize the influence by setting of R₁ value low, what is in opposite to maximizing its value because of current consumption.

So when selecting the R₁ and R₂ values we need to find a compromise between desired V_{OUT} error (temperature dependent) and total circuit quiescent current.

If we want to simplify this task, we can say the I_{R2} should be 100–times higher than I_{ADJ} at expected T_J temperature range. If we chose the ratio “I_{R2} to I_{ADJ}” higher (for example more than 100 as stated before), the ΔV_{OUT} error caused by I_{ADJ} change over temperature would be lower and opposite, if the ratio “I_{R2} to I_{ADJ}” is smaller, the error would be bigger.

In limited T_J temperature range –40°C to +85°C the I_{ADJ} is about 10–times smaller than in the full temperature range –40°C to +125°C (see typical characteristics graph of I_{ADJ} over temperatures), so we can use bigger R₁, R₂ values, as could be seen at next examples.

Example 1:

Desired V_{OUT} voltage is 5.0 V. Computed maximal T_J in application (based on max. power dissipation and cooling) is 85°C. Than I_{ADJ} at 85°C is about: I_{ADJ85} = 10 nA.

NCP730

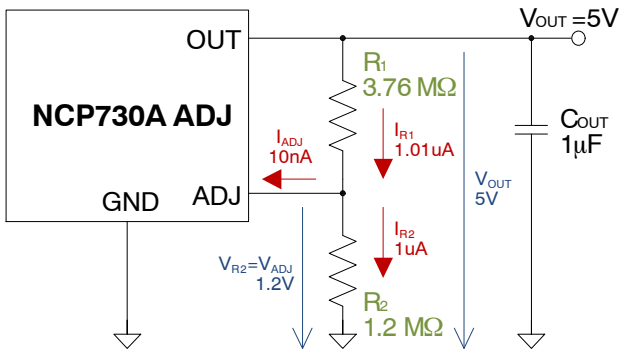


Figure 31. ADJ Output Voltage Schematic – Example 1

We chose:

$$I_{R2} = 100 \cdot I_{ADJ85} = 100 \cdot 10E-9 = 1 \mu A$$

Then:

$$R_2 = \frac{V_{R2}}{I_{R2}} = \frac{1.2}{1E-6} = 1.2 \text{ M}\Omega$$

$$R_1 = \frac{V_{R1}}{I_{R1}} = \frac{V_{OUT} - V_{R2}}{I_{ADJ85} + I_{R2}} = \frac{5 - 1.2}{10E-9 + 1E-6} = \frac{3.8}{1.01E-6} = 3.762 \text{ M}\Omega$$

Verification:

For low temperature ($T_J = 25^\circ\text{C}$) the $I_{ADJ25} = 1 \text{ nA}$:

$$V_{OUT} = V_{ADJ} \cdot \left(1 + \frac{R_1}{R_2}\right) + I_{ADJ} \cdot R_1$$

$$V_{OUT} = 1.2 \cdot \left(1 + \frac{3.762E6}{1.2E6}\right) + 1E-9 \cdot 3.762E6 = 4.966 \text{ V}$$

For maximal temperature ($T_J = 85^\circ\text{C}$) the $I_{ADJ85} = 10 \text{ nA}$:

$$V_{OUT} = 1.2 \cdot \left(1 + \frac{3.762E6}{1.2E6}\right) + 10E-9 \cdot 3.762E6 = 5.000 \text{ V}$$

Output voltage error for temperatures 85°C to 25°C is:

$$\Delta V_{OUT} = \frac{V_{OUT85} - V_{OUT25}}{V_{OUT85}} \cdot 100 = \frac{5.000 - 4.966}{5.000} \cdot 100 = 0.68\%$$

Total circuit quiescent current at $T_J = 25^\circ\text{C}$ is:

$$I_{Q(TOT)} = I_{Q(LDO)} + I_{R1} = 1.3E-6 + 1.01E-6 = 2.31 \mu A$$

We can see that current consumption of external resistor divider is almost the same as quiescent current of LDO.

Example 2:

Desired V_{OUT} voltage is 5.0 V. Computed maximal T_J in application (based on max. power dissipation and cooling) is in this case higher, 125°C , to show the difference. Than maximal I_{ADJ} at 125°C is $I_{ADJ125} = 100 \text{ nA}$ (based on Electrical characteristics table).

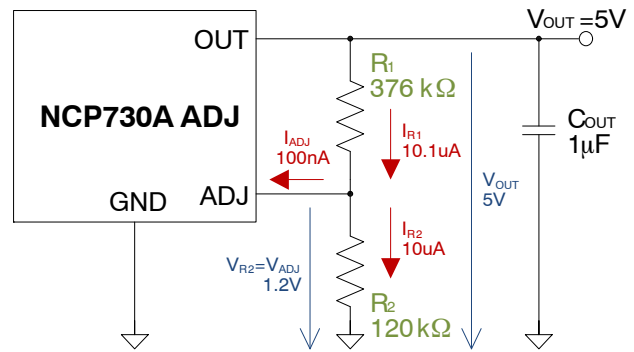


Figure 32. ADJ Output Voltage Schematic – Example 2

We chose:

$$I_{R2} = 100 \cdot I_{ADJ125} = 100 \cdot 100E-9 = 10 \mu A$$

Then:

$$R_2 = \frac{V_{R2}}{I_{R2}} = \frac{1.2}{10E-6} = 120 \text{ k}\Omega$$

$$R_1 = \frac{V_{R1}}{I_{R1}} = \frac{V_{OUT} - V_{R2}}{I_{ADJ125} + I_{R2}} = \frac{5 - 1.2}{100E-9 + 10E-6} = \frac{3.8}{10.1E-6} = 376.2 \text{ k}\Omega$$

Verification:

For low temperature ($T_J = 25^\circ\text{C}$) the $I_{ADJ25} = 1 \text{ nA}$:

$$V_{OUT} = V_{ADJ} \cdot \left(1 + \frac{R_{ADJ1}}{R_{ADJ2}}\right) + I_{ADJ} \cdot R_{ADJ1}$$

$$V_{OUT} = 1.2 \cdot \left(1 + \frac{376.2E3}{120E3}\right) + 1E-9 \cdot 376.2E3 = 4.962 \text{ V}$$

For maximal temperature ($T_J = 125^\circ\text{C}$) the $I_{ADJ125} = 100 \text{ nA}$:

$$V_{OUT} = 1.2 \cdot \left(1 + \frac{376.2E3}{120E3}\right) + 100E-9 \cdot 376.2E3 = 5.000 \text{ V}$$

Output voltage error for temperatures 125°C to 25°C is:

$$\Delta V_{OUT} = \frac{V_{OUT125} - V_{OUT25}}{V_{OUT125}} \cdot 100 = \frac{5.000 - 4.962}{5.000} \cdot 100 = 0.76\%$$

Total circuit quiescent current at $T_J = 25^\circ\text{C}$ is:

$$I_{Q(TOT)} = I_{Q(LDO)} + I_{R1} = 1.3E-6 + 10.1E-6 = 11.4 \mu A!!!$$

We can see that error of V_{OUT} voltage is almost the same as in example 1 (because we have used the same “ I_{R2} to I_{ADJ} ” ratio = 100x) but the application quiescent current is almost 10–times higher (because of 10–times higher divider current).

C_{FF} Capacitor

Even the NCP730 is very low quiescent current device, both the load transients over/under shoots and settling times are excellent. See the Typical characteristics graphs.

At adjustable application, the external resistor divider with input ADJ pin capacity and ADJ pin PCB trace capacity to GND makes a low pass filter what negatively affects the dynamic behavior of the LDO. On the next picture is shown how this unwanted side effect could be compensated by adding of feed-forward capacitor C_{FF} across R_1 resistor.

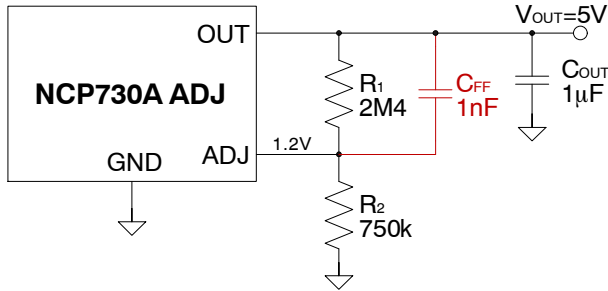


Figure 33. ADJ Output Voltage Schematic – C_{FF} Capacitor

The value of the C_{FF} depends on R_1 and R_2 resistor values. When R_1 , R_2 values are in hundreds of kilohms, proposed C_{FF} value is 1 nF, as shown on picture above, for the best dynamic performance. Generally, the value could be in range from 0 to 10 nF.

On next three pictures is shown the C_{FF} capacitor influence to dynamic parameters.

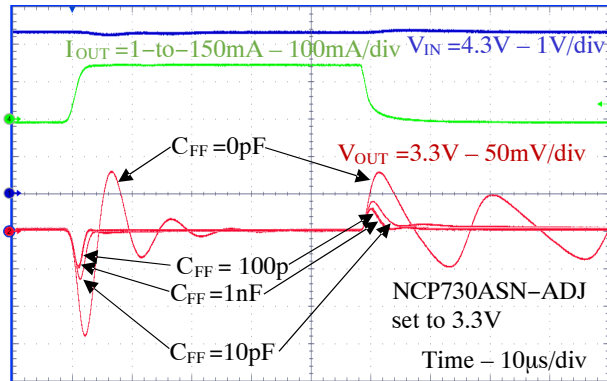


Figure 34. Load Transient – Different C_{FF}

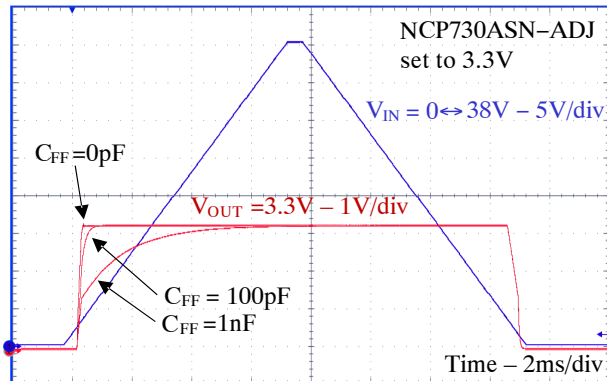


Figure 35. Startup Timing – Different C_{FF}

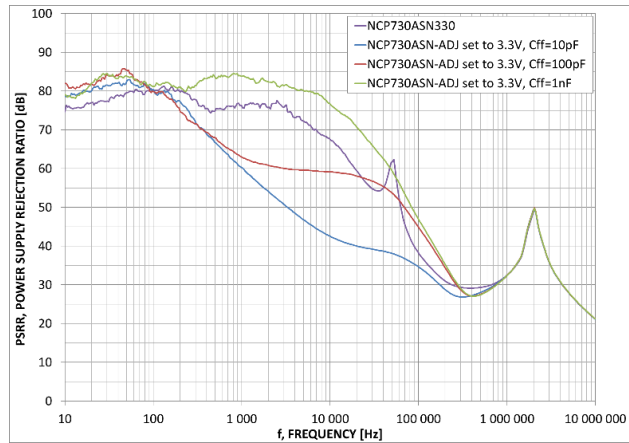


Figure 36. PSRR – Different C_{FF}

Startup

In the NCP730 device there are two main internal signals which triggers the startup process, the under-voltage lockout (UVLO) signal and enable signal. The first one comes from UVLO comparator, which monitors if the IN pin voltages is high enough, while the second one comes from EN pin comparator. Both comparators have embedded hysteresis to be insensitive to input noise.

Not only the comparator but also the pull-up current source is connected to EN pin. Current source is sourcing $I_{EN-PU} = 300$ nA current flowing out of the chip what ensures the level on the pin is high enough when it is left floating. The comparator compares the EN pin voltage with internal reference level 0.9 V (typ.). Hysteresis is 100 mV (typ.).

The UVLO comparator threshold voltage is 1.95 V (typ.) and hysteresis is 200 mV (typ.).

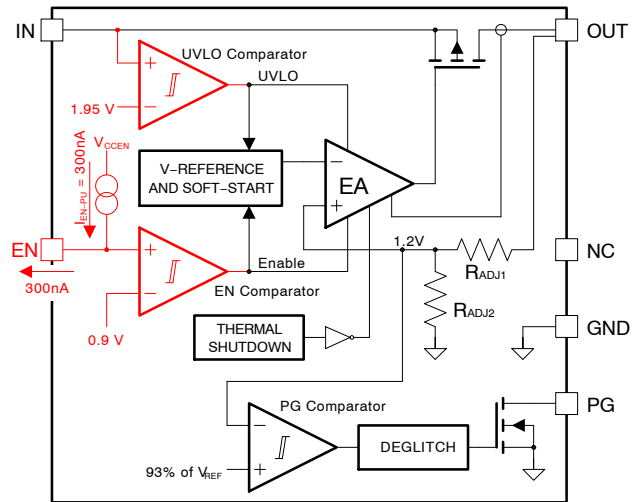


Figure 37. Internal Block Diagram – EN Pin

Startup by IN Pin Voltage

When the LDO is started by IN pin voltage rise, it is turned ON when the voltage is higher than UVLO threshold level. This is the case of both following application circuits, the first one with EN pin floating and the second one with EN pin connected to IN pin.

When the EN pin is floating (left unconnected) its voltage, after the LDO is powered, rises to V_{CCEN} level (2.5 V – 4.5 V, V_{IN} dependent) as the internal current source pulls the pin voltage up. V_{CCEN} voltage level on EN pin is higher than EN comparator threshold so the LDO is turned ON.

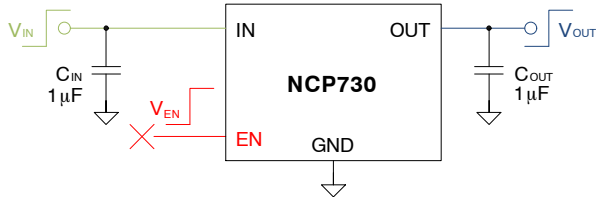


Figure 38. Circuit – Floating EN Pin

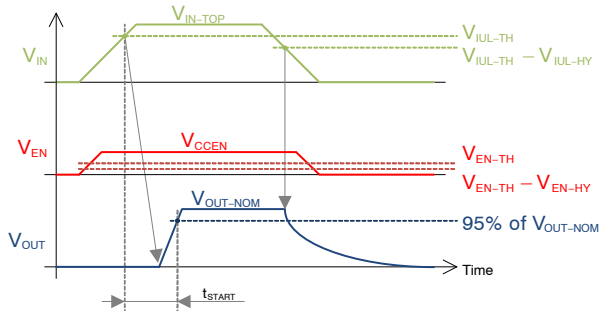


Figure 39. Startup Timing – Floating EN Pin

It is also possible to connect EN pin directly to IN pin in the whole input voltage range. The startup sequence is very similar to previous case, the only difference is that the EN pin voltage is not clamped to V_{CCEN} level but it is the same as V_{IN} voltage.

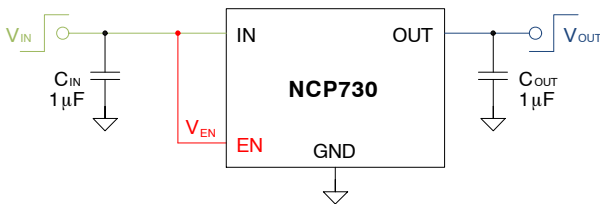


Figure 40. Circuit – EN Pin Connected to IN Pin

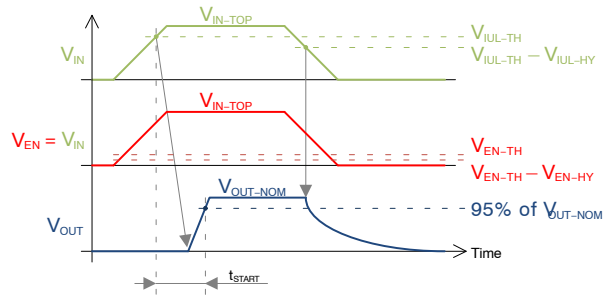


Figure 41. Startup Timing – EN Pin Connected to IN Pin

Startup time in both cases above is measured from the point where IN pin voltage reaches V_{IUL-TH} value to point when OUT pin voltage reaches 95% of its nominal value.

The reason why the LDO is started by the UVLO signal and not by the enable signal is the fact that the UVLO signal turns to valid state later then the enable. (EN pin voltage reaches the V_{EN-TH} level prior the IN pin voltage reaches the V_{IUL-TH} level).

Startup by EN Pin Voltage

When V_{IN} voltage in the application is settled above the V_{IUL-TH} level and control voltage to the EN pin is applied, the level higher than V_{EN-TH} enables the LDO and the level lower than ($V_{EN-TH} - V_{EN-HY}$) disables it.

Startup time is measured from point where V_{EN} voltage reaches V_{EN-TH} value to point when V_{OUT} voltage reaches 95% of its nominal value.

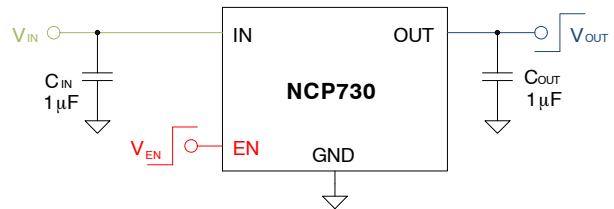


Figure 42. Circuit – LDO Controlled by V_{EN}

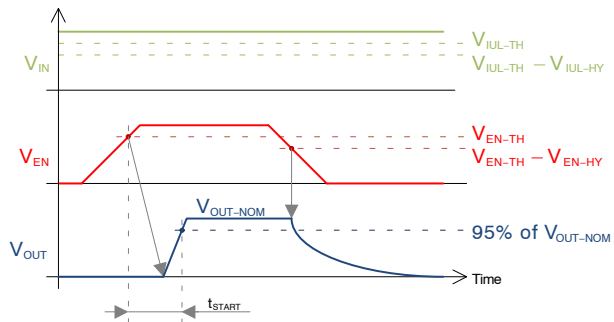


Figure 43. Timing – V_{EN} -Startup

Startup by IN Pin Voltage – Delayed

The startup time triggered by IN pin voltage rise could be delayed by adding of EN pin capacitor (C_{EN}). The startup sequence is following – after the V_{IN} voltage is applied, the charging of C_{EN} capacitor by internal pull-up current (I_{EN-PU}) is started. When the C_{EN} capacitor voltage (V_{CEN}) reaches EN comparator’s threshold voltage (V_{EN-TH}) the LDO is enabled. Charging of C_{EN} continues up to the V_{CCEN} level (2.5 V – 4.5 V, V_{IN} dependent) with no following effect. The steepness of the LDO’s output voltage rise (soft-start time) is not affected by using of C_{EN} capacitor. The additional delay time ($t_{CEN-DELAY}$) could be computed by:

$$t_{CEN-DELAY} = C_{EN} \cdot \frac{V_{EN-TH}}{I_{EN-PU}} = C_{EN} \cdot \frac{0.9 \text{ V}}{300 \text{ nA}} \quad (\text{eq. 2})$$

The total startup time ($t_{START-CEN}$) with connected C_{EN} capacitor is a sum of normal startup time (t_{START}) and additional delay time caused by C_{EN} capacitor ($t_{CEN-DELAY}$):

$$t_{START-CEN} = t_{START} + t_{CEN-DELAY} \quad (\text{eq. 3})$$

Value of the C_{EN} capacitor could be in range from 0 to several microfarads. Capacitor’s leakage current must be negligible to internal pull-up current I_{EN-PU} , otherwise the charging will be affected and adding of R_{EN} resistor from IN to EN pin will be needed.

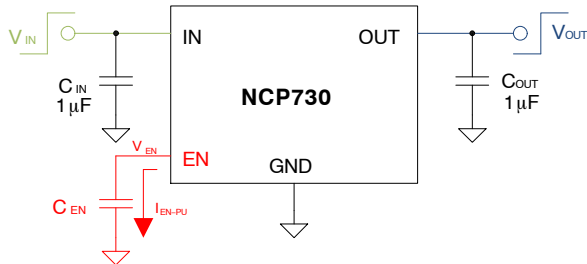


Figure 44. Circuit – C_{EN} -Delayed V_{IN} -Startup

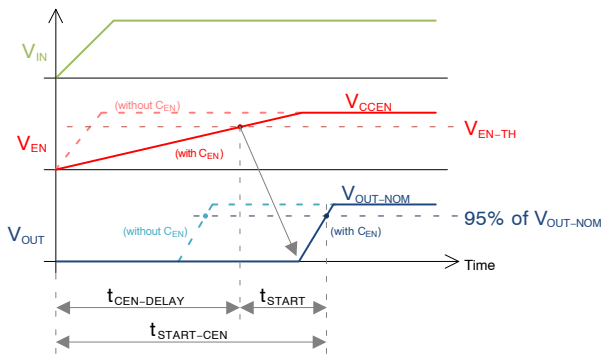


Figure 45. Timing – C_{EN} -Delayed V_{IN} -Startup

Startup by Transistor at EN Pin

If the LDO needs to be controlled by transistor or generally by open collector / open drain circuit as shown at the next picture, the control behavior is inverted. High control signal makes the EN pin voltage low and low control

signal makes it high because the transistor is connected as signal inverter.

In this application we need to care about transistor’s leakage current which must be negligible compared to the internal pull-up current $I_{EN-PU} = 300 \text{ nA}$ otherwise additional pull-up resistor R_{EN} will be needed. The maximum value of the EN resistor R_{EN-MAX} is computed from maximal external transistor leakage current (over desired temperature range) $I_{T-LK-MAX}$ and minimal input voltage V_{IN-MIN} :

$$R_{EN-MAX} = \frac{V_{IN-MIN}}{I_{T-LK-MAX}} \quad (\text{eq. 4})$$

For safe, select the EN resistor value R_{EN} lower enough to computed R_{EN-MAX} .

When R_{EN} is used the overall application shutdown current is increased because the current through R_{EN} resistor (I_{REN}) is added to input shutdown current of the LDO ($I_{SD(LDO)}$). The total application shutdown current ($I_{SD(TOT)}$) is:

$$I_{SD(TOT)} = I_{SD(LDO)} + I_{REN} \quad (\text{eq. 5})$$

$$I_{REN} = \frac{(V_{IN} - V_{T-DS})}{R_{EN}}$$

Where V_{T-DS} is the drain to source voltage of the transistor (given by R_{DSON} and I_{REN}).

The overall application quiescent current when R_{EN} is used is influenced only by the transistor’s leakage current I_{T-LK} .

$$I_{Q(TOT)} = I_{Q(LDO)} + I_{T-LK} \quad (\text{eq. 6})$$

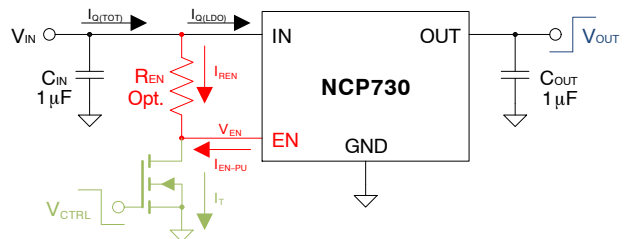


Figure 46. Circuit – EN Pin Controlled by Transistor

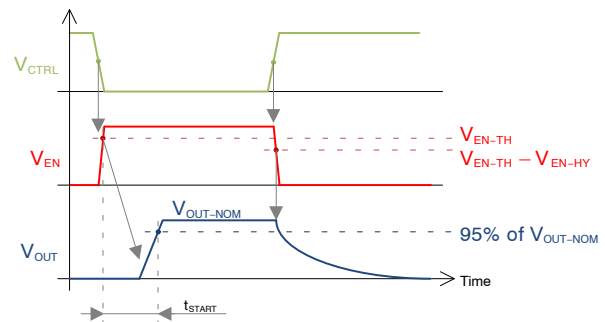


Figure 47. Startup Timing – EN Pin Controlled by Transistor

Startup by Transistor at EN Pin – Delayed

The startup time triggered by EN pin voltage rise, could be delayed the same way as IN pin triggered startup, by adding of C_{EN} capacitor. The startup sequence is following – when the external NMOS control voltage (V_{CTRL}) is high the C_{EN} capacitor connected to the EN pin is shorted to GND and LDO is disabled. After the V_{CTRL} is turned low the charging of C_{EN} capacitor by the internal pull-up current source (I_{EN-PU}) starts. When the C_{EN} capacitor voltage (V_{CEN}, which is the V_{EN} in fact) reaches EN comparator’s threshold voltage (V_{EN-TH}) the LDO is enabled. Charging of C_{EN} then continues up to the V_{CCEN} level (2.5 V – 4.5 V, V_{IN} dependent) with no following effect. The steepness of the LDO’s output voltage rise (soft-start time) is not affected by using of C_{EN} capacitor. The additional delay time (t_{CEN-DELAY}) could be computed by eq. 2 and the total delayed startup time with C_{EN} capacitor (t_{START-CEN}) by eq. 3. What has been said about the C_{EN} capacitor selection at previous paragraphs is applicable here as well.

Also in this application we need to care about transistor’s leakage current which must be negligible compared to the internal pull-up current I_{EN-PU} = 300 nA otherwise additional pull-up resistor R_{EN} will be needed. Same rules and computations as stated in previous paragraph about R_{EN} are applicable here. Note that R_{EN} would influence the speed of C_{EN} capacitor charging.

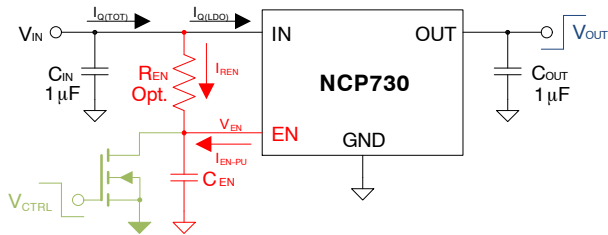


Figure 48. Circuit – EN Pin with C_{EN} Controlled by Transistor

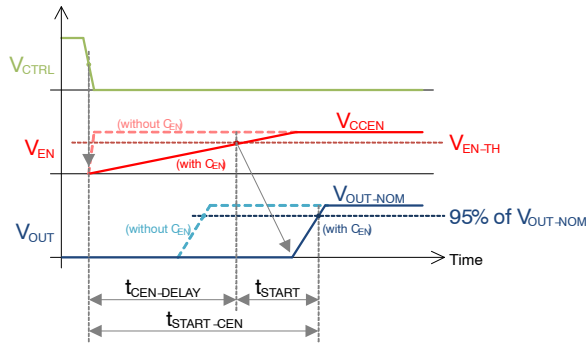


Figure 49. Startup Timing – EN Pin with C_{EN} Controlled by Transistor

Enable Input as Inaccurate IN Pin UVLO

The EN input pin on NCP730 device is specified by threshold voltage and hysteresis both with minimum and maximum value, what allows using EN comparator as adjustable input voltage UVLO function. To set the V_{IN}

UVLO threshold value, the external resistor divider from IN pin to EN pin, is needed.

Note that the specification of EN pin threshold voltage (0.7 V to 1.05 V over full operating temperature range) is not as precise as threshold voltage on dedicated UVLO devices. The reason is the EN circuit has to have ultra-low current consumption (NCP730 I_{SHDN} is 350 nA typ. even while I_{EN-PU} is 300 nA typ. so EN comparator is powered by less than 50 nA typ.). We need to count with that when thinking about the IN pin UVLO design. Below is the application example to show what precision we can get.

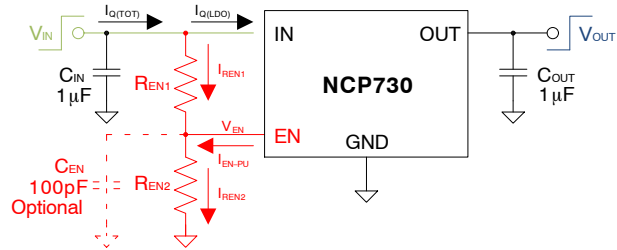


Figure 50. Circuit – IN Voltage UVLO by EN Pin

The two main equations for IN pin threshold computation are:

$$R_{EN1} = \frac{V_{IN-UVLO-TH} - V_{EN-TH}}{I_{REN1}} \quad (\text{eq. 7})$$

$$R_{EN2} = \frac{V_{EN-TH}}{I_{REN1} + I_{EN-PU}}$$

From that, we can get:

$$V_{IN-UVLO-TH} = V_{EN-TH} \cdot \left(1 + \frac{R_{EN1}}{R_{EN2}} \right) - R_{EN1} \cdot I_{EN-PU} \quad (\text{eq. 8})$$

We can see that IN pin UVLO threshold is EN pin threshold multiplied by the resistor divider ratio as expected but it is unwillingly affected by I_{EN-PU} pull-up current. As the I_{EN-PU} current could vary up to the 1 µA max., we need to choose the I_{REN1} current several times higher to make the I_{EN-PU} influence negligible. The good practice could be to choose I_{REN1} at least 10-times higher than I_{EN-PU} (the bigger the better for the accuracy).

An optional component in this application is C_{EN} capacitor. Its main function is filtering out the spurious signals coming from IN power supply and the minor function is to delay the startup as described in section before. The value of C_{EN} for filtering purpose could be in range from 10 pF to 10 nF. The time constant of this filter is given by:

$$t_{FILTER} = C_{EN} \cdot \frac{R_{EN1} \cdot R_{EN2}}{R_{EN1} + R_{EN2}} \quad (\text{eq. 9})$$

The side effect of the UVLO divider is increased overall power consumption. At no load state, the quiescent current I_{Q(TOT)} of the application is:

$$I_{Q(TOT)} = I_{Q(LDO)} + I_{REN1} \quad (\text{eq. 10})$$

So if we select the I_{REN1} value at least 10-times higher than I_{EN-PU-MAX} (1 µA), then the UVLO divider current is

almost 10-times higher than typical LDO's quiescent current (1.3 μ A).

IN voltage UVLO application example:

Desired V_{OUT} voltage is 5 V, the LDO's input voltage in normal state is 12 V. We want to turn-off the LDO's output voltage when input voltage is below 10 V (max.).

First, choose the I_{REN1} current as 10-times the maximum I_{EN-PU} current:

$$I_{REN1} = 10 \cdot I_{EN-PU} = 10 \cdot 1 \mu A = 10 \mu A \quad (\text{eq. 11})$$

Then, to obtain R_{EN1} and R_{EN2} values for maximal $V_{IN-UVLO-TH} = 10$ V, we need to put maximum value of V_{EN-TH} (1.05 V) and minimum value of I_{EN-PU} (0 μ A) into the equations for R_{EN1} and R_{EN2} :

$$R_{EN1} = \frac{V_{IN-UVLO-TH} - V_{EN-TH}}{I_{REN1}} = \frac{10 \text{ V} - 1.05 \text{ V}}{10 \mu A} = 895 \text{ k}\Omega \quad (\text{eq. 12})$$

$$R_{EN2} = \frac{V_{EN-TH}}{I_{REN1} + I_{EN-PU}} = \frac{1.05}{10 \mu A + 0 \mu A} = 105 \text{ k}\Omega$$

The resulting $V_{IN-UVLO-TH}$ limits will be:

$$V_{IN-UVLO-TH-MIN} = V_{EN-TH-MIN} \cdot \left(1 + \frac{R_{EN1}}{R_{EN2}}\right) - R_{EN1} \cdot I_{EN-PU-MAX} \quad (\text{eq. 13})$$

$$V_{IN-UVLO-TH-MIN} = 0.7 \cdot \left(1 + \frac{895 \text{ k}\Omega}{105 \text{ k}\Omega}\right) - 895 \text{ k}\Omega \cdot 1 \mu A$$

$$V_{IN-UVLO-TH-MIN} = 5.77 \text{ V}$$

$$V_{IN-UVLO-TH-MAX} = V_{EN-TH-MAX} \cdot \left(1 + \frac{R_{EN1}}{R_{EN2}}\right) - R_{EN1} \cdot I_{EN-PU-MIN}$$

$$V_{IN-UVLO-TH-MAX} = 1.05 \cdot \left(1 + \frac{895 \text{ k}\Omega}{105 \text{ k}\Omega}\right) - 895 \text{ k}\Omega \cdot 0 \mu A$$

$$V_{IN-UVLO-TH-MAX} = 10.0 \text{ V}$$

$$I_{Q(TOT)} = I_{Q(LDO)} + I_{REN1} = 1.3 \mu A + 10 \mu A = 11.3 \mu A$$

When higher I_{REN1} is selected the $V_{IN-UVLO-TH-MIN}$ would be slightly near the target value, the $V_{IN-UVLO-TH-MAX}$ would stay the same but the $I_{Q(TOT)}$ would be significantly higher:

$$I_{REN1} = 100 \cdot I_{EN-PU} = 100 \cdot 1 \mu A = 100 \mu A \quad (\text{eq. 14})$$

We would get:

$$R_{EN1} = 89.5 \text{ k}\Omega \quad (\text{eq. 15})$$

$$R_{EN2} = 10.5 \text{ k}\Omega$$

$$V_{IN-UVLO-TH-MIN} = 6.58 \text{ V}$$

$$I_{Q(TOT)} = I_{Q(LDO)} + I_{REN1} = 1.3 \mu A + 100 \mu A = 101.3 \mu A$$

We can see the IN pin UVLO threshold precision computed above (5.77 V or 6.58 V min. / 10.0 V max.) is not too high because the EN pin threshold and EN pin internal pull-up current specifications are not so tight as on dedicated UVLO devices but at some applications this precision could fit the needs.

Output Current Limit

Output current is internally limited to 280 mA typ. The LDO will source this current when the output voltage drops down from the nominal output voltage (test condition is 90% of $V_{OUT-NOM}$). If the output voltage is shorted to ground, the device continues with current limitation at the same current level. The current limit and short circuit protection will work properly over the whole temperature and input voltage ranges. There is no limitation for the short circuit duration.

Minimal output current limit value is 200 mA what could be used to cover current demand peaks, higher than the LDO's nominal output current (150 mA)..

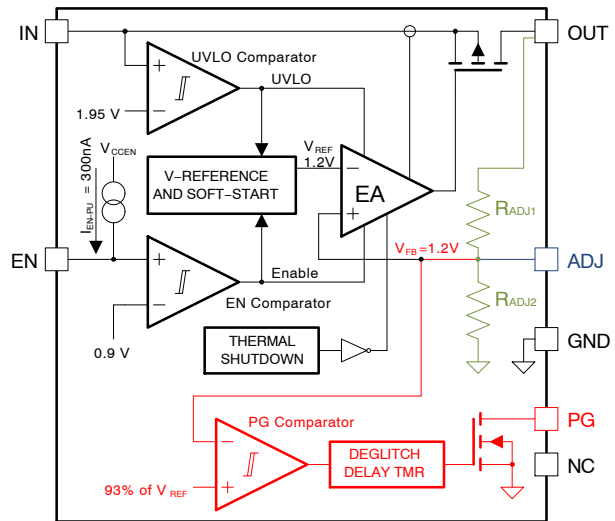
Power Supply Rejection Ratio

The LDO features high power supply rejection ratio even it is very low quiescent current device. See the Typical characteristics section for the graphs over different conditions.

The PSRR at higher frequencies (from about 100 kHz) can be tuned by the selection of C_{OUT} capacitor, applied input voltage and proper PCB layout (minimizing impedance from load to C_{OUT}).

PG Output

Version B of the NCP730 device contains PG circuit for the V_{OUT} voltage level monitoring. Internally it is combined from PG comparator, deglitch/delay timer and output NMOS transistor (highlighted by red color at picture below). At both, ADJ and FIX versions, the PG comparator compares internal feedback signal voltage (V_{FB}) with the 93% of V_{REF} (typ.) what makes the function independent to the output voltage absolute value (it always compares set V_{OUT} with 93% of its nominal value).



Note: Blue objects are valid for ADJ version
Green objects are valid for FIX version

Figure 51. Power Good Output Block Diagram

The PG output is in high impedance state (Hi-Z) to show “power ok state” when the V_{OUT} voltage is above the PG threshold level (V_{PG-TH}) or is shorted to GND pin to show “power fail state” when the V_{OUT} falls below the low level ($V_{PG-TH} - V_{PG-HY}$).

The PG threshold voltage is 93% of $V_{OUT-NOM}$ (typ.) and the hysteresis is 2% of $V_{OUT-NOM}$ (typ.).

Because the PG output is open drain type it needs to be connected by external pull resistor to a voltage level, which defines the PG pin voltage at time when it is in Hi-Z state. It allows connections of PG pin to circuit with the same or different power supply voltage to the LDO’s V_{OUT} level. Below are the connections examples.

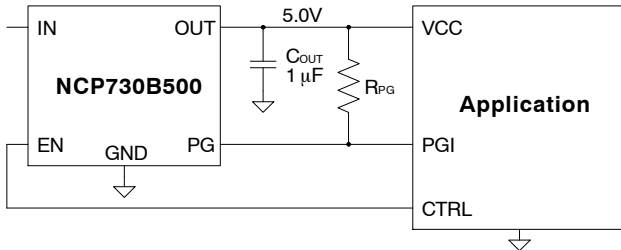


Figure 52. Circuit Example – PG Connected to LDO’s Output

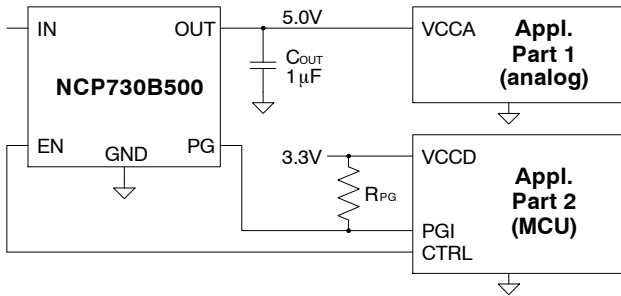


Figure 53. Circuit Example – PG Connected to Application Power Supply

Following timing diagrams show the situation when LDO falls out of regulation 3 times (output voltage drops down from nominal value) because of (for example) insufficient IN pin voltage.

Note that the V_{PG} voltage at “power ok state” follows the voltage where the R_{PG} is connected because the PG output is in Hi-Z state and just R_{PG} connection point defines the V_{PG} level. In the first example when R_{PG} is connected to LDO’s output, the V_{PG} follows the LDO’s V_{OUT} including the drops. In the second example the R_{PG} is connected to LDO independent power rail (3.3 V) so the V_{PG} is not following the LDO’s output voltage.

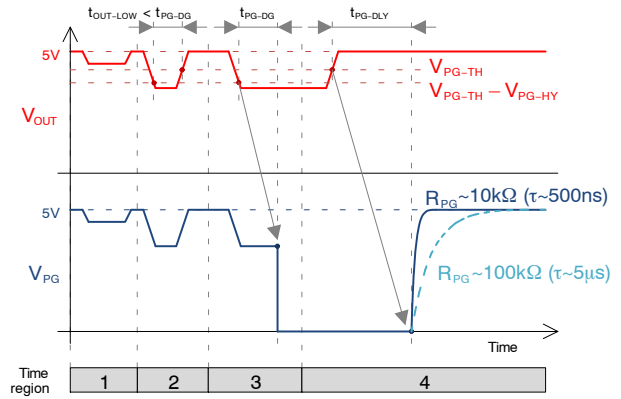


Figure 54. Timing – PG Connected to LDO’s Output

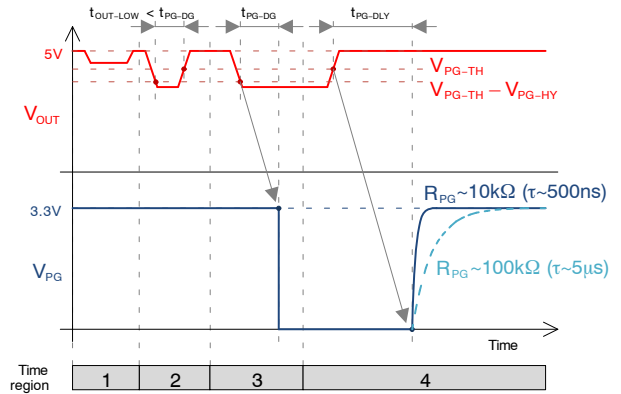


Figure 55. Timing – PG Connected to Application Power Supply 3.3 V

The timing diagrams have been divided into 4 time regions to show different situations:

In region-1, the V_{OUT} drop is not deep enough so the PG output shows “power ok state”.

In region-2, the V_{OUT} drop is deeper and crosses the V_{PG-TH} threshold level but the duration of the drop is shorter than PG deglitch time ($t_{PG-DG} = 160 \mu s$ typ.) so the PG output still shows “power ok state”. Note that the deglitch time has been intentionally implemented to filter out spurious output voltage drops (caused for example by fast load transients etc.).

In both two first regions the V_{PG} is high and follows the voltage level where the R_{PG} resistor is connected to ($V_{LDO(OUT)}$ or V_{CCD}).

In region-3, the V_{OUT} drop is deep enough and the duration is longer than t_{PG-DG} time so the PG output is shorted to GND pin and shows power fail state.

In region-4, the V_{OUT} returns back to its nominal value. When it crosses the level ($V_{PG-TH} - V_{PG-HY}$) the PG output turns from short to GND into Hi-Z state, not immediately, but after the PG delay time ($t_{PG-DLY} = 320 \mu s$ typ.). The PG delay ensures that low PG pulse, showing “power fail state”, is always longer than the t_{PG-DLY} time and then could be caught by the application circuit (for example by MCU).

R_{PG} Value Selection

As shown on the Figure 54 and Figure 55 in the time region-4, the steepness of PG signal return to high level depends on the R_{PG} pull-up resistance (with relation to capacitance of LDO's PG output, parasitic capacitance of PG signal PCB traces and the application circuit PGI input capacitance. The lower R_{PG} resistance the faster PG return to high level.

At the most applications, the PG return speed to high level is not a concern, mainly because of the fact that the LDO already delays the PG return by the t_{PG-DLY} time (320 μs typ.) intentionally so the returning speed itself is negligible.

The next view to the R_{PG} value is the power consumption at “power fail state” when the current from the supply flows through the R_{PG} to the grounded PG pin. This is just a case of the power fail state so probably not a concern too.

At the electrical characteristics table we can find the parameter “PG Output Low Level Voltage (V_{PG-OL})” which defines the drop across the PG internal transistor when it sinks current 1 mA. We can take this current condition (1 mA) as a maximal PG current (I_{PG-MAX}) for the R_{PG-MIN} computation (as we know the PG drop at this level, 0.4 V max.). If the application input current I_{PGI} is negligible to I_{RPG} we can compute the R_{PGI-MIN} by:

$$R_{PG-MIN} = \frac{V_{CC-RPG}}{I_{PG-MAX}} \quad (\text{eq. 16})$$

And, for example, when R_{PG} is connected to 3.3 V power rail:

$$R_{PG-MIN} = \frac{V_{CC-RPG}}{I_{PG-MAX}} = \frac{3.3 \text{ V}}{1 \text{ mA}} = 3.3 \text{ k}\Omega \quad (\text{eq. 17})$$

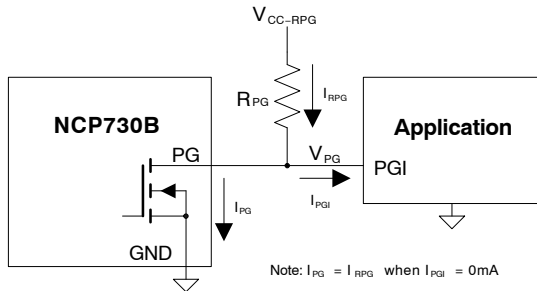


Figure 56. Circuit Example for R_{PG} Value Selection

From the opposite side, R_{PG} is limited to its maximum value, based on: maximum PG leakage current I_{PG-LK-MAX}, maximum threshold voltage of the application input V_{PGL-TH-MAX} and maximum application input leakage current I_{PGL-LK-MAX}. Then:

$$R_{PG-MAX} = \frac{V_{CC-RPG} - V_{PGL-TH-MAX}}{I_{PG-LK-MAX} + I_{PGL-LK-MAX}} \quad (\text{eq. 18})$$

For example, when R_{PG} is connected to 3.3 V power rail, max. threshold voltage of the application input is 1.3 V and application input leakage current is 3 μA max.:

$$R_{PG-MAX} = \frac{V_{CC-RPG} - V_{PGL-TH-MAX}}{I_{PG-LK-MAX} + I_{PGL-LK-MAX}} \quad (\text{eq. 19})$$

$$= \frac{3.3 \text{ V} - 1.3 \text{ V}}{1 \mu\text{A} + 3 \mu\text{A}} = 500 \text{ k}\Omega$$

Based on results above, the R_{PG} value could be selected in range from 3.3 kΩ to 500 kΩ to fit the example application.

Thermal Shutdown

When the LDO's die temperature exceeds the thermal shutdown threshold value the device is internally disabled. The IC will remain in this state until the die temperature decreases by the thermal shutdown hysteresis value. Once the IC temperature falls this way, the LDO is back enabled. The thermal shutdown feature provides the protection against overheating due to some application failure and it is not intended to be used as a normal working function.

Power Dissipation

Power dissipation caused by voltage drop across the LDO and by the output current flowing through the device needs to be dissipated out from the chip. The maximum power dissipation is dependent on the PCB layout, number of used Cu layers, Cu layers thickness and the ambient temperature. The maximum power dissipation can be computed by following equation:

$$P_{D(MAX)} = \frac{T_J - T_A}{\theta_{JA}} = \frac{125 - T_A}{\theta_{JA}} \text{ [W]} \quad (\text{eq. 20})$$

Where: (T_J - T_A) is the temperature difference between the junction and ambient temperatures and θ_{JA} is the thermal resistance (dependent on the PCB as mentioned above).

For reliable operation junction temperature should be less than +125°C.

The power dissipated by the LDO for given application conditions can be calculated by the next equation:

$$P_D = V_{IN} \cdot I_{GND} + (V_{IN} - V_{OUT}) \cdot I_{OUT} \text{ [W]} \quad (\text{eq. 21})$$

Where: I_{GND} is the LDO's ground current, dependent on the output load current.

Connecting the exposed pad and NC pin to a large ground planes helps to dissipate the heat from the chip.

The relation of θ_{JA} and P_{D(MAX)} to PCB copper area and Cu layer thickness could be seen on the Figures 57 and 58.

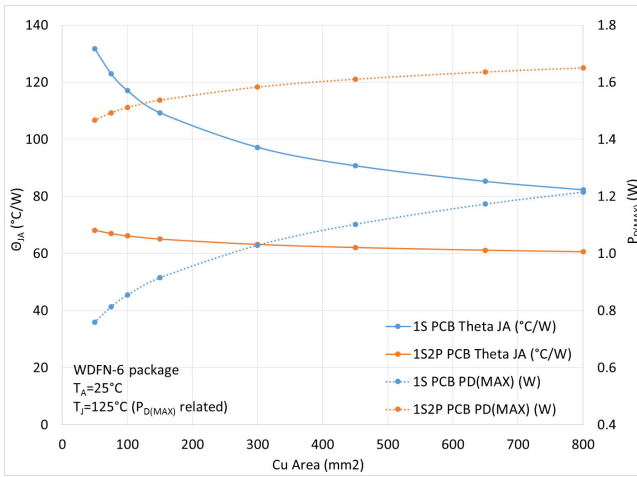


Figure 57. θ_{JA} and $P_{D(MAX)}$ vs. Copper Area

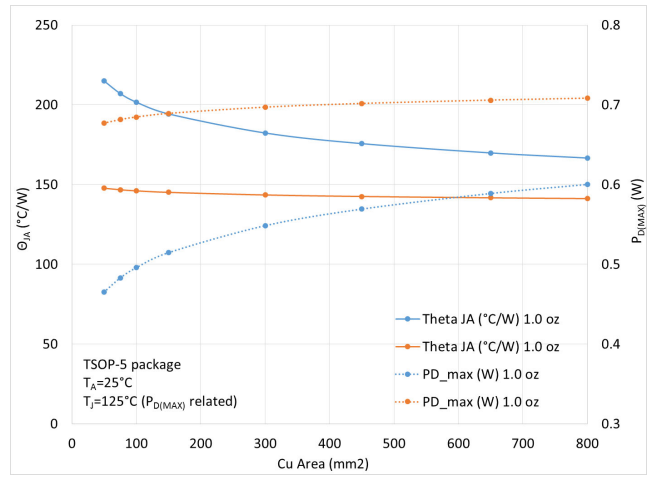


Figure 58. θ_{JA} and $P_{D(MAX)}$ vs. Copper Area

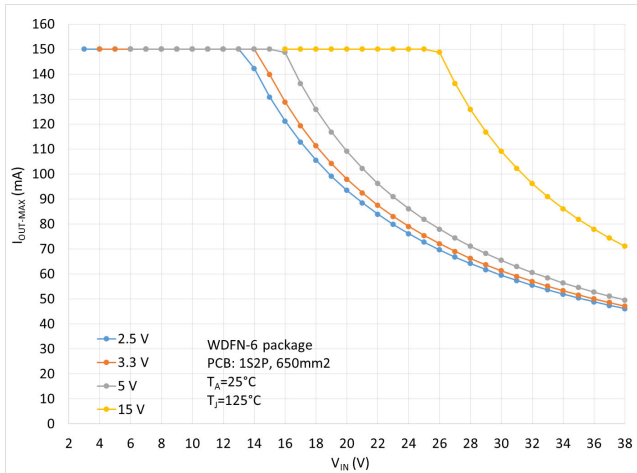


Figure 59. Maximum Output Current vs. Input Voltage

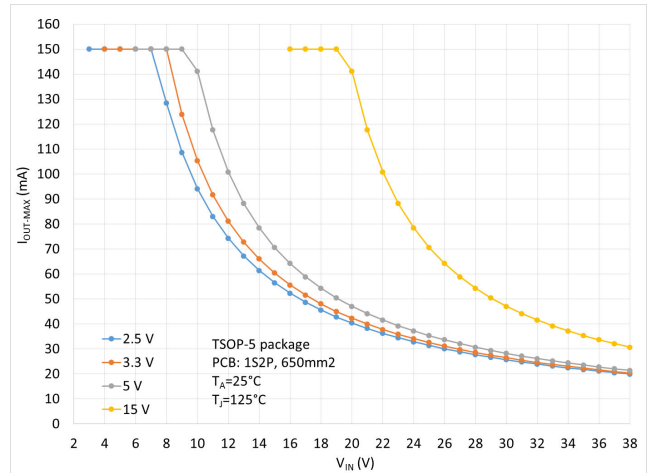


Figure 60. Maximum Output Current vs. Input Voltage

PCB Layout Recommendations

To obtain good LDO's stability, transient performance and good regulation characteristics place C_{IN} and C_{OUT} capacitors as close as possible to the device pins and make the PCB traces wide, short and place capacitors to the same layer as the LDO is (to avoid connection through vias). The same rules should be applied to the connections between C_{OUT} and the load – the less parasitic impedance the better transients and regulation at the point of load.

To minimize the solution size, use 0402 or 0201 capacitor sizes with appropriate effective capacitance in mind.

Regarding high impedance ADJ pin, prevent capacitive coupling of the trace to any switching signals in the circuitry.

Adequate input power filtering is always a good practice. For load transients the input capacitor value must be high enough to cover the current demands especially if the power source is connected by long traces/wires with high impedance.

Demo Boards

Below are the main part of the schematics and top/bottom board layout pictures of the NCP730 demo boards for various packages. These boards have been used during evaluation to capture the data shown in this datasheet like: transients, PSRR, startups etc. At some of these pictures are shown details of PCB traces surrounding the LDO including C_{IN} , C_{OUT} , resistor divider R_1/R_2 , feed forward capacitor C_{FF} and IN/OUT–FORCE/SENSE connections.

Generally, when testing LDOs dynamic performance on demo board which is connected to laboratory power supply typically by long cables, the device needs additional input capacitor. This capacitor covers the voltage drop generated by the load current transients at the impedance of long connection cables (note this is very different to normal application where the distance of the LDO to its power source is short).

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Besides the LDO application circuit, each demo board includes some supporting staff, the same at all boards:

- Positions for optional through hole SMB connectors at IN, OUT and EN pins (Molex 73100–0258 or compatible) mainly for line/load transients, PSRR, noise and startup testing the demo board includes.
- Edge connector where all these signal leads too (the appropriate receptacle type is SAMTEC MECF–20–01–L–DV–WT).
- Thermal management circuit (heating transistor and diodes as temperature sensors).

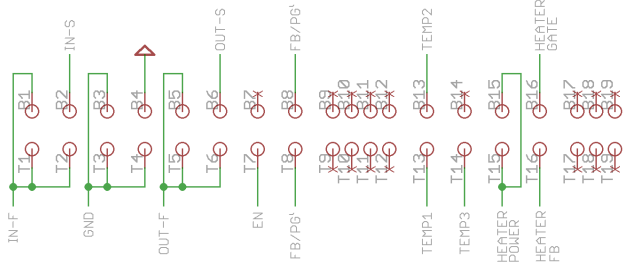


Figure 61. Edge Connector Pinout (All Demo Boards)

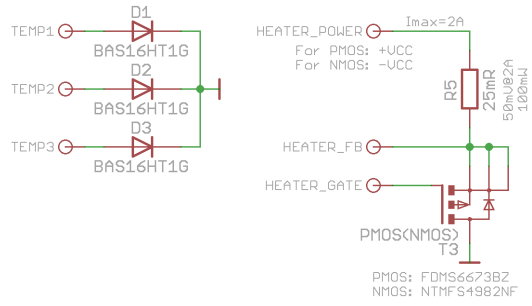


Figure 62. Thermal Circuit (All Demo Boards)

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NCP730ASN/BSN (TSOP-5 package) Demo Board (2 layer PCB, rev. 1)

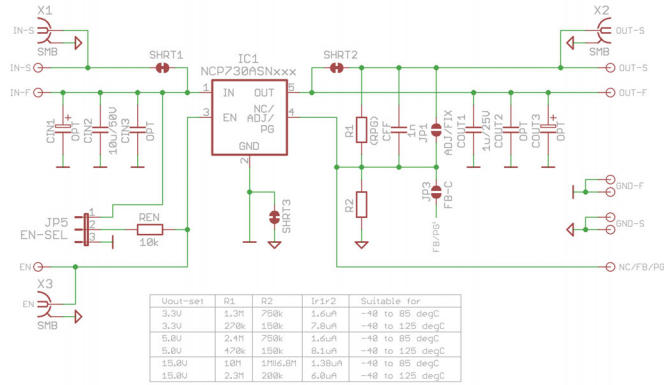


Figure 63. TSOP-5 Demo Board (2 layer, rev. 1) – Schematics (Main Part)

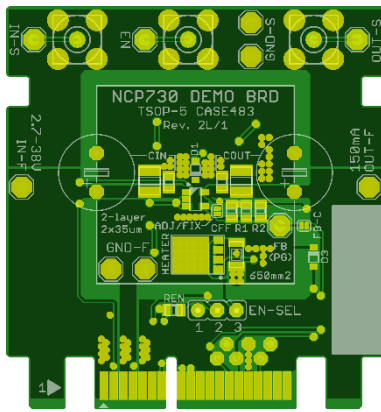


Figure 64. NCP730 Demo Board (2 layer, rev. 1) – PCB Top Layer

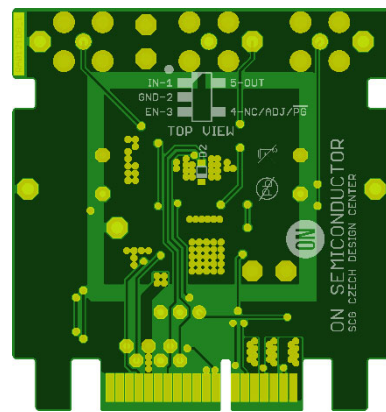


Figure 65. TSOP-5 Demo Board (2 layer, rev. 1) – PCB Bottom Layer

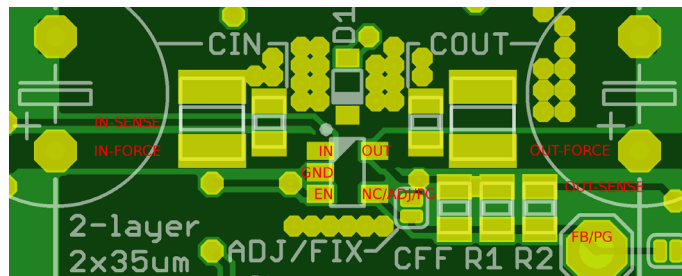


Figure 66. TSOP-5 Demo Board (2 layer, rev. 1) – PCB Top Layer, Zoomed, Added Signal Labels

NCP730

NCP730AMT/BMT (WDFN-6 2x2 package) Demo Board (2 layer PCB, rev. 1)

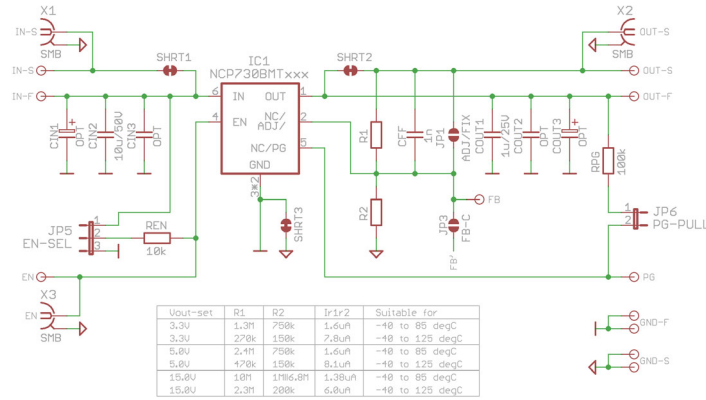


Figure 67. WDFN-6 2x2 Demo Board (2 layer, rev. 1) – Schematics (Main Part)

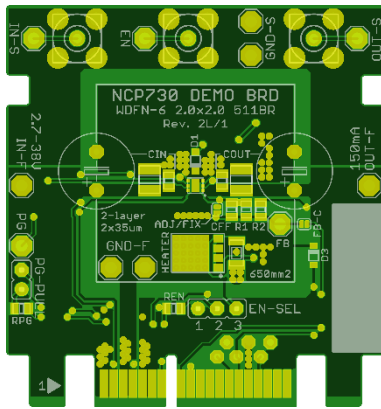


Figure 68. WDFN-6 2x2 Demo Board (2 layer, rev. 1) – PCB Top Layer

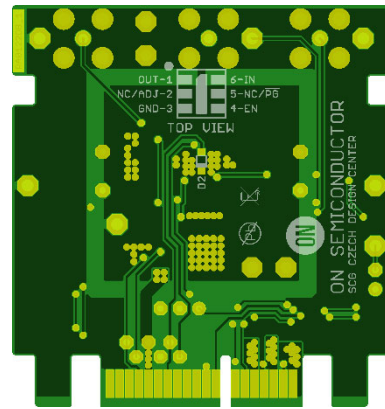


Figure 69. WDFN-6 2x2 Demo Board (2 layer, rev. 1) – PCB Bottom Layer

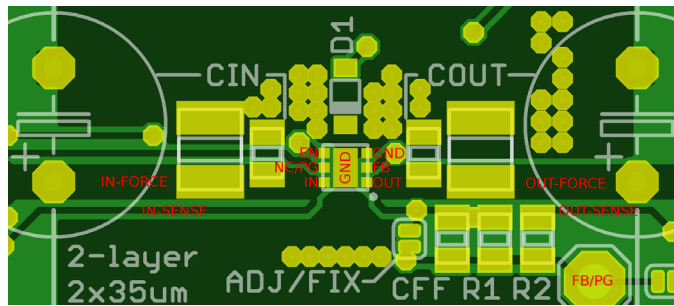


Figure 70. WDFN-6 2x2 Demo Board (2 layer, rev. 1) – PCB Top Layer, Zoomed, Added Signal Labels

NCP730

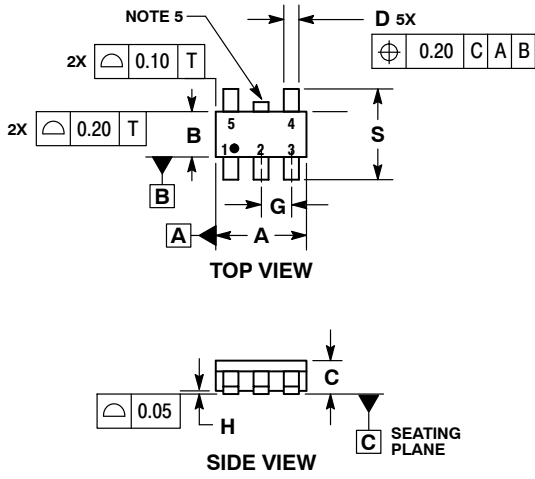
ORDERING INFORMATION

Part Number	Marking	Voltage Option (V _{OUT-NOM})	Version	Package	Shipping
NCP730ASNADJT1G	HAA	ADJ	Without PG	TSOP-5 (Pb-Free)	3000 / Tape & Reel
NCP730ASN250T1G	HAC	2.5 V			
NCP730ASN280T1G	HAD	2.8 V			
NCP730ASN300T1G	HAF	3.0 V			
NCP730ASN330T1G	HAE	3.3 V			
NCP730ASN500T1G	HAG	5.0 V			
NCP730BMTADJTBG	MA	ADJ	With PG	WDFN6 2x2 (Pb-Free)	3000 / Tape & Reel
NCP730BMT250TBG	MC	2.5 V			
NCP730BMT280TBG	MD	2.8 V			
NCP730BMT300TBG	ME	3.0 V			
NCP730BMT330TBG	MF	3.3 V			
NCP730BMT500TBG	MG	5.0 V			
NCP730BMT1500TBG	MH	15.0 V			

NCP730

PACKAGE DIMENSIONS

TSOP-5 CASE 483 ISSUE M

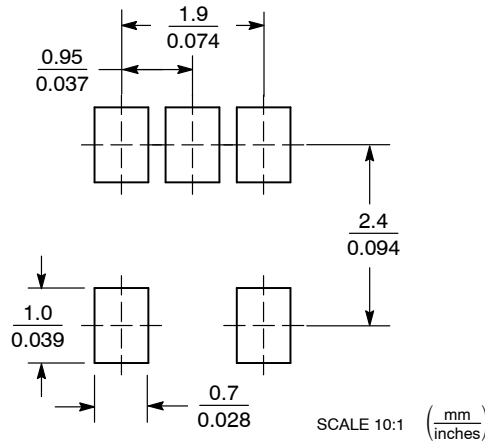


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

DIM	MILLIMETERS	
	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0° 10°	
S	2.50	3.00

SOLDERING FOOTPRINT*

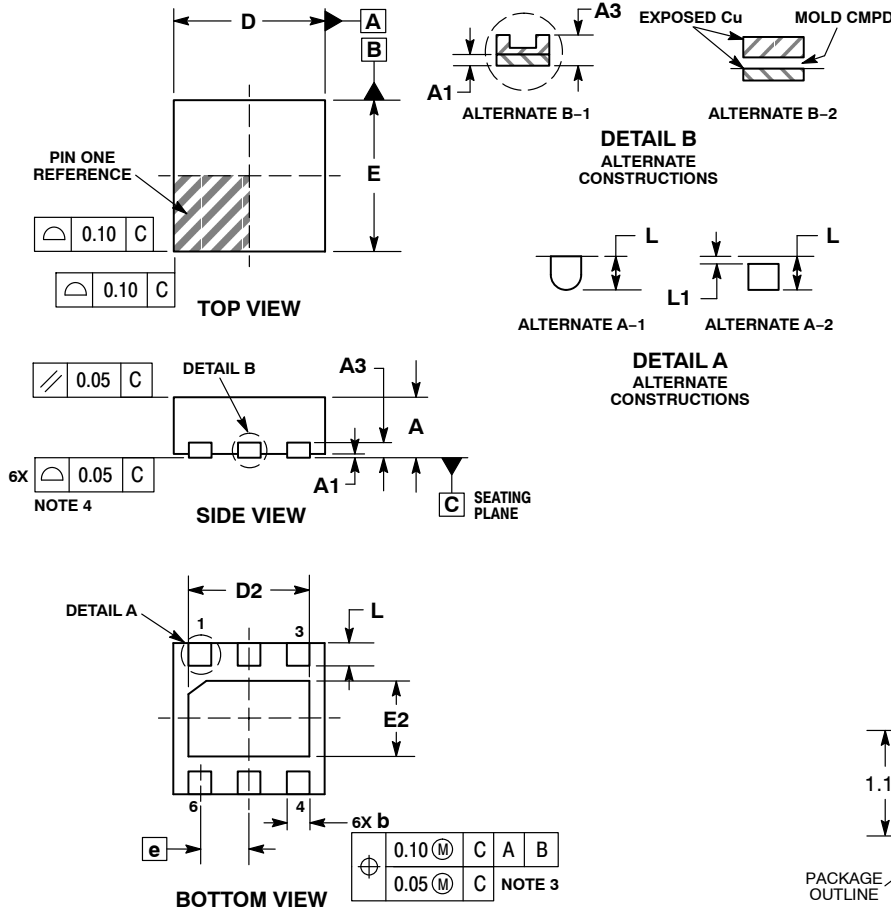


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NCP730

PACKAGE DIMENSIONS

WDFN6 2x2, 0.65P
CASE 511BR
ISSUE B

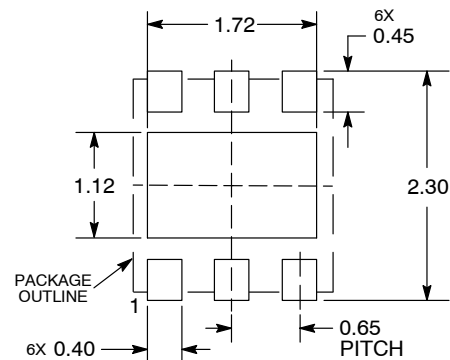


NOTES:

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2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. FOR DEVICES CONTAINING WETTABLE FLANK OPTION, DETAIL A ALTERNATE CONSTRUCTION A-2 AND DETAIL B ALTERNATE CONSTRUCTION B-2 ARE NOT APPLICABLE.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
L	0.20	0.40
L1	---	0.15

RECOMMENDED MOUNTING FOOTPRINT



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