NCP13992

High Performance Current Mode Resonant Controller with Integrated High-Voltage Drivers

The NCP13992 is a high performance current mode controller for half bridge resonant converters. This controller implements 600 V gate drivers, simplifying layout and reducing external component count. The built−in Brown−Out input function eases implementation of the controller in all applications. In applications where a PFC front stage is needed, the NCP13992 features a dedicated output to drive the PFC controller. This feature together with quiet skip mode technique further improves light load efficiency of the whole application. The NCP13992 provides a suite of protection features allowing safe operation in any application. This includes: overload protection, over−current protection to prevent hard switching cycles, brown−out detection, open optocoupler detection, automatic dead−time adjust, over−voltage (OVP) and over−temperature (OTP) protections.

Features

- High−Frequency Operation from 20 kHz up to 750 kHz
- Current Mode Control Scheme
- Automatic Dead−time with Maximum Dead−time Clamp
- Dedicated Startup Sequence for Fast Resonant Tank Stabilization
- Light Load Operation Mode for Improved Efficiency
- Quiet Skip Operation Mode for Minimize Transformer Acoustic Noise
- Latched or Auto−Recovery Overload Protection
- Latched or Auto−Recovery Output Short Circuit Protection
- Latched Input for Severe Fault Conditions, e.g. OVP or OTP
- Out of Resonance Switching Protection
- Open Feedback Loop Protection
- Precise Brown−out Protection
- PFC Stage Operation Control According to Load Conditions
- Startup Current Source with Extremely Low Leakage Current
- Dynamic Self−Supply (DSS) Operation in Off−mode or Fault Modes
- Pin to Adjacent Pin / Open Pin Fail Safe
- These are Pb−Free Devices

Typical Applications

- Adapters and Offline Battery Chargers
- Flat Panel Display Power Converters
- Computing Power Supplies
- Industrial and Medical Power Sources

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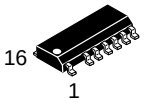
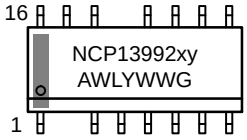


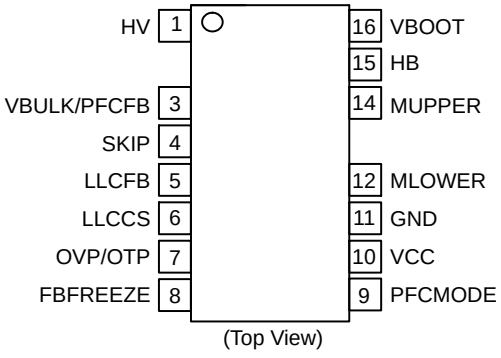
SOIC−16 NB
(LESS PINS 2 AND 13)
D SUFFIX
CASE 751DU

MARKING DIAGRAM



NCP13992 = Specific Device Code
x = A
y = A
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

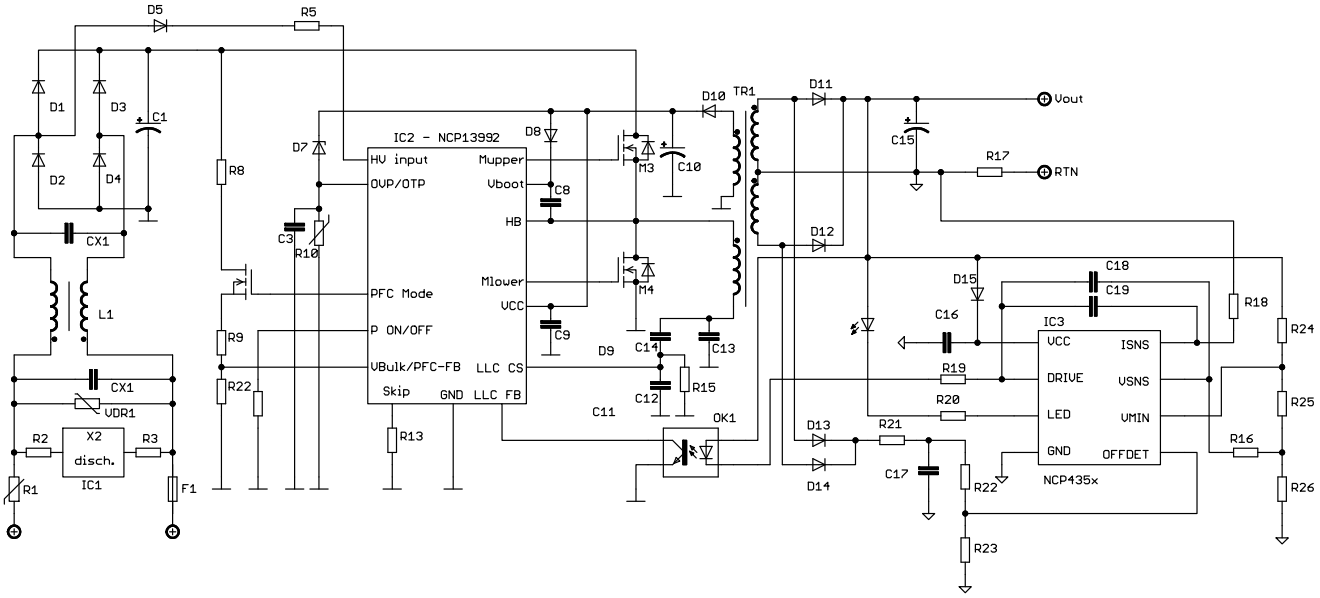


Figure 1. Typical Application Example without PFC Stage − WLLC Design

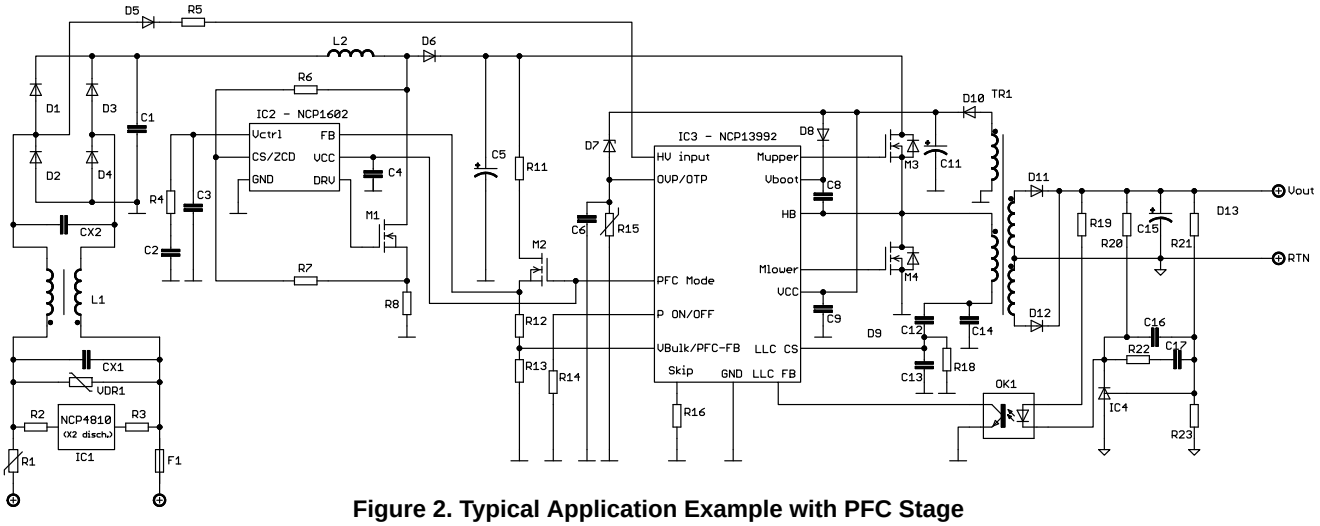


Figure 2. Typical Application Example with PFC Stage

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Pin Description
1	HV	High−voltage startup current source input	Connects to rectified AC line or to bulk capacitor to perform functions of Start−up Current Source and Dynamic Self−Supply
2	NC	Not connected	Increases the creepage distance
3	VBULK / PFC FB	Bulk voltage monitoring input	Receives divided bulk voltage to perform Brown−out protection.
4	SKIP	Skip threshold adjust	Sets the skip in threshold via a resistor connected to ground
5	LLC FB	LLC feedback input	Defines operating frequency based on given load conditions. Activates skip mode operation under light load conditions.
6	LLC CS	LLC current sense input	Senses divided resonant capacitor voltage to perform on−time modulation, out of resonant switching protection, over−current protection and secondary side short circuit protection.
7	OTP / OVP	Over−temperature and over−voltage protection input	Implements over−temperature and over−voltage protection on single pin.
8	FB FREEZE	Minimum internal FB level	Adjusts minimum internal FB level that can be reached during light load operation.
9	PFC MODE	PFC and external HV switch control output	Provides supply voltage for PFC front stage controller and/or enables Vbulk sensing network HV switch.
10	VCC	Supplies the controller	The controller accepts up to 20 V on VCC pin
11	GND	Analog ground	Common ground connection for adjust components, sensing networks and DRV outputs.
12	MLOWER	Low side driver output	Drives the lower side MOSFET
13	NC	Not connected	Increases the creepage distance
14	MUPPER	High side driver output	Drives the higher side MOSFET
15	HB	Half−bridge connection	Connects to the half−bridge output.
16	VBOOT	Bootstrap pin	The floating VCC supply for the upper stage

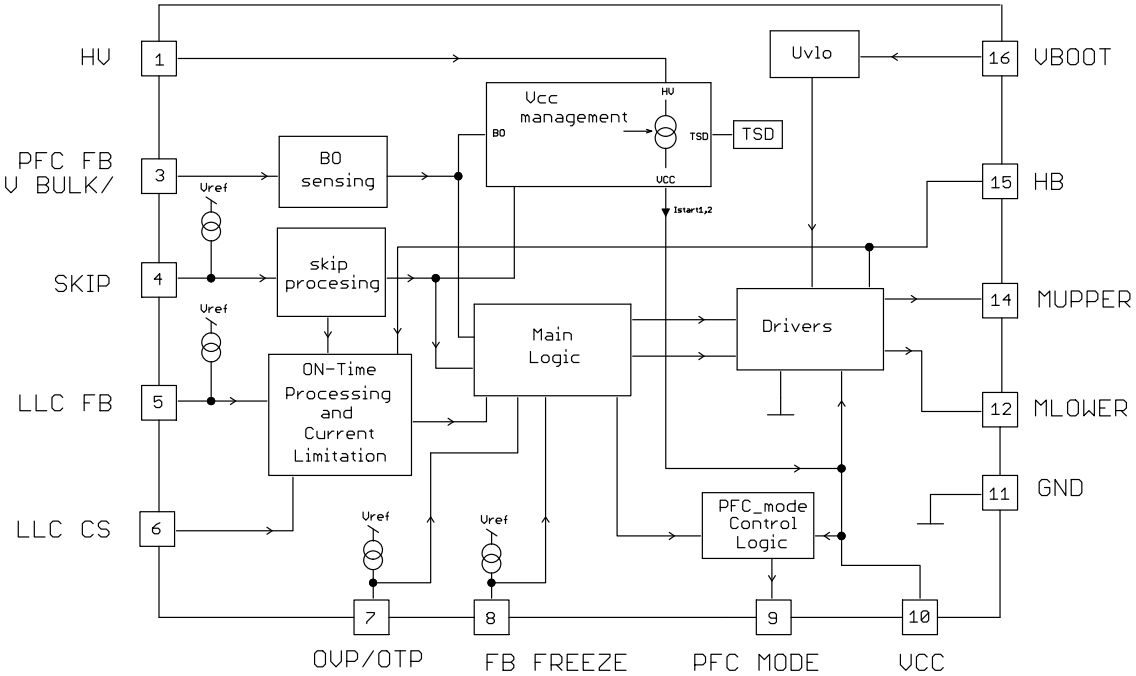


Figure 3. Internal Circuit Architecture

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
HV Startup Current Source HV Pin Voltage (Pin 1)	V_{HV}	−0.3 to 600	V
VBULK/PFC FB Pin Voltage (Pin3)	$V_{BULK/PFC\ FB}$	−0.3 to 5.5	V
SKIP Pin Voltage (Pin 4)	V_{SKIP}	−0.3 to 5.5	V
LLC FB Pin Voltage (Pin 5)	V_{FB}	−0.3 to 5.5	V
LLC CS Pin Voltage (Pin 6)	V_{CS}	−5 to 5	V
PFC MODE Pin Output Voltage (Pin 9)	$V_{PFC\ MODE}$	−0.3 to VCC+0.3	V
VCC Pin Voltage (Pin 10)	V_{CC}	−0.3 to 20	V
Low Side Driver Output Voltage (Pin 12)	V_{DRV_MLOWER}	−0.3 to VCC + 0.3	V
High Side Driver Output Voltage (Pin 14)	V_{DRV_MUPPER}	V_{HB} – 0.3 to V_{BOOT} + 0.3	V
High Side Offset Voltage (Pin 15)	V_{HB}	V_{Boot} −20 to V_{Boot} +0.3	V
High Side Floating Supply Voltage (Pin 16)	V_{BOOT}	−0.3 to 620	V
High Side Floating Supply Voltage (Pin 15 and 16)	$V_{Boot–VHB}$	−0.3 to 20.0	V
Allowable Output Slew Rate on HB Pin (Pin 15)	dV/dt_{max}	50	V/ns
OVP/OTP Pin Voltage (Pin 7)	$V_{OVP/OTP}$	−0.3 to 5.5	V
FB FREEZE Pin Voltage (Pin 8)	$V_{P\ ON/OFF}$	−0.3 to 5.5	V
Junction Temperature	T_J	−50 to 150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
Thermal Resistance Junction−to−air	$R_{\theta JA}$	130	°C/W
Human Body Model ESD Capability per JEDEC JESD22−A114F (except HV Pin – Pin 1)	−	4.5	kV
Machine Model ESD Capability per JEDEC JESD22−A115C	−	250	V
Charged−Device Model ESD Capability per JEDEC JESD22−C101E	−	1	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
1. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78

ELECTRICAL CHARACTERISTICS

(For typical values Tj = 25°C, for min/max values Tj = −40°C to +125°C, Vcc = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
HV STARTUP CURRENT SOURCE						
V_{HV_MIN1}	Minimum voltage for current source operation (V_{CC} = V_{CC_ON} −0.5 V, I_{START2} drops to 95%)	1	−	−	60	V
V_{HV_MIN2}	Minimum voltage for current source operation (V_{CC} = V_{CC_ON} −0.5 V, I_{START2} drops to 5 mA)	1	−	−	60	V
I_{START1}	Current flowing out of V_{CC} pin (V_{CC} = 0 V)	1, 10	0.2	0.5	0.8	mA
I_{START2}	Current flowing out of V_{CC} pin (V_{CC} = V_{CC_ON} −0.5 V)	1, 10	6	9	13	mA
I_{START_OFF}	Off−state leakage current (V_{HV} = 500 V, V_{CC} = 15 V)	1	−	−	10	μA
SUPPLY SECTION						
V_{CC_ON}	Turn−on threshold level, V_{CC} going up	10	15.3	15.8	16.3	V
V_{CC_OFF}	Minimum operating voltage after turn−on	10	9.0	9.5	10	V
V_{CC_RESET}	V_{CC} level at which the internal logic gets reset	10	5.8	6.6	7.2	V
$V_{CC\_INHIBIT}$	V_{CC} level for I_{START1} to I_{START2} transition	10	0.40	0.80	1.25	V
$I_{CC\_SKIP−MODE}$	Controller supply current in skip−mode, V_{CC} = 15 V, OVP/OTP block debiased during skip mode	10, 11	500	780	950	μA

ELECTRICAL CHARACTERISTICS

(For typical values Tj = 25°C, for min/max values Tj = −40°C to +125°C, Vcc = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
SUPPLY SECTION						
I_{CC_LATCH}	Controller supply current in latch−off mode, $V_{CC} = V_{CC\_ON} - 0.2$ V	10, 11	350	570	700	μA
$I_{CC\_AUTOREC}$	Controller supply current in auto−recovery mode, $V_{CC} = V_{CC\_ON} - 0.2$ V	10, 11	400	580	700	μA
$I_{CC\_OPERATION}$	Controller supply current in normal operation, f_{sw} = 100 kHz, C_{load} = 1 nF, V_{CC} = 15 V	10, 11	4.0	5.4	7.0	mA
BOOTSTRAP SECTION						
V_{BOOT_ON}	Startup voltage on the floating section (Note 3)	16, 15	7.5	9.0	10.0	V
V_{BOOT_OFF}	Cutoff voltage on the floating section	16, 15	7.0	8.2	9.1	V
I_{BOOT1}	Upper driver consumption, no DRV pulses	16, 15	30	75	130	μA
I_{BOOT2}	Upper driver consumption, C_{load} = 1 nF between Pins 13 & 15 f_{sw} = 100 kHz, HB connected to GND	16, 15	1.30	1.65	2.00	mA
HB DISCHARGER						
$I_{DISCHARGE1}$	HB sink current capability V_{HB} = 30 V	15	7	9.6	12	mA
$I_{DISCHARGE2}$	HB sink current capability $V_{HB} = V_{HB\_MIN}$	15	1	4.1	8	mA
V_{HB_MIN}	HB voltage @ $I_{DISCHARGE}$ changes from 2 to 0 mA	15	–	–	10	V
DRIVER OUTPUTS						
t_r	Output voltage rise−time @ C_L = 1 nF, 10−90% of output signal	12, 14	20	45	80	ns
t_f	Output voltage fall−time @ C_L = 1 nF, 10−90% of output signal	12, 14	5	30	50	ns
R_{OH}	Source resistance	12, 14	4	16	32	Ω
R_{OL}	Sink resistance	12, 14	1	5	11	Ω
$I_{DRVSOURCE}$	Output high short circuit pulsed current V_{DRV} = 0 V, PW ≤ 10 μs	12, 14	–	0.5	–	A
$I_{DRVSINK}$	Output high short circuit pulsed current V_{DRV} = VCC, PW ≤ 10 μs	12, 14	–	1	–	A
I_{HV_LEAK}	Leakage current on high voltage pins to GND	14, 15, 16	–	–	5	μA
DEAD−TIME GENERATION						
$t_{DEAD\_TIME\_MAX}$	Maximum Dead−time value if no dV/dt falling/rising edge is received	12, 14	720	800	880	ns
N_{DT_MAX}	Number of DT_MAX events to enters IC into fault	12, 14, 16	–	8	–	–
dV/dt DETECTOR						
P_{dV/dt_th_1}	Positive slew rate on V_{BOOT} pin above which is dV/dt_P sensor triggered, VHB rising from 0 to 100 V linearly (Note 2)	16	–	178	200	V/μs
P_{dV/dt_th_2}	Positive slew rate on V_{BOOT} pin above which is dV/dt_P sensor triggered, VHB rising from 100 to 200 V linearly (Note 2)	16	–	226	250	V/μs
P_{dV/dt_th_3}	Positive slew rate on V_{BOOT} pin above which is dV/dt_P sensor triggered, VHB rising from 200 to 400 V linearly (Note 2)	16	–	246	280	V/μs
N_{dV/dt_th_1}	Negative slew rate on V_{BOOT} pin above which is dV/dt_N sensor triggered, VHB falling from 100 to 0 V linearly	16	–	163	–	V/μs
N_{dV/dt_th_2}	Negative slew rate on V_{BOOT} pin above which is dV/dt_N sensor triggered, VHB falling from 200 to 100 V linearly	16	–	290	–	V/μs
N_{dV/dt_th_3}	Negative slew rate on V_{BOOT} pin above which is dV/dt_N sensor triggered, VHB falling from 400 to 200 V linearly	16	–	250	–	V/μs

ELECTRICAL CHARACTERISTICS

(For typical values Tj = 25°C, for min/max values Tj = −40°C to +125°C, Vcc = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
PFC MODE OUTPUT AND P ON/OFF ADJUST						
$V_{PFC\_M\_OFF}$	PFC MODE output voltage when application enters skip mode (inject 1 mA into the PFC MODE output)	9	−	−	0.1	V
$V_{PFC\_M\_BO}$	PFC MODE output voltage when $V_{FB} < V_{P\ ON/OFF}$ (sink 1 mA current from PFC MODE output)	9	5.75	6.00	6.25	V
$V_{PFC\_M\_ON}$	PFC MODE output voltage when $V_{FB} > V_{P\ ON/OFF}$ (sink 20 mA current from PFC MODE output)	9	V_{CC} − 0.4	−	−	V
$I_{PFC\_M\_LIM}$	PFC MODE output current limit ($V_{PFC\ MODE}$ < 2 V)	9	0.7	1.2	1.85	mA
OVP/OTP						
V_{OVP}	OVP threshold voltage ($V_{OVP/OTP}$ going up)	7	2.35	2.50	2.65	V
V_{OTP}	OTP threshold voltage ($V_{OVP/OTP}$ going down)	7	0.76	0.80	0.84	V
I_{OTP}	OTP/OVP pin source current for external NTC – during normal operation	7	90	95	100	μA
I_{OTP_BOOST}	OTP/OVP pin source current for external NTC – during startup	7	180	190	200	μA
t_{OVP_FILTER}	Internal filter for OVP comparator	7	32	37	44	μs
t_{OTP_FILTER}	Internal filter for OTP comparator	7	200	330	500	μs
t_{BLANK_OTP}	Blanking time for OTP input during startup	7	14	16	18	ms
V_{CLAMP_OVP/OTP_1}	OVP/OTP pin clamping voltage @ $I_{OVP/OTP}$ = 0 mA	7	1.0	1.2	1.4	V
V_{CLAMP_OVP/OTP_2}	OVP/OTP pin clamping voltage @ $I_{OVP/OTP}$ = 1 mA	7	1.8	2.4	3.0	V
START−UP SEQUENCE PARAMETERS						
$t_{1st\_MLOWER\_TON}$	Initial Mlower DRV on−time duration	12	4.7	4.9	5.4	μs
$t_{1st\_MUPPER\_TON}$	Initial Mupper DRV on−time duration	14	0.72	0.79	0.88	μs
$t_{SS\_INCREMENT}$	On−time period increment during soft−start	12, 14	17	20	22	ns
$K_{SS\_INCREMENT}$	Soft−Start increment division ratio	12, 14	−	4	−	−
$t_{WATCHDOG}$	Time duration to restart IC if start−up phase is not finished	12, 14	0.45	0.50	0.55	ms
FEEDBACK SECTION						
R_{FB}	Internal pull−up resistor on FB pin	5	15	18	25	kΩ
K_{FB}	V_{FB} to internal current set point division ratio	5	1.92	2.00	2.08	−
V_{FB_REF}	Internal voltage reference on the FB pin	5	4.60	4.95	5.30	V
V_{FB_CLAMP}	Internal clamp on FB input of On−time comparator referred to external FB pin voltage	5	4.4	4.6	4.8	V
$V_{FB\_SKIP\_HYST}$	Skip comparator hysteresis	5	148	174	222	mV
$V_{FB\_LL\_IN}$	Feedback voltage thresholds to enter Light load mode	5	0.468	0.508	0.548	V
$V_{FB\_LL\_OUT}$	Feedback voltage thresholds to exit Light load mode	5	0.595	0.635	0.675	V
$t_{1st\_MLOWER\_SKIP}$	On−time duration of 1st Mlower pulse when FB cross $V_{FB\_SKIP\_IN}$ + $V_{FB\_SKIP\_HYST}$ threshold	5, 12	0.95	1.05	1.15	μs
$V_{1st\_MUPPER\_SKIP}$	Internal FB level reduction during 1st Mupper pulse when FB cross $V_{FB\_SKIP\_IN}$ + $V_{FB\_SKIP\_HYST}$ threshold (Note 2)	5, 6, 14	−	150	−	mV
SKIP INPUT						
I_{SKIP}	Internal Skip pin current source	4	48	50	52	μA
$C_{SKIP\_LOAD\_MAX}$	Maximum loading capacitance for skip pin voltage filtering (Note 2)	4	−	−	10	nF

ELECTRICAL CHARACTERISTICS

(For typical values Tj = 25°C, for min/max values Tj = −40°C to +125°C, Vcc = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
QUIET−SKIP PARAMETERS						
$t_{LAST\_ML\_PATTERN}$	The portion of previous MU on−time that is place for last ML pulse in pattern	12	−	50	−	%
$t_{LAST\_ML\_SKIP}$	The portion of previous MU on−time that is place for last ML pulse before the LL or skip mode is activated	12	−	50	−	%
t_{GEAR_UP}	Skip burst off−time duration that is needed to increase number of skipped valleys between following patterns	12, 14	−	5	−	ms
t_{GEAR_DOWN}	Skip burst on−time duration that is needed to decrease number of skipped valleys between following patterns	12, 14	−	15	−	ms
t_{VALLEY_WD}	Time duration to force valley count logic if valley is not detected	12, 14	4.5	5	5.5	μs
t_{QS_timer}	Quiet Timer duration	12, 14	−	5	−	ms
$N_{QS\_1/4}$	Number of patterns adjustment when bust period is shorter than ¼ of QS_timer duration	12, 14	−	2	−	−
$N_{QS\_2/4}$	Number of patterns adjustment when bust period is longer than ¼ and shorter than 2/4 of QS_timer duration	12, 14	−	1	−	−
$N_{QS\_3/4}$	Number of patterns adjustment when bust period is longer than 2/4 and shorter than 3/4 of QS_timer duration	12, 14	−	0	−	−
$N_{QS\_4/4}$	Number of patterns adjustment when bust period is longer than 3/4 and shorter than 4/4 of QS_timer duration	12, 14	−	0	−	−
N_{QS_INF}	Number of patterns adjustment when bust period is longer than QS_timer duration	12, 14	−	−1	−	−
$N_{PATTERN\_INIT}$	Initial number of patterns placed when LL or skip mode is activated	12, 14	−	1	−	−
N_{LL_blank}	Number of MU pulses during which FB_LL_IN cmp is blanked once VFB > VFB_LL_OUT	14	−	60	−	−
FB FREEZE INPUT						
I_{FB_Freeze}	FB Freeze pin current source	4	18	20	22	μA
$C_{FB\_Freeze\_LOAD\_MAX}$	Maximum loading capacitance for FB Freeze pin voltage filtering (Note 2)	4	−	−	10	nF
CURRENT SENSE INPUT SECTION						
t_{pd_CS}	On−time comparator delay to Mupper driver turn off V_{FB} = 2.5 V, V_{CS} goes up from –2.5 V to 2.5 V with rising edge of 100 ns	5, 6	−	−	250	ns
$I_{CS\_LEAKAGE}$	Current sense input leakage current for V_{CS} = ± 3 V	6	−	−	±1	μA
V_{CS_OFFSET}	Current sense input offset voltage	6	160	200	240	mV
t_{LEB}	Leading edge blanking time of the on−time comparator output	5, 6, 14	360	440	540	ns
LFFGAIN	Line Feed Forward current source transconductance ($V_{VBULK/PFC\_FB} > V_{BO}$)	3, 6	−	0	−	μA/V
FAULTS AND AUTO−RECOVERY TIMER						
t_{TON_MAX}	Maximum on−time clamp	12, 14	7.3	7.7	8.4	μs
$N_{TON\_MAX\_COUNTER}$	Number of TON_MAX events to confirm fault	12,14	−	1	−	−
$t_{FB\_FAULT\_TIMER}$	FB fault timer duration	−	160	200	240	ms
V_{FB_FAULT}	FB voltage when FB fault is detected	5	4.5	4.7	4.9	V
$N_{CS\_FAULT\_COUNTER}$	Number of CS_fault cmp. pulses to confirm CS fault	−	−	5	−	−
V_{CS_FAULT}	CS voltage when CS fault is detected (NCP13992xA)	6	2.5	2.7	2.9	V

ELECTRICAL CHARACTERISTICS

(For typical values Tj = 25°C, for min/max values Tj = −40°C to +125°C, Vcc = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
FAULTS AND AUTO−RECOVERY TIMER						
t_{A-REC_TIMER}	Auto−recovery duration (common timer for all fault condition)	−	0.8	1	1.2	s
BROWN−OUT PROTECTION						
V_{BO}	Brown−out turn−off threshold	3	0.965	1.000	1.035	V
I_{BO}	Brown−out hysteresis current, $V_{VBULK/PFC\_FB} < V_{BO}$	3	4.1	5.0	5.7	μA
V_{BO_HYST}	Brown−Out comparator hysteresis	3	5	12	25	mV
I_{BO_BIAS}	Brown−Out input bias current	3	−	−	0.05	μA
t_{BO_FILTR}	BO filter duration	3	10	20	30	μs
RAMP COMPENSATION						
RC_{GAIN}	Ramp compensation gain	−	58	82	108	mV/μs
t_{RC_SHIFT}	Ramp compensation time shift	−	−	0.4	−	μs
TEMPERATURE SHUTDOWN PROTECTION						
T_{TSD}	Temperature shutdown T_J going up	−	−	124	−	°C
T_{TSD_HYST}	Temperature shutdown hysteresis	−	−	30	−	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Guaranteed by design.
3. Minimal resistance connected in series with bootstrap diode is 3.3 Ω

IC OPTIONS

Option	FB fault	FB fault source	Cumulative FB fault timer/ counter	CS_FAULT	TON_MAX	OVP	OTP	OVP/OTP bias during skip
NCP13992AA	Auto−recovery	Timer	NO	Auto−recovery	Auto−recovery	Latch	Auto−recovery	ON

Option	PFC_MODE skip status	Skip mode	Dead time control	Dead time fault	BO status	Ramp comp status	Dedicated Soft_start_-seq
NCP13992AA	ON	Quiet Skip	Auto−recovery	Active OFF	ON	Without ramp shift	ON

ORDERING INFORMATION

Device	Package Marking	Package	Shipping†
NCP13992AADR2G	NCP13992AA	SOIC−16, Less Pin 2 and 13 (Pb−free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

VCC Management with High−voltage Startup Current Source

The NCP13992 controller features a HV startup current source that allows fast startup time and extremely low standby power consumption. Two startup current levels (I_{start1} and I_{start2}) are provided by the system for safety in case of short circuit between VCC and GND pins. In addition, the HV startup current source features a dedicated over−temperature protection to prevent IC damage for any failure mode that may occur in the application. The HV startup current source is primarily enabled or disabled based on V_{CC} level. The startup HV current source can be also enabled by BO_OK rising edge, auto−recovery timer end and TSD end event. The HV startup current source charges the VCC capacitor before IC start−up.

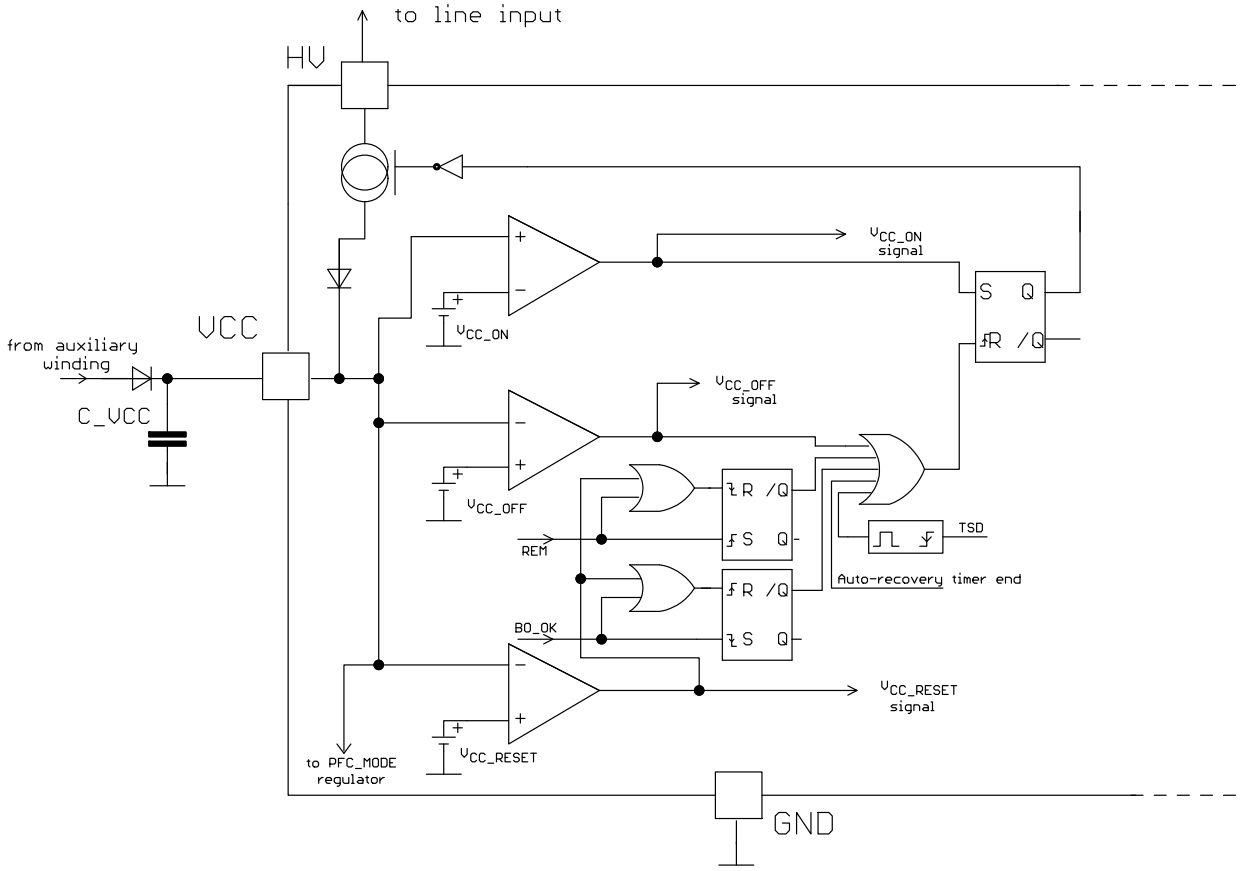


Figure 4. Internal Connection of the VCC Management Block

The NCP13992 controller disables the HV startup current source once the VCC pin voltage level reaches V_{CC_ON} threshold – refer to Figure 4. The application then starts operation and the auxiliary winding maintains the voltage bias for the controller during normal and skip−mode operating modes. The IC operates in so called Dynamic Self Supply (DSS) mode when the bias from auxiliary winding is not sufficient to keep the V_{CC} voltage above V_{CC_OFF} threshold (i.e. V_{CC} voltage is cycling between V_{CC_ON} and V_{CC_OFF} thresholds with no driver pulses on the output during positive V_{CC} ramp). Please refer to Figure 23 through Figure 25 to find an illustration of the NCP13992 VCC management system under all operating conditions/modes.

The HV startup current source features an independent over–temperature protection system to limit I_{start2} current when the die temperature reaches 130°C. At this temperature, I_{start2} will be progressively to prevent the die temperature from rising above 130°C.

Brown−out Protection − VBULK/PFC FB Input

Resonant tank of an LLC converter is always designed to operate within a specific bulk voltage range. Operation below minimum bulk voltage level would result in current and temperature overstress of the converter power stage. The NCP13992 controller features a VBULK/PFC FB input in order to precisely adjust the bulk voltage turn−ON and turn−OFF levels. This Brown−Out protection (BO) greatly simplifies application level design.

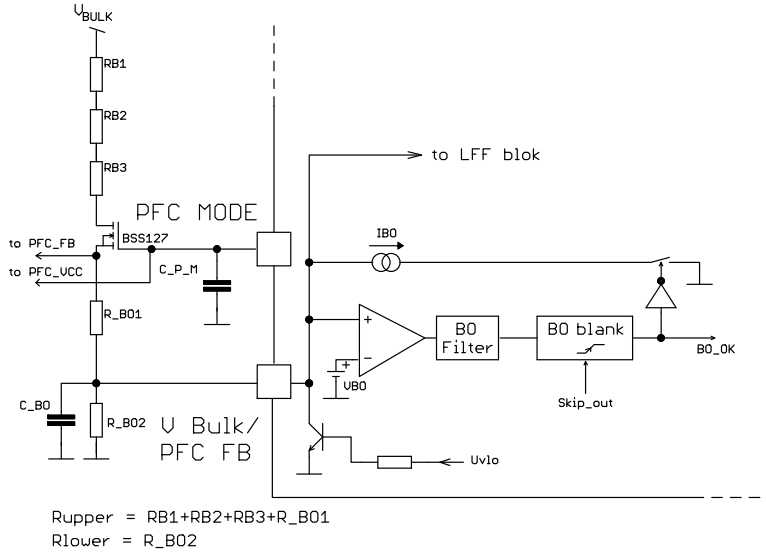


Figure 5. Internal Connection of the Brown−out Protection Block

The internal circuitry shown in Figure 5 allows monitoring the high−voltage input rail (V_{bulk}). A high−impedance resistive divider made of R_{upper} and R_{lower} resistors brings a portion of the V_{bulk} rail to the VBULK/PFC FB pin. The Current sink (I_{BO}) is active below the *bulk voltage turn−on* level (V_{bulk_ON}). Therefore, the *bulk voltage* turn−on level is higher than defined by the division ratio of the resistive divider. To the contrary, when the internal BO_OK signal is high, i.e. the application is running, the I_{BO} sink is disabled. The bulk voltage turn−off threshold (V_{bulk_OFF}) is then given by BO comparator reference voltage directly on the resistor divider. The advantage of this solution is that the V_{bulk_OFF} threshold precision is not affected by I_{BO} hysteresis current sink tolerance.

The V_{bulk_ON} and V_{bulk_OFF} levels can be calculated using equations below:

The I_{BO} is ON:

$$V_{BO} + V_{BOhyst} = V_{bulk\_ON} \cdot \frac{R_{lower}}{R_{lower} + R_{upper}} - I_{BO} \cdot \left(\frac{R_{lower} \cdot R_{upper}}{R_{lower} + R_{upper}} \right) \quad \text{(eq. 1)}$$

The I_{BO} is OFF:

$$V_{BO} = V_{bulk\_OFF} \cdot \frac{R_{lower}}{R_{lower} + R_{upper}} \quad \text{(eq. 2)}$$

One can extract R_{lower} term from equation 2 and use it in equation 1 to get needed R_{upper} value:

$$R_{lower} = \frac{\frac{V_{bulk\_ON} \cdot V_{BO}}{V_{bulk\_OFF}} - V_{BO} - V_{BOhyst}}{I_{BO} \cdot \left(1 - \frac{V_{BO}}{V_{bulk\_OFF}} \right)} \quad \text{(eq. 3)}$$

$$R_{upper} = R_{lower} \cdot \frac{V_{bulk\_OFF} - V_{BO}}{V_{BO}} \quad \text{(eq. 4)}$$

Note that the VBULK/PFC FB pin is pulled down by an internal switch when the controller is in startup phase − i.e. when the V_{CC} voltage ramps up from $V_{CC} < V_{CC\_RESET}$ towards the V_{CC_ON} level on the VCC pin. This feature assures that the VBULK/PFC FB pin voltage will not ramp up before the IC operation starts. The I_{BO} hysteresis current sink is activated and BO discharge switch is disabled once the V_{CC} voltage crosses V_{CC_ON} threshold. The VBULK/PFC FB pin voltage then ramps up naturally according to the BO divider information. The BO comparator then authorizes or disables the LLC stage operation based on the actual V_{bulk} level.

The low I_{BO} hysteresis current of the NCP13992 brown out protection system allows increasing the bulk voltage divider resistance and thus reduces the application power consumption during light load operation. On the other hand, the high impedance divider can be noise sensitive due to capacitive coupling to HV switching traces in the application. This is why a filter (t_{BO_FILTR}) is added after the BO comparator in order to increase the system noise immunity. Despite the internal filtering, it is also recommended to keep a good layout for BO divider resistors and use a small external filtering capacitor on the VBULK/PFC pin if precise BO detection wants to be achieved.

The bulk voltage HV divider can be also used by a PFC front stage controller as a feedback sensing network (refer again to Figure 5). The shared bulk voltage resistor divider between PFC and LLC stage offers a way how to further reduce power losses during no−load operation. The NCP13992 features a PFC MODE pin that disconnects bias

of the PFC stage during light load or fault mode operation. This technique further reduces the no−load power consumption down again since the power losses of voltage divider are not affected by the bulk voltage at all.

Please refer to Figure 23 through Figure 25 for an illustration of NCP13992 Brown−out protection system in all operating conditions/modes.

The VBULK/PFC FB pin voltage is also used by Line Feed Forward block (LFF). Please refer to ON−time modulation and feedback loop block description for more information about LFF function.

Over−voltage and Over−temperature Protection

The OVP/OTP pin is a dedicated input to allow for a simple and cost effective implementation of two key protection features that are needed in adapter applications: over−voltage (OVP) and over−temperature (OTP) protections. Both of these protections can be either latched or auto−recovery– depending on the version of NCP13992. The OVP/OTP pin has two voltage threshold levels of detection (V_{OVP} and V_{OTP}) that define a no−fault window. The controller is allowed to run when OVP/OTP input voltage is within this working window. The controller stops the operation, after filter time delay, when the OVP/OTP input voltage is out of the no−fault window. The controller then either latches−off or or starts an auto−recovery timer − depending on the IC version − and triggered the protection threshold (V_{OTP} or V_{OVP}).

The internal current source I_{OTP} allows a simple OTP implementation by using a single negative temperature coefficient (NTC) thermistor. An active soft clamp composed from V_{clamp} and R_{clamp} components prevents the OVP/OTP pin voltage from reaching the V_{OVP} threshold when the pin is pulled up by the I_{OTP} current. An external pull − up current, higher than the pull − down capability of the internal clamp ($V_{CLAMP\_OVP/OTP}$), has to be applied to pull the OVP/OTP pin above V_{OVP} threshold to activate the OVP protection. The t_{OVP_FILTER} and t_{OTP_FILTER} filters are implemented in the system to avoid any false triggering of the protections due to application noise and/or poor layout.

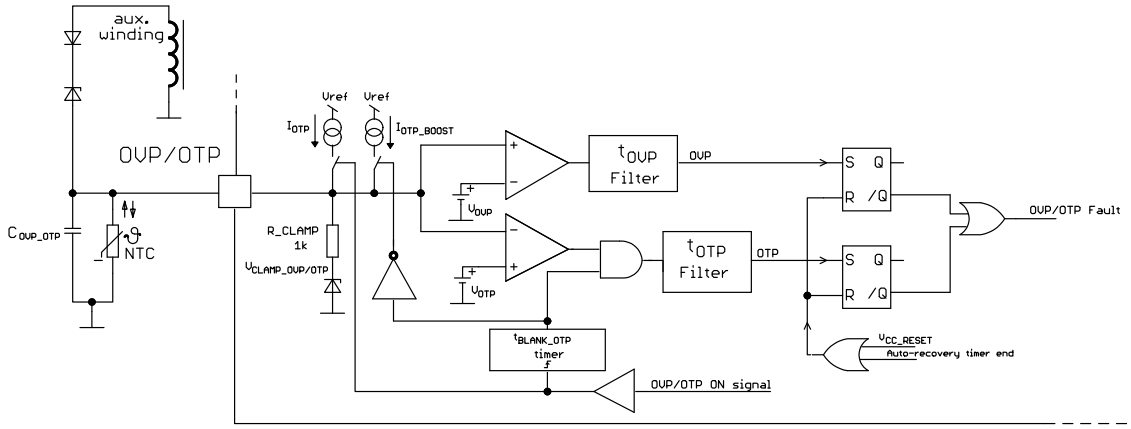


Figure 6. Internal Connection of OVP/OTP Input

The OTP protection could be falsely triggered during controller startup due to the external filtering capacitor charging current. Thus the t_{BLANK_OTP} period has been implemented in the system to overcome such behavior. The OTP comparator output is ignored during t_{BLANK_OTP} period. In order to speed up the charging of the external filtering capacitor C_{OVP_OTP} connected to OVP/OTP pin, the I_{OTP} current has been doubled to I_{OTP_BOOST}. The maximum value of filtering capacitor is 100 nF.

The OVP/OTP ON signal is set after the following events:

- the V_{CC} voltage exceeds the V_{CC_ON} threshold during first start−up phase (after VCC pin voltage was below V_{CC_RESET} threshold)
- BO OK signal is received from BO block
- Auto−recovery timer elapsed and a new restart occurs
- IC returns to operation from skip−mode ($V_{FB\_SKIP\_IN}$ + $V_{FB\_SKIP\_HYST}$ threshold was reached)

The I_{OTP} current source is disabled when:

- V_{CC} falls below V_{CC_OFF} threshold
- BO OK signal goes to low state (i.e. Brown−out condition occurs on the mains)
- Fault signal is activated (Auto−recovery timer starts counting or Latch fault is present)
- IC goes into the skip−mode operation ($V_{FB\_SKIP\_IN}$ threshold was reached)

IC option that keeps OVP/OTP block working during skip mode is also available. The IC consumption is increased for this version by OVP/OTP block bias.

The latched OVP or OTP versions of NCP13992 enters latched protection mode when V_{CC} voltage cycles between V_{CC_ON} and V_{CC_OFF} thresholds and no pulses are provided by drivers. The controller VCC pin voltage has to be cycled down below V_{CC_RESET} threshold in order to restart operation. This would happen when the power supply is unplugged from the mains.

PFC MODE Output

The NCP13992 has PFC MODE pin that can be used to disable or enable PFC stage operation based on actual application operating state – please refer to Figure 7. The PFC MODE output pin can be used for two purposes:

1st to control the external small signal HV MOSFET switch that connects the bulk voltage divider to the VBULK/PFC FB input

2nd to control the PFC front stage controller operation via PFC controller supply pin

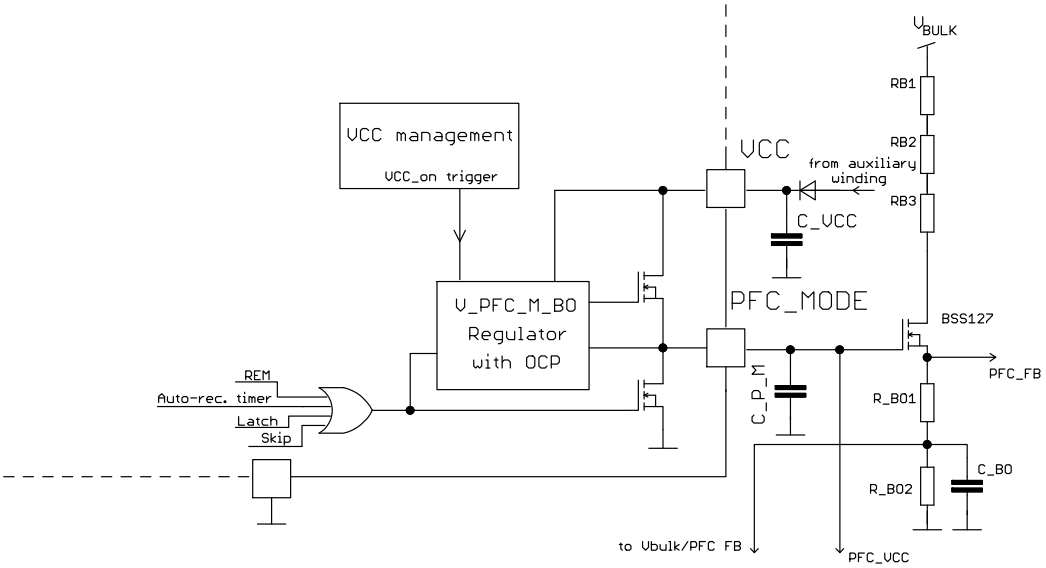


Figure 7. Internal Connection of the PFC MODE Block

There are two possible states of the PFC MODE output that can be placed by the controller based on the application operating conditions:

a) The PFC MODE output pin is pulled−down by an internal MOSFET switch before controller startup. This technique ensures minimum VCC pin current consumption in order to ramp V_{CC} voltage in a short time from the HV startup current source. This approach speeds up the startup and restart time of an SMPS. The PFC MODE output pin is also pulled−down in protection mode during which the HV startup current source is operated in DSS mode. Application power consumption is reduced in both above cases.

b) The pull−down switch is disabled and controller connects VCC pin voltage to PFC MODE output with minimum dropout ($V_{PFC\_M\_ON}$).

The PFC MODE pin output current is limited when the VCC to PFC MODE bypass switch is activated. The current limitation avoids bypass switch damage during PFC VCC decoupling capacitor charging process or short circuit. A minimum value PFC VCC decoupling capacitance should be used in order to speed up PFC stage startup after it is enabled by the NCP13992 controller.

Please refer to Figure 23 through Figure 25 for an illustration of NCP13992 PFC operation control.

ON−time Modulation and Feedback Loop Block

Frequency modulation of today's commercially available resonant mode controllers is based on the output voltage regulator feedback only. The feedback voltage (or current) of output regulator drives voltage (or current) controlled oscillator (VCO or CCO) in the controller. This method presents three main disadvantages:

1st – The 2nd order pole is present in small signal gain−phase characteristics => the lower cross over frequency and worse transient response is imposed by the system when voltage mode control is used. There is no direct link to the actual primary current – i.e. no line feed forward mechanism which results in poor line transient response.

2nd – Precise VCO (or CCO) is needed to assure frequency modulation with good reproducibility, f_{min} and f_{max} clamps need to be adjusted for each design => need for an adjustment pin(s).

3rd – Dedicated overload protection system, requiring an additional pin, is needed to assure application safety during overload and/or secondary short circuit events.

The NCP13992 resolves all disadvantages mentioned above by implementing a current mode control scheme that ensures best transient response performance and provides inherent cycle−by−cycle over−current protection feature in the same time. The current mode control principle used in this device can be seen in Figure 8.

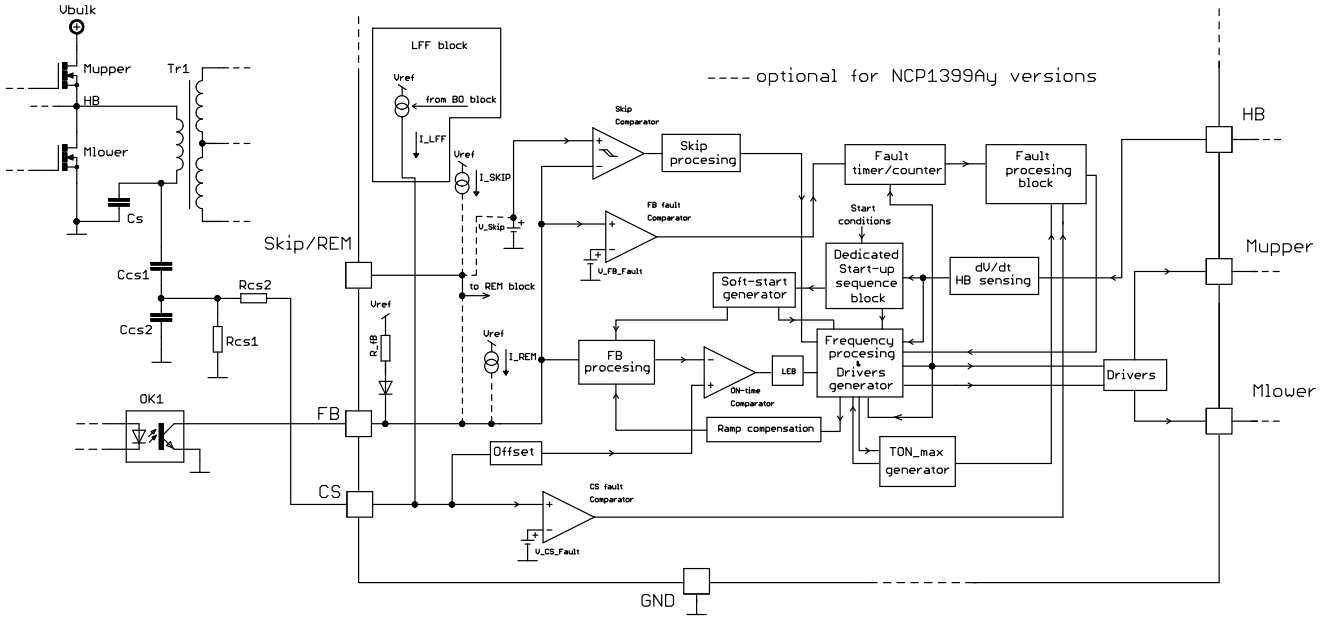


Figure 8. Internal Connection of the NCP13992 Current Mode Control Scheme

The basic principle of current mode control scheme implementation lies in the use of an ON−time comparator that defines upper switch on−time by comparing voltage ramp, derived from the current sense input voltage, to the divided feedback pin voltage. The upper switch on−time is then re−used for low side switch conduction period. The switching frequency is thus defined by the actual primary current and output load conditions. Digital processing with 10 ns minimum on−time resolution is implemented to ensure high noise immunity. The ON−time comparator output is blanked by the leading edge blanking (t_{LEB}) after the Mupper switch is turned−on. The ON−time comparator LEB period helps to avoid false triggering of the on−time modulation due to noise generated by the HB pin voltage transition.

The voltage signal for current sense input is prepared externally via natural primary current integration by the resonant tank capacitor Cs. The resonant capacitor voltage is divided down by capacitive divider (Ccs1, Ccs2, Rcs1, Rcs2) before it is provided to the CS input. The capacitive divider division ratio, which is fully externally adjustable, defines the maximum primary current level that is reached in case of maximum feedback voltage – i.e. the capacitive divider division ration defines the maximum output power of the converter for given bulk voltage. The CS is a bipolar input pin which an input voltage swing is restricted to ±5 V. A fixed voltage offset is internally added to the CS pin signal in order to assure enough voltage margin for operation the feedback optocoupler − the FB optocoupler saturation voltage is ~ 0.15 V (depending on type). However, the CS pin useful signal for frequency modulation swings from 0 V, so current mode regulation would not work under light load conditions if no offset would be added to the CS pin before it is stabilized to the level of the on−time comparator input. The CS pin signal is also used for secondary side short circuit detection – please refer to chapter dedicated to short circuit protection.

The second input signal for the on−time comparator is derived from the FB pin voltage. This internal FB pin signal is also used for the following purposes: skip mode operation detection, PFC MODE control and overload / open FB pin fault detection. The detailed description of these functions can be found in each dedicated chapters. The internal pull−up resistor assures that the FB pin voltage increases when the optocoupler LED becomes less biased – i.e. when output load is increased. The higher FB pin voltage implies a higher reference level for on−time comparator i.e. longer Mupper switch on−time and thus also higher output power. The FB pin features a precise voltage clamp which limits the internal FB signal during overload and startup. The FB pin signal passes through the FB processing block before it is brought to the ON−time comparator input. The FB processing block scales the FB signal down by a K_{FB} ratio in order to limit the CS input dynamic voltage range. The scaled FB signal is then further processed by subtraction of a ramp compensation generator signal in order to ensure stability of the current mode control scheme. The divided internal FB signal is overridden by a Soft−start generator output voltage during device starts−up.

The actual operating frequency of the converter is defined based on the CS pin and FB pin input signals. The maximum output power of the converter, under given input voltage, is limited by maximum internal FB voltage clamp that is reached when optocoupler provides no current. The maximum output power limit is bulk voltage dependent due to changing ratio between magnetizing and load primary current components. Line Feed Forward (LFF) system is implemented in the controller to compensate for maximum output power clamp variation. The I_{LFF} current that flows out from the Cs pin is BO/PFC FB pin voltage proportional

and creates voltage offset on the resistor connected to the Cs pin. The higher input voltage, the higher drop is created on external resistor. The Mupper switch on−time is thus reduced for given maximum internal FB voltage clamp when input voltage increases. The I_{LFF} current is provided only when BO pin voltage exceeds BO_OK threshold voltage.

Please refer to Figure 9 and below description for better understanding of the NCP13992 frequency modulation system.

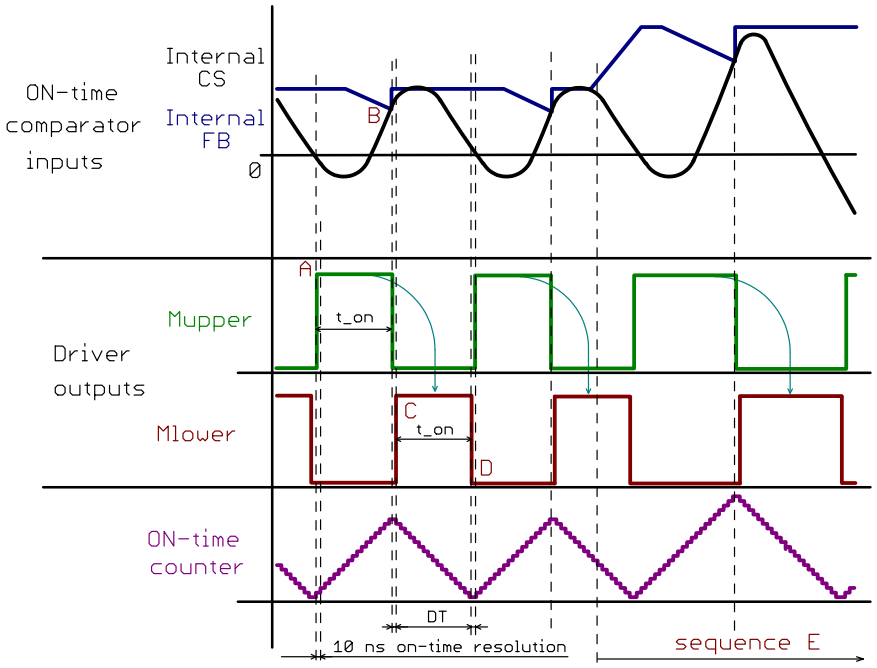


Figure 9. NCP13992 On−time Modulation Principle

The Mupper switch is activated by the controller after dead−time (DT) period lapses in point **A**. The frequency processing block increments the ON−time counter with 10 ns resolution until the internal CS signal crosses the internal FB set point for the ON−time comparator in point **B**. A DT period is then introduced by the controller to avoid any shoot−through current through the power stage switches. The DT period ends in point **C** and the controller activates the Mlower switch. The ON−time processing block decrements the ON_time counter down until it reaches zero. The Mlower switch is then turned−OFF at point **D** and the DT period is started. This approach results in perfect duty cycle symmetry for Mlower and Mupper switches. The Mupper switch on−time naturally increases and the operating frequency drops when the FB pin voltage is increased, i.e. when higher current is delivered by the converter output – sequence **E**.

The resonant capacitor voltage and thus also CS pin voltage can be out of balance in some cases – this is the case during transition from full load to no−load operation when skip mode is not used or adjusted correctly. The current mode operation is not possible in such case because the ON−time comparator output stays active for several switching cycles. Thus a special logic has been implemented in NCP13992 in order to repeat the last valid on−time until the current mode operation recovers – i.e. until the CS pin signal balance is restored by the system.

Overload and Open FB Protections

The overload protection and open FB pin detection are implemented via FB pin voltage monitoring in this controller. The FB fault comparator is triggered once the FB pin voltage reaches its maximum level and the V_{FB_FAULT} threshold is exceeded. The fault timer or counter (depending on IC option) is then enabled – refer to Figure 10. The time period to the FB fault event confirmation is defined by the preselected $t_{FB\_FAULT\_TIMER}$ parameter when the fault timer option is used. The FB fault counter, once selected as a FB fault confirmation period source, defines the fault confirmation period via Mupper DRV pulses counting. The FB fault confirmation time is thus dependent on switching frequency. The fault timer/counter is reset once the FB fault condition diminishes. A digital noise filter has been added after the FB fault comparator to overcome false triggering of the FB fault timer/counter due to possible noise on the FB input. The noise filter has a period of 2 μs for FB fault timer/counter activation and 20 μs for reset/deactivation to assure high noise immunity. A cumulative timer/counter IC option is also available on request. The FB fault timer/counter is not reset when the FB fault condition diminishes in this case. The FB fault timer/counter is disabled and memorizes the fault period information. The cumulative FB fault timer/counter integrates all the FB fault events over the IC operation time. The Fault timer/counter can be reset via skip mode or VCC UVLO event.

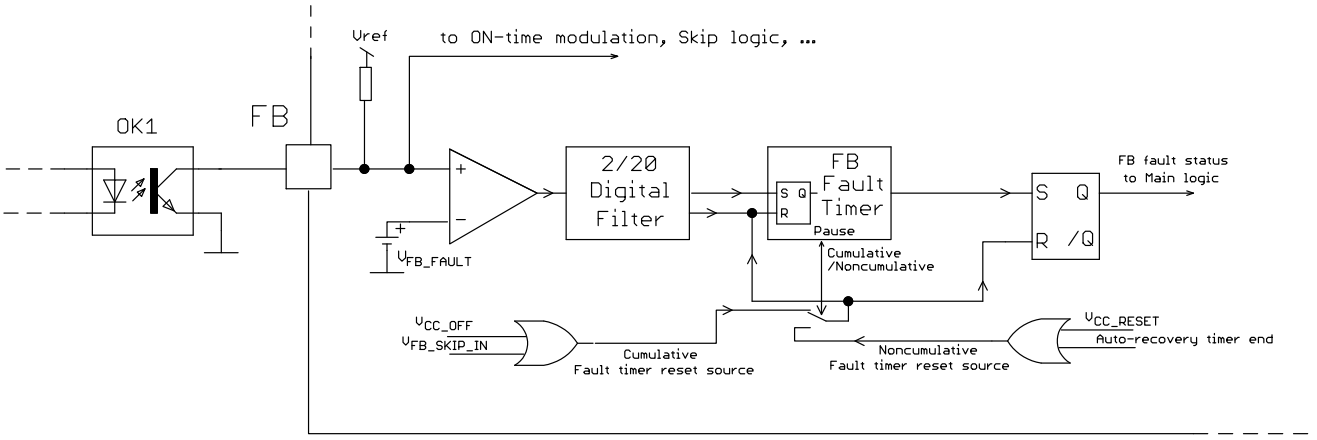


Figure 10. Internal FB Fault Management

The controller disables driver pulses and enters protection mode once the FB fault event is confirmed by the FB fault timer or counter. Latched or auto−recovery operation is then triggered – depends on selected IC option. The controller adds an auto−recovery off−time period (t_{A-REC_TIMER}) and restarts the operation via soft start in case of auto−recovery option. The application temperature runaway is thus avoided in case of overload while the automatic restart is still possible once the overload condition disappears. The IC with latched FB fault option stays latched−off, supplied by the HV startup current source working in DSS mode, until the V_{CC_RESET} threshold is reached on the VCC pin – i.e. until user re−connects power supply mains.

Please refer to Figure 23 and Figure 24 for an illustration of the NCP13992 FB fault detection block.

Secondary Short Circuit Detection

The protection system described previously, implemented via FB pin voltage level detection, prevents continuous overload operation and/or open FB pin conditions. The primary current is naturally limited by the NCP13992 on−time modulation principle in this case. But the primary current increases when the output terminals are shorted. The NCP13992 controller will maintain zero voltage switching operation in such case, however high currents will flow through the power MOSFETS, transformer winding and secondary side rectification. The NCP13992 implements a dedicated secondary side short circuit protection system that will shut down the controller much faster than the regular FB fault event in order to limit the stress of the power stage components. The CS pin signal is monitored by the dedicated CS fault comparator − refer to Figure 8. The CS fault counter is incremented each time the CS fault comparator is triggered. The controller enters auto−recovery or latched protection mode (depending on IC option) in case the CS fault counter overflows refer to Figure 11. The CS fault counter is then reset once the CS fault comparator is inactive for at least 50 Mupper upcoming pulses. This digital filtering improves CS fault protection system noise immunity.

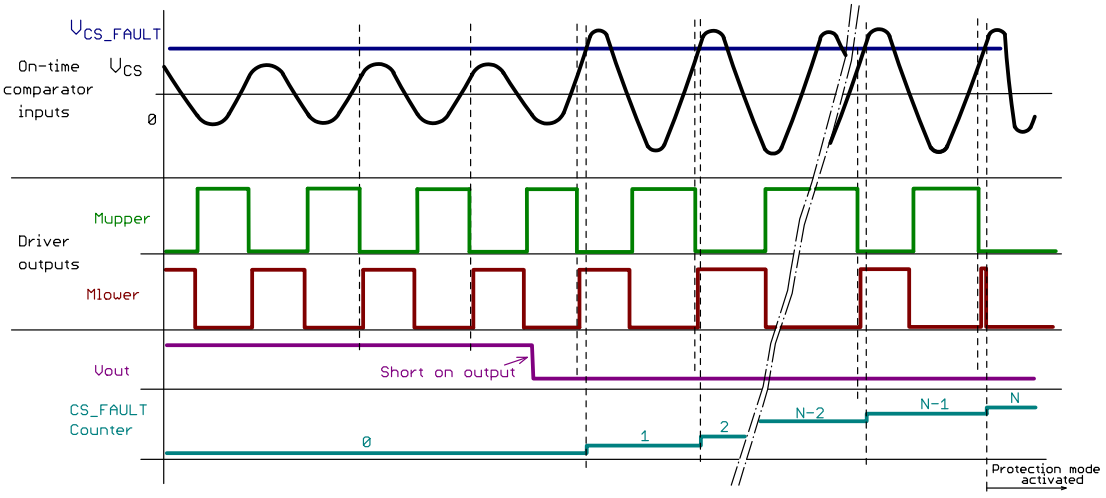


Figure 11. NCP13992 CS Fault Principle

Dedicated Startup Sequence and Soft−Start

Hard switching conditions can occur in a resonant SMPS application when the resonant tank operation is started with 50% duty cycle symmetry – refer to Figure 12. This hard switching appears because the resonant tank initial conditions are not optimal for the clean startup.

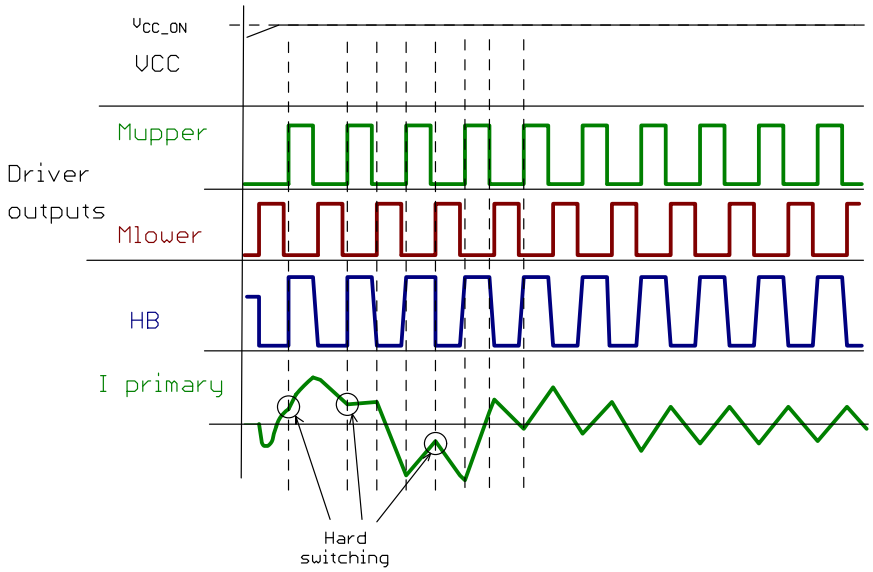


Figure 12. Hard Switching Cycle Appears in the LLC Application when Resonant Tank is Excited by 50% Duty Cycle during Startup

The initial resonant capacitor voltage level can differ depending on how long delay was placed before application operation restart. The resonant capacitor voltage is close to zero level when application restarts after very long delay – for example several seconds, when the resonant capacitor is discharged by leakage to the power stage. However, the resonant capacitor voltage value can be anywhere between Vbulk and 0 V when the application restarts operation after a short period of time – like during periodical SMPS turn−on/off. Another factor that plays significant role during resonant power supply startup is the actual load impedance seen by the power stage during the first pulses of startup sequence. This impedance is not only defined by resonant tank components but also by the output loading conditions and actual output voltage level. The load impedance of resonant tank is low when the output is loaded and/or the output voltage is low enough to made secondary rectifies conducting during first switching cycles of startup phase. The resonant frequency of the resonant tank is given by the resonant capacitor capacitance and resonant inductance −note that the magnetizing inductance does not participate in resonance in this case. However, if the application starts−up when the output capacitors is charged and there is no load connected to the output, the secondary rectification diodes is not conducting during each switching cycle of startup sequence and thus the resonant frequency of resonant tank is affected also by the magnetizing inductance. In this case, the resonant frequency is much lower than in case of startup into loaded/discharged output.

These facts show that a clean, hard switching free and parasitic oscillation free, startup of an LLC converter is not an easy task, and cannot be achieved by duty cycle imbalance and/or simple resonant capacitor pre−charge to Vbulk/2 level. These methods only work in specific startup conditions.

This explains why the NCP13992 implements a proprietary startup sequence − see Figure 13 and Figure 14. The resonant capacitor is discharged down to 0 V before any application restart − except when restarting from skip mode.

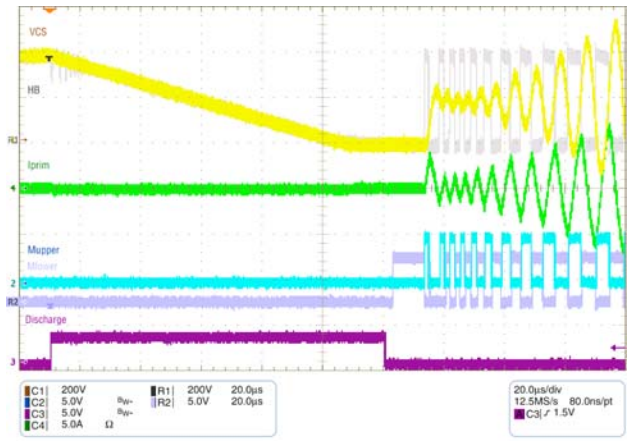


Figure 13. Initial Resonant Capacitor Discharge before Dedicated Startup Sequence is Placed

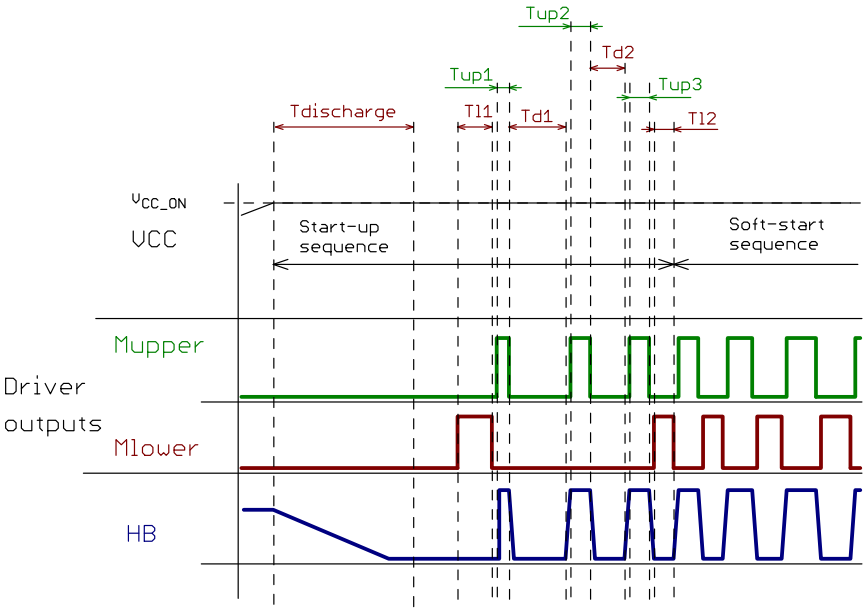


Figure 14. Dedicated Startup Sequence Detail

The resonant capacitor discharging process is simply implemented by activating an internal current limited switch connected between the HB pin and IC ground – refer to Figure 13. This technique assures that the resonant capacitor energy is dissipated in the controller without ringing or oscillations that could swing the resonant capacitor voltage to a positive or negative level. The controller detects that the discharge process is complete via HB pin voltage level monitoring. The discharge switch is disabled once the HB pin voltage drops below the V_{HB_MIN} threshold.

The dedicated startup sequence continues by activation of the Mlower driver output for Tl1 period (refer to Figure 14). This technique ensures that the bootstrap capacitor is fully charged before the first high−side driver pulse is introduced by the controller. The first Mupper switch on−time Tup1 period is fixed and depends on the application parameters. This period can be adjusted internally – various IC options are available. The Mupper switch is released after T_{up1} period and it is not followed by the Mlower switch activation. The controller waits for a new ZVS condition for Mupper switch instead and measures actual resonant tank conditions this way. The Mupper switch is then activated again after the Mlower blank period is used for measurement purposes. The second Mupper driver conduction period is then dependent on the previously measured conditions:

1. The Mupper switch is activated for 3/2 of previous Mupper conduction period in case the measured time between previous Mupper turn−off event and upper ZVS condition detection is twice higher than the the previous Mupper pulse conduction period
2. The Mupper switch is activated for previous Mupper conduction period in case the measured time between previous Mupper turn−off event and upper ZVS condition detection is twice lower than the previous Mupper pulse conduction period

The startup period then depends on the previous condition. Another blank Mlower switch period is placed by the controller in case condition a) occurred. A normal Mlower driver pulse, with DC of 50% to previous Mupper DRV pulse, is placed in case condition b) is fulfilled.

The dedicated startup sequence is placed after the resonant capacitor is discharged (refer to Figure 13 and Figure 14) in order to exclude any hard switching cycles during the startup sequence. The first Mupper switch cycle in startup phase is always non−ZVS cycle because there is no energy in the resonant tank to prepare ZVS condition. However, there is no energy in the resonant tank at this time, there is also no possibility that the power stage MOSFET body diodes conducts any current. Thus the hard commutation of the body diode cannot occur in this case.

The IC will not start and provide regular driver output pulses until it is placed into the target application, because the startup sequence cannot be finished until HB pin signal is detected by the system. The IC features a startup watchdog timer ($t_{WATCHDOG}$) which activates a dedicated startup sequence periodically in case the IC is powered without application (during bench testing) or in case the startup sequence is not finished correctly. The IC will provide the first Mlower and first Mupper DRV pulses with a $t_{WATCHDOG}$ off−time in−between startup attempts.

Soft−start

The dedicated startup sequence is complete when condition b) from previous chapter is fulfilled and the controller continues operation with the soft−start sequence. A fully digital non−linear soft−start sequence has been implemented in NCP13992 using a soft−start counter and D/A converter that are gradually incremented by the Mlower driver pulses. A block diagram of the NCP13992 soft−start system is shown in Figure 15.

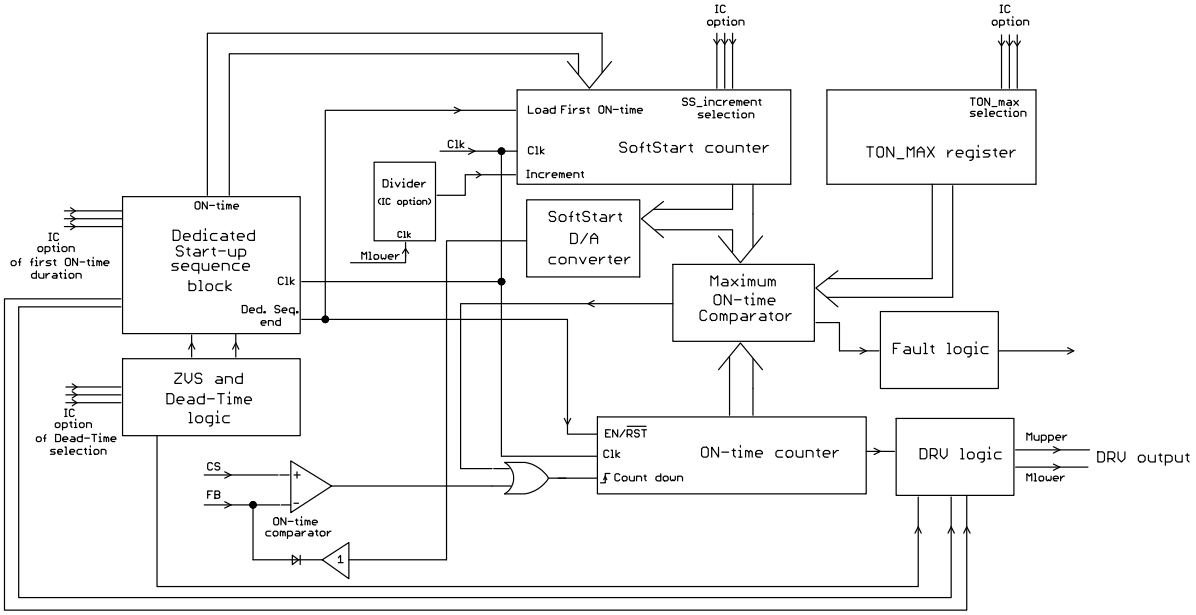


Figure 15. Soft−start Block Internal Implementation

The soft−start block subsystems and operation are described below:

1. The **Soft−Start counter** is a unidirectional counter that is loaded with the last Mupper on−time value that is reached at the dedicated startup sequence end (i.e. during condition b occurrence explained in previous chapter). The on−time period used in the initial period of the soft−start sequence is affected by the first Mupper on−time period selection and the dedicated startup sequence processing. The Soft−Start counter counts up from this initial on time period to its maximum value which corresponds to the IC maximum on−time. The Soft−Start counter is incremented by the soft−start increment number ($t_{SS\_INCREMENT}$) during each Mlower switch on−time period. The soft−start start increment, selectable via IC option, thus affects the soft−start time duration. The Mlower clock signal for the Soft−Start counter can be divided down by the SS clock divider ($K_{SS\_INCREMENT}$) in case the soft−start period needs to be prolonged further – this can be also done via IC option selection. The Soft−Start period is terminated (i.e. the counter is loaded to its maximum) when the FB pin voltage drops below $V_{FB\_SKIP\_IN}$ level.

2. The **ON−time counter** is a bidirectional counter that is used as a main system counter for on−time modulation during soft−start, normal operation or overload conditions. The ON−time counter counts−up during Mupper switch conduction period and then counts down to zero – defining Mlower switch conduction period. This technique assures perfect 50% duty cycle symmetry for both power switches as afore mentioned. The ON−time counter count−up mode can be switched to the count−down mode by either of two events: **1st** when the ON−time counter value reaches the maximum on−time value (t_{TON_MAX}) or **2nd** when the actual Mupper on−time is terminated based on the current sense input information.

4. The **Maximum ON−time comparator** compares the actual ON−time counter value with the maximum on−time value (t_{TON_MAX}) and activates the latch (or auto−recovery) protection mode once IC detect requested number of TON_MAX events. The minimum operating frequency of the controller is defined the same way. The Maximum ON−time comparator reference is loaded by the Soft−Start counter value on each switching cycle during soft−start. The Maximum ON−time fault signal is ignored during Soft−Start operation. The converter Mupper switch on−time (and thus operating frequency) is thus defined by the Soft−Start counter value indirectly – via Maximum ON−time comparator. The Mupper switch on−time is increased until the Soft−Start counter reaches t_{TON_MAX} period and Maximum on−time protection is activated, or until ON−time comparator takes action and overrides the Maximum ON−time comparator.

5. The **Soft−Start D/A converter** generates a soft−start voltage ramp for ON−time comparator input synchronously with Soft−Start counter incrementing. The internal FB signal for ON−time comparator input is artificially pulled−down and then ramped−up gradually when soft−start period is placed by the system – refer to Figure 16. The FB loop is supposed to take over at certain point when regulation loop is closed and output gets regulated so that soft−start has no other effect on the on−time modulation. The Soft−Start counter continues counting−up until it reaches its maximum value which corresponds to the IC maximum on−time value – i.e. the IC minimum operating frequency. The Soft−Start period is terminated (i.e. counter is loaded to its maximum) when the FB pin voltage drops below $V_{FB\_SKIP\_IN}$ level. The D/A converter output evolve accordingly to the Soft−Start counter as it is loaded from its output data bus.

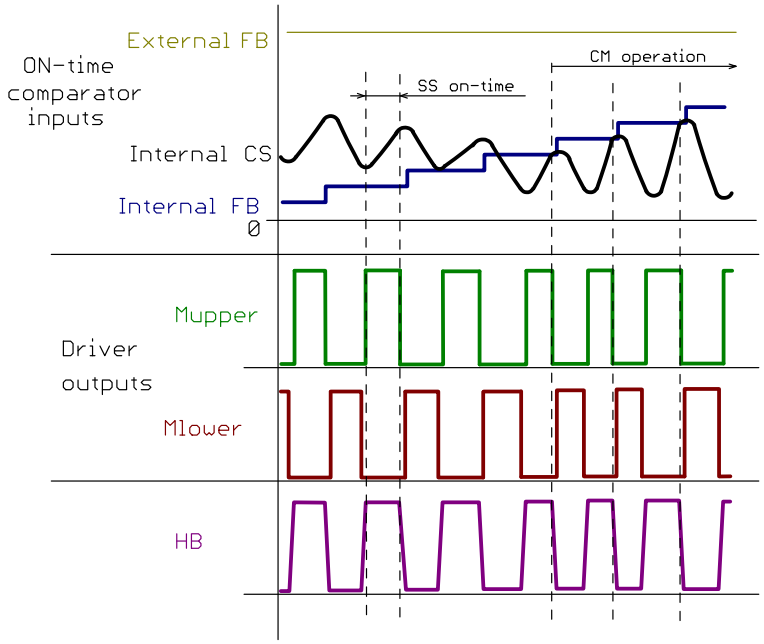


Figure 16. Soft Start Behavior

The Controller Operation during Soft−start Sequence Evolves as Follows:

The Soft−Start counter is loaded by last Mupper on−time value at the end of the dedicated startup sequence. The ON−time counter is released and starts count−up from zero until the value that is equal to the actual Soft−Start counter state. The Mupper switch is active during the time when ON−time counter counts−up. The Maximum ON−time comparator then changes counting mode of the ON−time comparator from count−up to count−down. A dead−time is placed and the Mlower switch is activated till the ON−time counter reaches zero value. The Soft−Start counter is incremented by selected increment during corresponding Mlower on−time period so that the following Mupper switch on−time is prolonged automatically – the frequency thus drops naturally. Because the operating frequency of the controller drops and Mlower DRV signal is used as a clock source for the Soft−start counter, the soft−start speed starts to decrease on each (or on each N−th) Mlower driver pulse (where N is defined by $K_{SS\_INCREMENT}$) of switching cycle. So we have non−linear soft−start that helps to speed up output charging in the beginning of the soft−start operation and reduces the output voltage slope when the output is close to the regulation level. The output bus of the Soft−Start counter addresses the D/A converter that defines the ON−time comparator reference voltage. This reference voltage thus also increases non−linearly from initial zero level until the level at which the current mode regulation starts to work. The on−time of the Mupper and Mlower switch is then defined by the ON−time comparator action instead of the Maximum ON−time comparator. The soft−start then continues until the regulation loop is closed and the on−time is fully controlled by the secondary regulator. The Soft−Start counter then continues in counting and saturates at its maximum possible value which corresponds to IC minimum operating frequency. The maximum on−time fault detection system is enabled when Soft−Start counter value is equal to t_{TON_MAX} value.

The previous on−time repetition feature, described above in the ON−time modulation and feedback loop chapter, is disabled in the beginning of soft start period. This is because the ON−time comparator output stays high for several cycles of soft start period – until the current mode regulation takes over. The previous on−time repetition feature is enabled once the current modulation starts to work fully, i.e. in the time when the ON−time comparator output periodically drops to low state within actual Mupper switch on−time period. Typical startup waveform of the LLC application driven by NCP13992 controller can be seen in Figure 17.

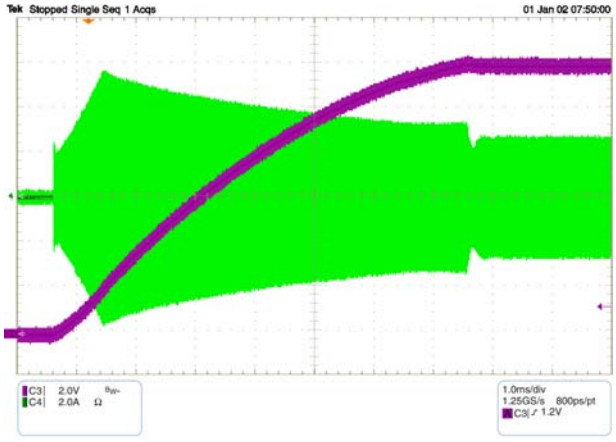


Figure 17. Application Startup with NCP13992 − Primary Current − Green, V_{out} − Magenta

Skip Mode Operation

Then NCP13992 implements proprietary light load and quiet skip mode operating techniques that improve light load efficiency, reduce no−load power consumption and significantly reduce acoustic noise. Controller uses 50% duty cycle symmetry under full and medium load conditions. Normal current mode frequency modulation takes place during this operating mode – refer to on−time processing section of this datasheet. The 50% duty cycle symmetry operating mode is replaced by continues operation with minimum switching patterns repeated after controlled amount of off−time when load is decreased below preselected level. Zero voltage switching technique is still present for the power switches to achieve high light load efficiency. Quiet skip mode operation is initiated when load drops further and FB voltage drops below another FB threshold that is user adjustable on the skip pin. The frequency of skip burst is regulated by internal digital controller around preselected quiet skip frequency clamp in order to reduce acoustic noise. The skip frequency then drops to very low values during no−load conditions. Refer to Figure 18, Figure 19 and Figure 20 for typical application waveforms during light load and quiet skip mode operating modes.

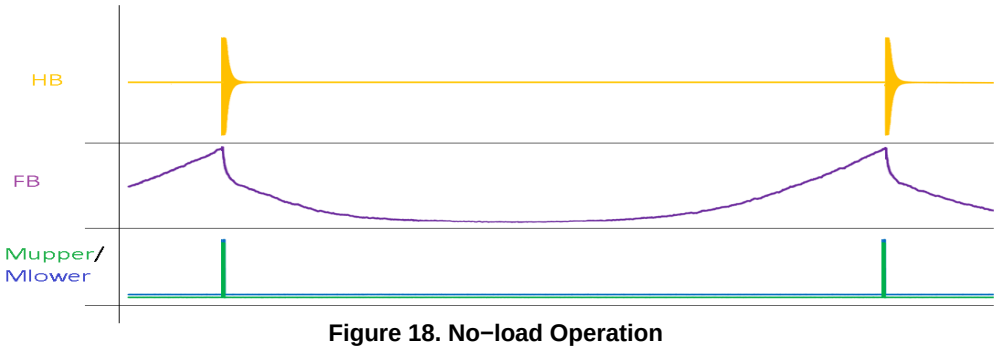


Figure 18. No−load Operation

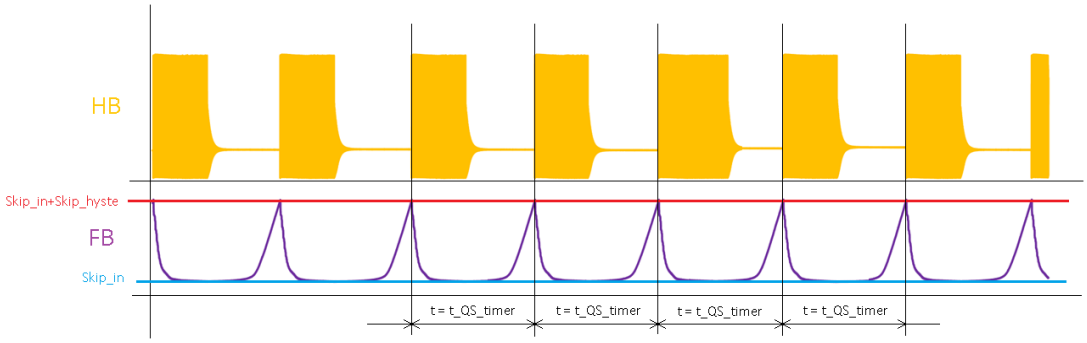


Figure 19. Quiet Skip Mode Operation

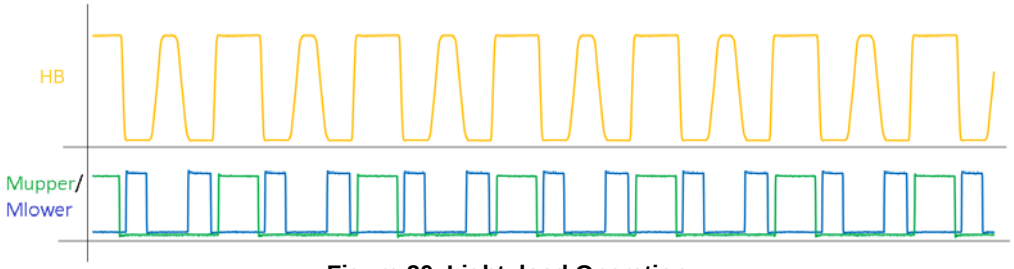


Figure 20. Light−load Operation

The High Voltage Half−bridge Driver

The driver features a traditional bootstrap circuitry, requiring an external high voltage diode with resistor in series for the capacitor refueling path. Minimum series resistor Rboot value is 3.3 Ω. Figure 21 shows the internal architecture of the drivers section. The device incorporates an upper UVLO circuitry that makes sure enough V_{GS} is available for the upper side MOSFET.

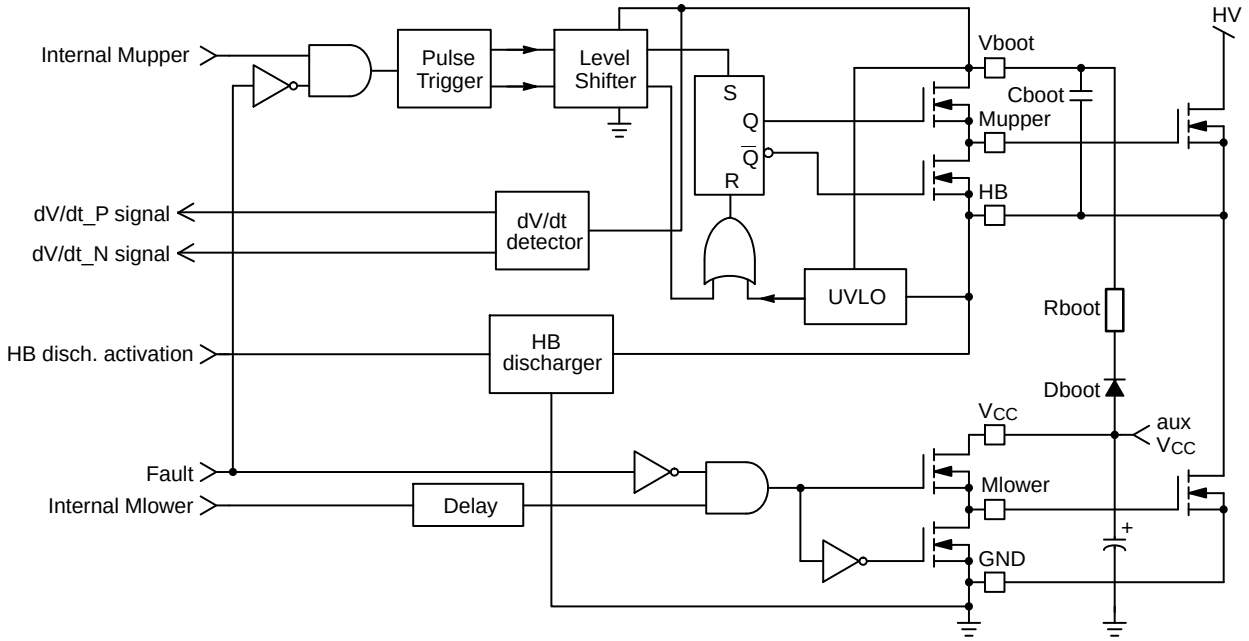


Figure 21. The NCP13992 Internal DRVs Structure

The internal dV/dt sensor, connected to the VBOOT pin, detects the HB pin voltage transitions in order to setup the optimum DT period – please refer to Dead−Time chapter. The internal HV discharge switch is connected to the HB pin and discharges resonant capacitor before application startup. The current through the switch is regulated to $I_{DISCHARGE}$ level until the V_{HB_MIN} threshold voltage is reached on the HB pin. The discharge system assures always the same startup conditions for application – regardless of previous operating state.

As stated in the maximum ratings section, the floating portion can go up to 620 VDC on the BOOT pin. This voltage range makes the IC perfectly suitable for offline applications featuring a 400 V PFC front stage.

Automatic Dead−time Adjust

The dead−time period between the Mupper and Mlower drivers is always needed in half bridge topologies to prevent any cross conduction through the power stage MOSFETs that would result in excessive current, high EMI noise generation or total destruction of the application. Fixed dead−time period is often used in the resonant converters because this approach is simple to implement. However, this method does not ensure optimum operating conditions in resonant topologies because the magnetizing current is changing with line and load conditions. The optimum dead−time, under a given operating conditions, is equal to the time that is needed for bridge voltage to transition between upper and lower states and vice versa – refer to Figure 22.

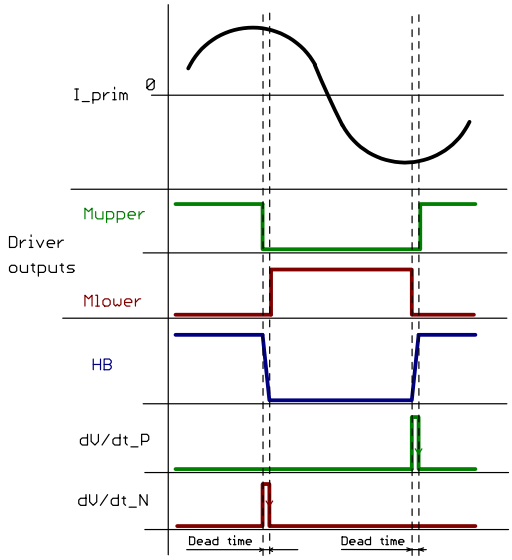


Figure 22. Optimum Dead−time Period Adjust

The MOSFET body diode conduction time is minimized when optimum dead−time period is used which results in maximum efficiency of a resonant converter power stage. There are several methods to determine the optimum dead−time period or to approximate it (for example using auxiliary winding on main transformer or modulating dead−time period with operating frequency of the converter). These approaches however require a dedicated pin for nominal dead−time adjust or auxiliary winding

voltage sensing. The NCP13992 uses a dedicated method that senses the VBOOT pin voltage internally and adjusts the optimum dead−time period with respect to the actual operating conditions of the converter. The high−voltage dV/dt detector, connected to the VBOOT pin, delivers two internal digital signals that are indicating Mupper to Mlower and Mlower to Mupper transitions that occur on the HB and VBOOT pins after the corresponding MOSFET switch is turned−off. The controller enables the opposite MOSFET in the power stage once the corresponding dV/dt sensor output provides information about HB (or VBOOT) pin transition ends.

The ZVS transition on the bridge pin (HB) could take a longer time or even does not finish in some cases – for example with extremely low bulk voltage or when some critical failure occurs. This situation should not occur normally in correctly designed application because several other protections would prevent such a situation. The NCP13992 implements maximum DT period clamp that limits driver's off−time period to the $t_{DEAD\_TIME\_MAX}$ value. The corresponding MOSFET driver is forced to turn−on by the internal logic regardless of missing dV/dt sensor signal. This situation does not occur during normal operation and will be considered a fault state by the device. There are several possibilities on how the controller continues operation after this event occurrence – depending on the IC option:

1. The opposite MOSFET switch is forced to turn−on when $t_{DEAD\_TIME\_MAX}$ period elapses and no fault is generated
2. The controller is latched−off in case the ZSV condition is not detected within selected $t_{DEAD\_TIME\_MAX}$ period
3. The controller stops operation and restarts operation after auto−recovery period in case the ZSV condition has not been detected within the selected $t_{DEAD\_TIME\_MAX}$ period

A DT fault counter option is available. Selected number (N_{DT_MAX}) or DT fault events have to occur in order to confirm DT fault in this case.

A fixed DT option is also available for this device. The internal dV/dt sensor signal is not used for this device option and the $t_{DEAD\_TIME\_MAX}$ period is used as a regular DT period instead. The DT fault detection is disabled in this case.

Temperature Shutdown

The NCP13992 includes a temperature shutdown protection. The typical TSD hysteresis is 30°C. When the temperature rises above the upper threshold, the controller stops switching instantaneously, and goes into the off−mode with extremely low power consumption. The V_{CC} supply is maintained (by operating the HV start−up in DSS mode) in order to memorize the TSD event information. When the temperature falls below the lower threshold, the full restart (including soft−start) is initiated by the controller. The HV startup current source features an independent over−temperature protection which limits its output current in case the DIE temperature exceeds TSD to avoid damage to the HV startup silicon structure.

APPLICATION INFORMATION

Controller Operation Sequencing of NCP13992 LLC Controller

The paragraphs below describe controller operation sequencing under several typical cases as well as transitions between them.

1. Application start, Brown−out off and restart, OVP/OTP latch and then restart – Figure 23

Application is connected to the mains at point **A** thus the HV input of the controller becomes biased. The HV startup current source starts charged VCC capacitor until V_{CC} reaches V_{CC_ON} threshold.

The VCC pin voltage reached V_{CC_ON} threshold in point **B**. The BO, FB, OVP/OTP and PFC MODE blocks are enabled. The VBULK/PFC FB pin starts to receive divided bulk voltage as the external HV switch is activated by PFC MODE output. The V_{CC} blank is activated during each V_{CC_ON} event to ensure that the internal logic ignores all fault inputs until the internal blocks are fully biased and stabilized after a V_{CC_ON} event. The IC DRVs were not enabled after first V_{CC} blank period in this case as the voltage on VBULK/PFC FB is below V_{BO} level. The IC keeps all internal blocks biased and operates in the DSS (Dynamic Self−Supply) mode as long as the fault conditions is still present.

The BO_OK condition is received (voltage on VBULK/PFC FB reach V_{BO} level) at point **C**. The IC activates the startup current source to refill VCC capacitor in order to assure sufficient energy for a new startup. The VCC capacitor voltage reaches V_{CC_ON} level again and the VCC blank period is started. The DRVs are enabled and the application is started after V_{CC} blank period lapses because there is no faults condition at that time.

Line and also bulk voltage drops at point **D** so the BO_OK signal become low (voltage on VBULK/PFC FB drops below V_{BO} level). The LLC DRVs are disabled as well as OVP/OTP block bias. The PFC MODE output stay high to keep the bulk voltage divider connected, so the BO block still monitors the bulk voltage. The controller activates the HV startup current source into DSS mode to keep enough VCC voltage for operation of all blocks that are active while the IC is waiting for BO_OK condition.

The line voltage and thus also bulk voltage increase at point **E** so the Brown−out block provide the BO_OK signal once the V_{BO} level is reached. The startup current source is activated after BO_OK signal is received to charge the VCC capacitor for a new restart.

The V_{CC_ON} level is reached in point **F**. The OVP/OTP block is biased and the VCC blank period is started at the same time. The controller restores operation via the regular startup sequence and soft−start after VCC blank period lapses since there is no fault condition detected.

The application then operates normally until the OVP/OTP input is pulled−up at point **G**. The controller then enters latch−off mode in which all blocks are disabled except for the feedback block. The VCC management controls the HV startup in DSS mode in order to keep enough VCC level to hold the latch−up state memorized while the application remains plugged−in to the mains.

The power supply is removed from the mains at point **H** and the VCC voltage drops down below V_{CC_RESET} level thus the low voltage controller is released from latch. A new application start occurs when the user plugs the application the mains again.

2. Application start, Brown−out off and restart, output short fault with auto−recovery restart – Figure 24

Operating waveforms descriptions for this figure is similar to one for Figure 23 from point **A** till point **G** – with one difference. The skip mode operation (FB < $V_{FB\_SKIP\_IN}$) blocks the IC startup after first V_{CC_ON} event instead of BO_fault.

The LLC converter operation is stopped in point **G** because the controller detects an overload condition (short circuit event in this case as the Vout drops abruptly). The controller disables all blocks except for the FB block and the fault logic. The HV startup DSS operation is initiated in order to keep enough VCC level for all internal blocks that need to be biased. Internal auto−recovery timer counts down the recovery delay period t_{A-REC_TIMER}.

The auto−recovery restart delay period lapses at point **H**. The HV startup current source is activated to recharge VCC capacitor before a new restart.

The V_{CC_ON} threshold is reached in point **I** and all the internal blocks are biased. The V_{CC} blank and OVP/OTP blank period are started at the same time. The LLC converter operation is enabled, including a dedicated startup and soft−start period. The output short circuit is removed in between thus the Vout ramped−up and the FB loop took over during the LLC converter soft−start period.

3. Startup, skip−mode operation, low line detection and restart into skip−mode – Figure 25

The application is plugged into the mains at point **A** thus the HV input of the controller becomes biased. The HV startup current source starts charging the VCC capacitor until V_{CC} reaches the V_{CC_ON} threshold.

The VCC pin voltage reaches the V_{CC_ON} threshold at point **B**. The BO, FB, OVP/OTP and PFC MODE blocks are enabled. The VBULK/PFC FB pin begins to receive divided bulk voltage as the external HV switch is activated by the PFC MODE output. The V_{CC} blank period is activated during each V_{CC_ON} events. This blank ensures that the internal logic ignores all fault inputs until the internal blocks are fully biased and stabilized after V_{CC_ON} event. The IC DRVs are not enabled even after V_{CC} blank period ends because the OVP fault condition is present. The OVP fault condition disappears after some time so the HV startup current source is enabled to prepare enough V_{CC} for a new startup attempt. The new V_{CC} blank and OTP blank periods

are placed after the V_{CC_ON} event is detected. The controller authorizes DRVs at point **C** as there are no faults conditions present after the V_{CC} blank period elapses. The load current is reduced thus the FB loop reduces the primary controller FB pin voltage.

The load diminished further and the FB skip threshold is reached in point **D**. The controller turns−off all the blocks that are not essential for the controller operation during skip−mode – i.e. all blocks except FB block and VCC management. This technique is used to minimize the device consumption when there are no driver pulses during skip−mode operation. The output voltage then drops naturally and the FB loop reflects this change into the primary FB pin voltage that increases accordingly. The auxiliary winding is refilling VCC capacitor during each skip burst thus the controller is supplied from the application during the skip mode operation.

The controller FB skip−out threshold is reached in point **E;** the controller enables all blocks and LLC DRVs to refill the output capacitor. The controller did not activate the HV startup current source because there is enough voltage present on the VCC pin during skip mode. The OTP blank periods is activated at the beginning of the skip burst to mask possible OTP faults.

Note: The VCC capacitor needs to be chosen with a value high enough to ensure that V_{CC} will not drop below the V_{CC_OFF} level during skip mode. The device would enters into off−mode.

The line voltage drops in point **F,** but the bulk voltage is dropping slowly as there is nearly no consumption from the bulk capacitor during skip mode – only some refilling bursts are provided by the controller. The application thus continues in skip mode operation for several skip burst cycles.

The bulk voltage level less than V_{BO} threshold is detected by the controller in point **G** during one of the skip burst pulses. The controller thus disabled DRVs and enters DSS mode of operation in which the OVP/OTP block is disabled and the controller is waiting for BO_OK event. The PFC MODE provides the $V_{PFC\_M\_ON}$ voltage in this case to allow the PFC stage to refill bulk capacitors.

The line voltage is increased at point **H** thus the controller receives the BO_OK signal. The BO_OK signal is received during the period in which the HV startup current source is active and refills the VCC capacitor.

This V_{CC_ON} threshold is reached by the VCC pin at point **I**. The V_{CC} blank period and OVP/OTP blank period are started at the same time. The full startup sequence is enabled at the end of the V_{CC} blank period as no fault is detected. The application then enters skip mode again as the load current is low.

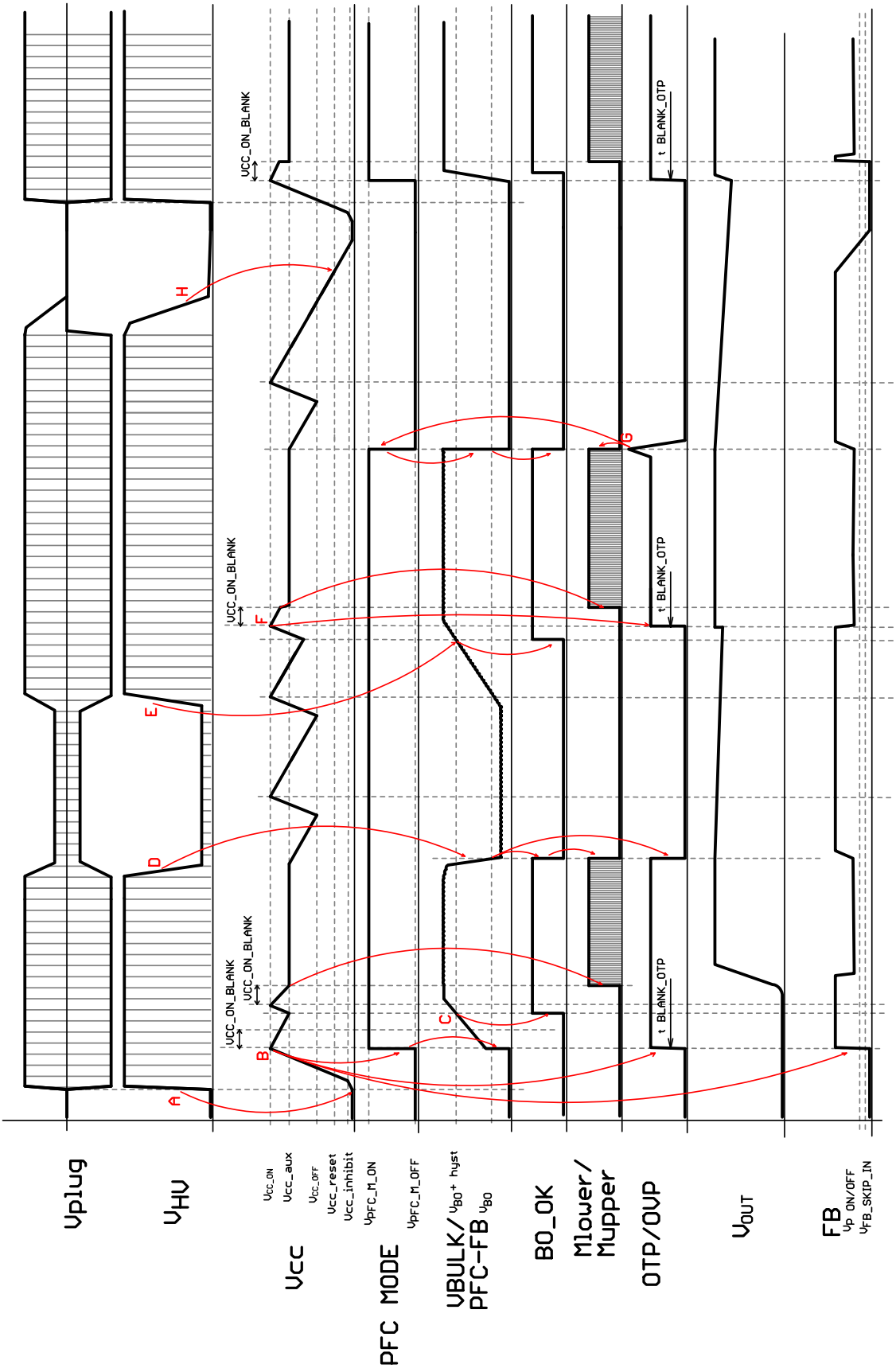


Figure 23. Application Start, Brown−out Off and Restart, OVP/OTP Latch and then Restart

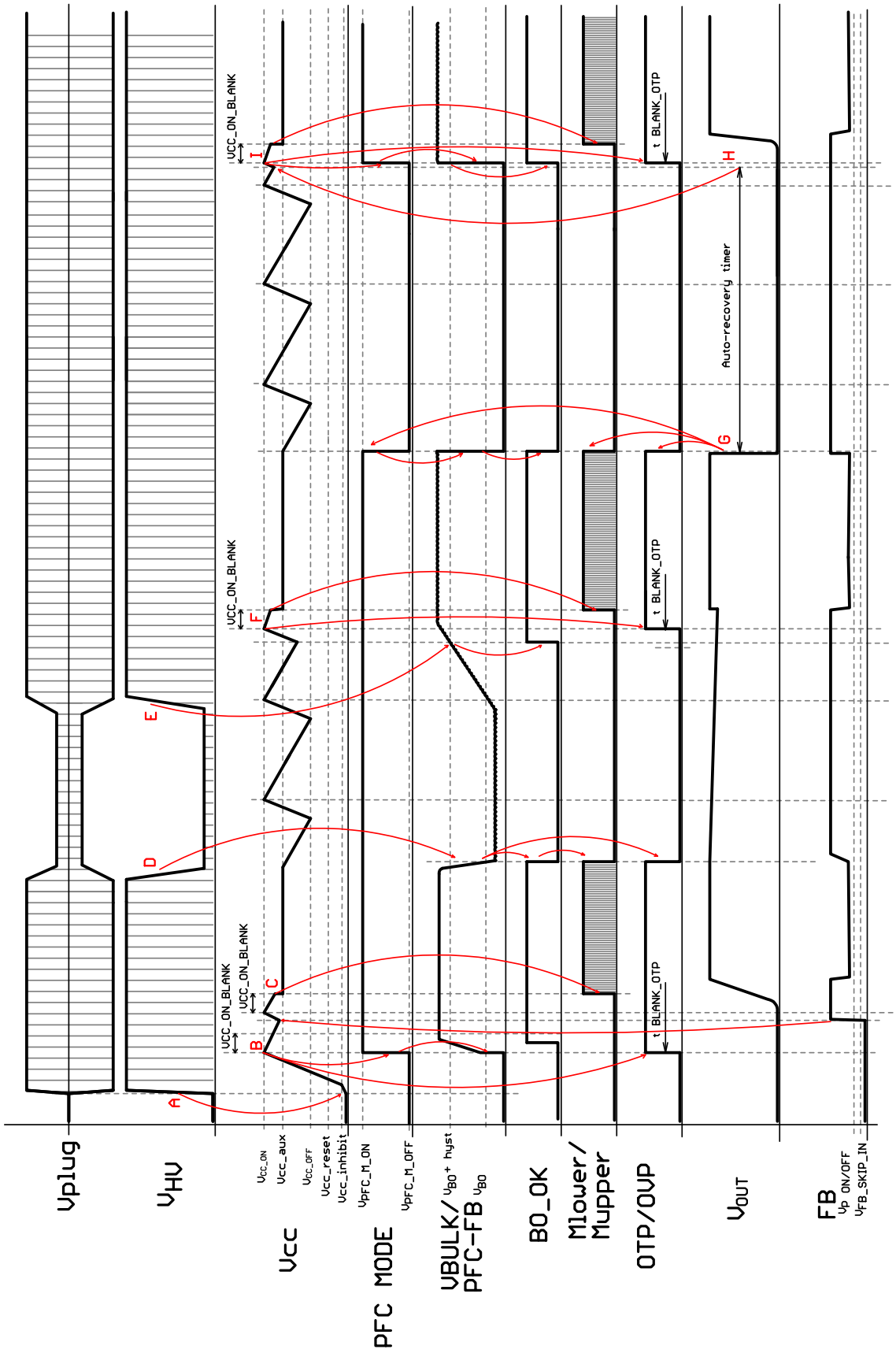


Figure 24. Application Start, Brown−out Off and Restart, Output Short Fault with Auto−recovery Restart

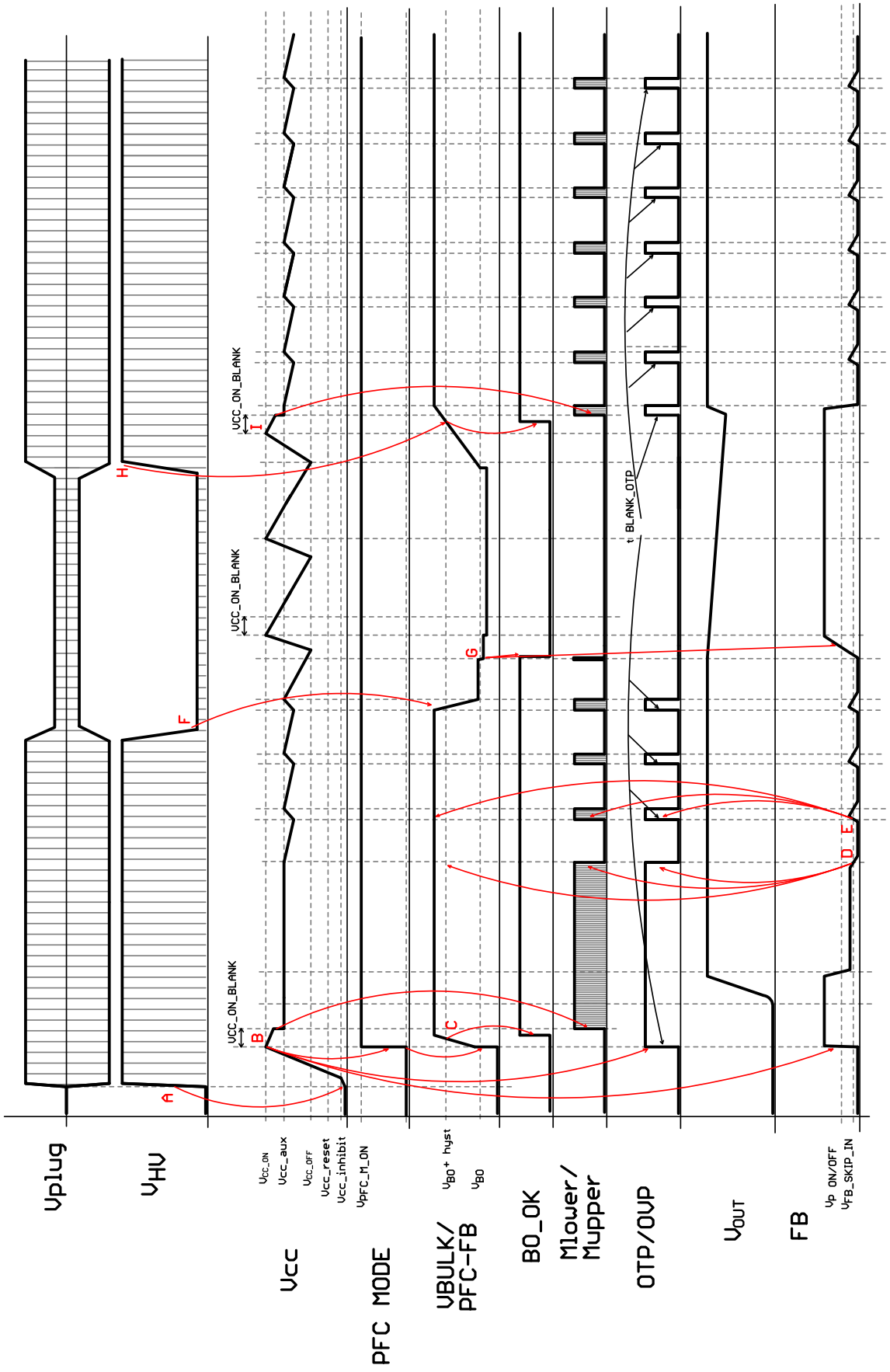


Figure 25. Startup, Skip−mode Operation, Low Line Detection and Restart into Skip

PACKAGE DIMENSIONS

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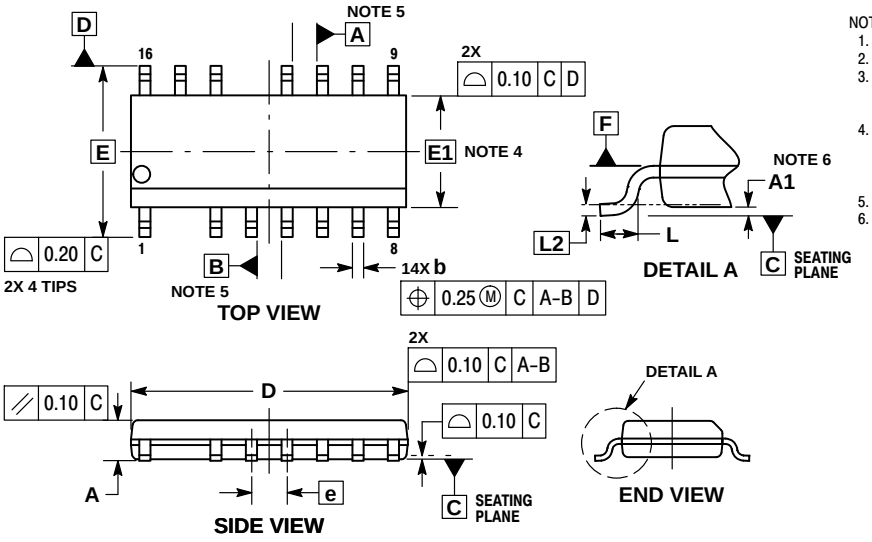

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.35	0.49
c	0.17	0.25
D	9.80	10.00
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.203 BSC	

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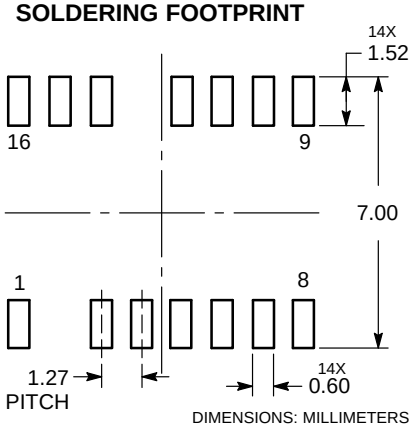

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