

# MC74HC597A

## 8-Bit Serial or Parallel-Input/Serial-Output Shift Register with Input Latch

### High-Performance Silicon-Gate CMOS

The MC74HC597A is identical in pinout to the LS597. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of an 8-bit input latch which feeds parallel data to an 8-bit shift register. Data can also be loaded serially.

The HC597A is similar in function to the HC589A, which is a 3-state device.

#### Features

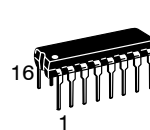
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 516 FETs or 129 Equivalent Gates
- These are Pb-Free Devices\*



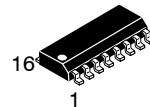
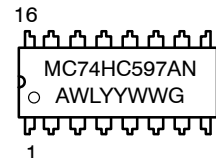
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<http://onsemi.com>

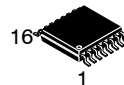
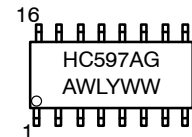
#### MARKING DIAGRAMS



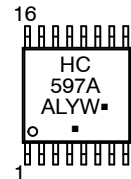
PDIP-16  
N SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G or ▪ = Pb-Free Package  
(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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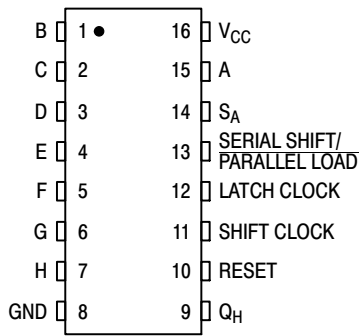


Figure 1. Pin Assignment

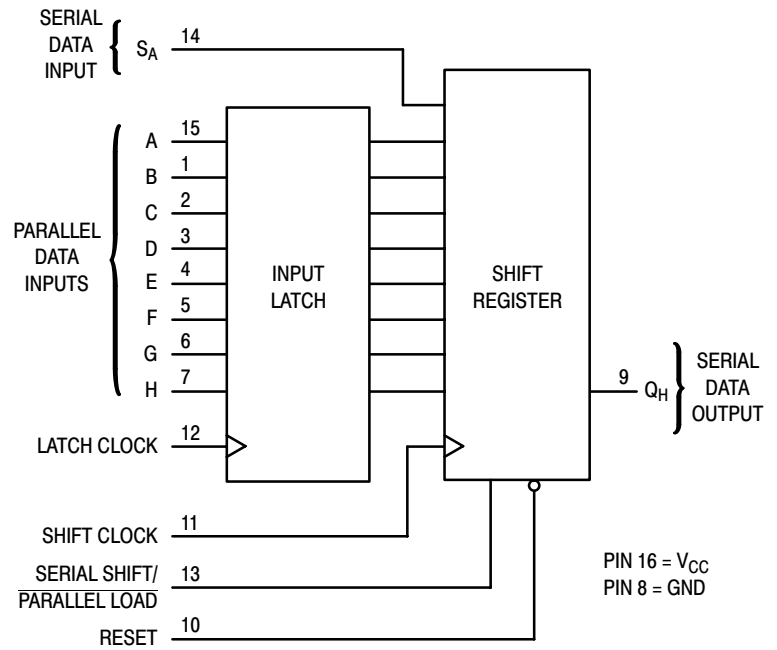


Figure 2. Logic Diagram

## ORDERING INFORMATION

| Device          | Package              | Shipping†         |
|-----------------|----------------------|-------------------|
| MC74HC597ANG    | PDIP-16<br>(Pb-Free) | 500 Units / Rail  |
| MC74HC597ADG    | SOIC-16<br>(Pb-Free) | 48 Units / Rail   |
| MC74HC597ADR2G  | SOIC-16<br>(Pb-Free) | 2500 Units / Reel |
| MC74HC597ADTR2G | TSSOP-16*            | 2500 Units / Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

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## MAXIMUM RATINGS\*

| Symbol    | Parameter  | Value                   | Unit |
|-----------|--|-------------------------|------|
| $V_{CC}$  | DC Supply Voltage (Referenced to GND)  | - 0.5 to + 7.0          | V    |
| $V_{in}$  | DC Input Voltage (Referenced to GND)   | - 0.5 to $V_{CC} + 0.5$ | V    |
| $V_{out}$ | DC Output Voltage (Referenced to GND)  | - 0.5 to $V_{CC} + 0.5$ | V    |
| $I_{in}$  | DC Input Current, per Pin  | $\pm 20$                | mA   |
| $I_{out}$ | DC Output Current, per Pin   | $\pm 25$                | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins   | $\pm 50$                | mA   |
| $P_D$     | Power Dissipation in Still Air, Plastic or Ceramic DIP†<br>SOIC Package†<br>TSSOP Package†               | 750<br>500<br>450       | mW   |
| $T_{stg}$ | Storage Temperature  | - 65 to + 150           | °C   |
| $T_L$     | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP, SOIC or TSSOP Package)<br>(Ceramic DIP) | 260<br>300              | °C   |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C  
Ceramic DIP: - 10 mW/°C from 100° to 125°C  
SOIC Package: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

| Symbol            | Parameter  | Min  | Max      | Unit |
|-------------------|--|------|----------|------|
| $V_{CC}$          | DC Supply Voltage (Referenced to GND)                | 2.0  | 6.0      | V    |
| $V_{in}, V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0    | $V_{CC}$ | V    |
| $T_A$             | Operating Temperature, All Package Types             | - 55 | + 125    | °C   |
| $t_r, t_f$        | Input Rise and Fall Time<br>(Figure 1)               |      |          | ns   |
|                   | $V_{CC} = 2.0 \text{ V}$                             | 0    | 1000     |      |
|                   | $V_{CC} = 3.0 \text{ V}$                             | 0    | 600      |      |
|                   | $V_{CC} = 4.5 \text{ V}$                             | 0    | 500      |      |
|                   | $V_{CC} = 6.0 \text{ V}$                             | 0    | 400      |      |

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## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol          | Parameter                                      | Test Conditions  | V <sub>CC</sub><br>V | Guaranteed Limit |         |          | Unit |
|-----------------|--|--|----------------------|------------------|---------|----------|------|
|                 |  |  |                      | - 55 to<br>25 °C | ≤ 85 °C | ≤ 125 °C |      |
| V <sub>IH</sub> | Minimum High-Level Input Voltage               | V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V<br> I <sub>out</sub>   ≤ 20 μA   | 2.0                  | 1.5              | 1.5     | 1.5      | V    |
|                 |  |  | 3.0                  | 2.1              | 2.1     | 2.1      |      |
|                 |  |  | 4.5                  | 3.15             | 3.15    | 3.15     |      |
|                 |  |  | 6.0                  | 4.2              | 4.2     | 4.2      |      |
| V <sub>IL</sub> | Maximum Low-Level Input Voltage                | V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V<br> I <sub>out</sub>   ≤ 20 μA   | 2.0                  | 0.5              | 0.5     | 0.5      | V    |
|                 |  |  | 3.0                  | 0.9              | 0.9     | 0.9      |      |
|                 |  |  | 4.5                  | 1.35             | 1.35    | 1.35     |      |
|                 |  |  | 6.0                  | 1.8              | 1.8     | 1.8      |      |
| V <sub>OH</sub> | Minimum High-Level Output Voltage              | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA  | 2.0                  | 1.9              | 1.9     | 1.9      | V    |
|                 |  |  | 4.5                  | 4.4              | 4.4     | 4.4      |      |
|                 |  |  | 6.0                  | 5.9              | 5.9     | 5.9      |      |
|                 |  | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 2.4 mA<br> I <sub>out</sub>   ≤ 4.0 mA<br> I <sub>out</sub>   ≤ 5.2 mA | 3.0                  | 2.48             | 2.34    | 2.20     |      |
|                 |  |  | 4.5                  | 3.98             | 3.84    | 3.70     |      |
|                 |  |  | 6.0                  | 5.48             | 5.34    | 5.20     |      |
| V <sub>OL</sub> | Maximum Low-Level Output Voltage               | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA  | 2.0                  | 0.1              | 0.1     | 0.1      | V    |
|                 |  |  | 4.5                  | 0.1              | 0.1     | 0.1      |      |
|                 |  |  | 6.0                  | 0.1              | 0.1     | 0.1      |      |
|                 |  | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 2.4 mA<br> I <sub>out</sub>   ≤ 4.0 mA<br> I <sub>out</sub>   ≤ 5.2 mA | 3.0                  | 0.26             | 0.33    | 0.40     |      |
|                 |  |  | 4.5                  | 0.26             | 0.33    | 0.40     |      |
|                 |  |  | 6.0                  | 0.26             | 0.33    | 0.40     |      |
| I <sub>in</sub> | Maximum Input Leakage Current                  | V <sub>in</sub> = V <sub>CC</sub> or GND   | 6.0                  | ± 0.1            | ± 1.0   | ± 1.0    | μA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current (per Package) | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0 μA  | 6.0                  | 4                | 40      | 160      | μA   |

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## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

| Symbol                                 | Parameter   | V <sub>CC</sub><br>V                    | Guaranteed Limit |        |         | Unit |
|--|---|---|------------------|--------|---------|------|
|  |   |   | - 55 to<br>25°C  | ≤ 85°C | ≤ 125°C |      |
| f <sub>max</sub>                       | Maximum Clock Frequency (50% Duty Cycle), Shift Clock<br>(Figures 4 and 10)                           | 2.0                                     | 10               | 9      | 8       | MHz  |
|  |   | 3.0                                     | 15               | 14     | 12      |      |
|  |   | 4.5                                     | 30               | 28     | 25      |      |
|  |   | 6.0                                     | 50               | 45     | 40      |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Latch Clock to Q <sub>H</sub><br>(Figures 3 and 10)                        | 2.0                                     | 175              | 225    | 275     | ns   |
|  |   | 3.0                                     | 100              | 110    | 125     |      |
|  |   | 4.5                                     | 40               | 50     | 60      |      |
|  |   | 6.0                                     | 30               | 40     | 50      |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Shift Clock to Q <sub>H</sub><br>(Figures 4 and 10)                        | 2.0                                     | 160              | 200    | 240     | ns   |
|  |   | 3.0                                     | 90               | 130    | 160     |      |
|  |   | 4.5                                     | 30               | 40     | 48      |      |
|  |   | 6.0                                     | 25               | 30     | 40      |      |
| t <sub>PHL</sub>                       | Maximum Propagation Delay, Reset to Q <sub>H</sub><br>(Figures 5 and 10)                              | 2.0                                     | 160              | 200    | 240     | ns   |
|  |   | 3.0                                     | 90               | 130    | 160     |      |
|  |   | 4.5                                     | 30               | 40     | 48      |      |
|  |   | 6.0                                     | 25               | 30     | 40      |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Serial Shift/ <u>Parallel Load</u> to Q <sub>H</sub><br>(Figures 6 and 10) | 2.0                                     | 160              | 200    | 240     | ns   |
|  |   | 3.0                                     | 90               | 130    | 160     |      |
|  |   | 4.5                                     | 30               | 40     | 48      |      |
|  |   | 6.0                                     | 25               | 30     | 40      |      |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, Any Output<br>(Figures 3 and 10)                                      | 2.0                                     | 75               | 95     | 110     | ns   |
|  |   | 3.0                                     | 27               | 32     | 36      |      |
|  |   | 4.5                                     | 15               | 19     | 22      |      |
|  |   | 6.0                                     | 13               | 16     | 19      |      |
| C <sub>in</sub>                        | Maximum Input Capacitance   | —                                       | 10               | 10     | 10      | pF   |
| C <sub>PD</sub>                        | Power Dissipation Capacitance (Per Package)*  | Typical @ 25°C, V <sub>CC</sub> = 5.0 V |                  |        | pF      |      |
|  |   | 40                                      |                  |        |         |      |

\* Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

## PIN DESCRIPTIONS

### DATA INPUTS

#### A, B, C, D, E, F, G, H (Pins 15, 1, 2, 3, 4, 5, 6, 7)

Parallel data inputs. Data on these inputs is stored in the input latch on the rising edge of the Latch Clock input.

#### S<sub>A</sub> (Pin 14)

Serial data input. Data on this input is shifted into the shift register on the rising edge of the Shift Clock input if Serial Shift/Parallel Load is high. Data on this input is ignored when Serial Shift/Parallel Load is low.

### CONTROL INPUTS

#### Serial Shift/Parallel Load (Pin 13)

Shift register mode control. When a high level is applied to this pin, the shift register is allowed to serially shift data. When a low level is applied to this pin, the shift register accepts parallel data from the input latch, and serial shifting is inhibited.

#### Reset (Pin 10)

Asynchronous, Active-low shift register reset. A low level applied to this input resets the shift register to a low level, but does not change the data in the input latch.

#### Shift Clock (Pin 11)

Serial shift register clock. A low-to-high transition on this input shifts data on the Serial Data Input into the shift register and data in stage H is shifted out Q<sub>H</sub>, being replaced by the data previously stored in stage G.

#### Latch Clock (Pin 12)

Latch clock. A low-to-high transition on this input loads the parallel data on inputs A–H into the input latch.

### OUTPUT

#### Q<sub>H</sub> (Pin 9)

Serial data output. This pin is the output from the last stage of the shift register.

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## TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

| Symbol                          | Parameter   | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|---------------------------------|---|----------------------|------------------|--------|---------|------|
|                                 |   |                      | - 55 to<br>25°C  | ≤ 85°C | ≤ 125°C |      |
| t <sub>su</sub>                 | Minimum Setup Time, Parallel Data inputs A–H to Latch Clock<br>(Figure 7)         | 2.0                  | 70               | 80     | 90      | ns   |
|                                 |   | 3.0                  | 40               | 45     | 50      |      |
|                                 |   | 4.5                  | 15               | 19     | 24      |      |
|                                 |   | 6.0                  | 13               | 16     | 20      |      |
| t <sub>su</sub>                 | Minimum Setup Time, Serial Data Input S <sub>A</sub> to Shift Clock<br>(Figure 8) | 2.0                  | 70               | 80     | 90      | ns   |
|                                 |   | 3.0                  | 40               | 45     | 50      |      |
|                                 |   | 4.5                  | 15               | 19     | 24      |      |
|                                 |   | 6.0                  | 13               | 16     | 20      |      |
| t <sub>su</sub>                 | Minimum Setup Time, Serial Shift/Parallel Load to Shift Clock<br>(Figure 9)       | 2.0                  | 70               | 80     | 90      | ns   |
|                                 |   | 3.0                  | 40               | 45     | 50      |      |
|                                 |   | 4.5                  | 15               | 19     | 24      |      |
|                                 |   | 6.0                  | 13               | 16     | 20      |      |
| t <sub>h</sub>                  | Minimum Hold Time, Latch Clock to Parallel Data Inputs A–H<br>(Figure 7)          | 2.0                  | 15               | 20     | 30      | ns   |
|                                 |   | 3.0                  | 10               | 15     | 25      |      |
|                                 |   | 4.5                  | 2                | 3      | 5       |      |
|                                 |   | 6.0                  | 2                | 3      | 4       |      |
| t <sub>h</sub>                  | Minimum Hold Time, Shift Clock to Serial Data Input S <sub>A</sub><br>(Figure 8)  | 2.0                  | 2                | 2      | 2       | ns   |
|                                 |   | 3.0                  | 2                | 2      | 2       |      |
|                                 |   | 4.5                  | 2                | 2      | 2       |      |
|                                 |   | 6.0                  | 2                | 2      | 2       |      |
| t <sub>rec</sub>                | Minimum Recovery Time, Reset Inactive to Shift Clock<br>(Figure 5)                | 2.0                  | 70               | 80     | 90      | ns   |
|                                 |   | 3.0                  | 40               | 45     | 50      |      |
|                                 |   | 4.5                  | 15               | 19     | 24      |      |
|                                 |   | 6.0                  | 13               | 16     | 20      |      |
| t <sub>w</sub>                  | Minimum Pulse Width, Latch Clock and Shift Clock<br>(Figures 3 and 4)             | 2.0                  | 60               | 70     | 80      | ns   |
|                                 |   | 3.0                  | 35               | 40     | 45      |      |
|                                 |   | 4.5                  | 12               | 15     | 19      |      |
|                                 |   | 6.0                  | 10               | 13     | 16      |      |
| t <sub>w</sub>                  | Minimum Pulse Width, Reset<br>(Figure 5)  | 2.0                  | 60               | 70     | 80      | ns   |
|                                 |   | 3.0                  | 35               | 40     | 45      |      |
|                                 |   | 4.5                  | 12               | 15     | 19      |      |
|                                 |   | 6.0                  | 10               | 13     | 16      |      |
| t <sub>w</sub>                  | Minimum Pulse Width, Serial Shift/Parallel Load<br>(Figure 6)                     | 2.0                  | 60               | 70     | 80      | ns   |
|                                 |   | 3.0                  | 35               | 40     | 45      |      |
|                                 |   | 4.5                  | 12               | 15     | 19      |      |
|                                 |   | 6.0                  | 10               | 13     | 16      |      |
| t <sub>r</sub> , t <sub>f</sub> | Maximum Input Rise and Fall Times<br>(Figure 3)                                   | 2.0                  | 1000             | 1000   | 1000    | ns   |
|                                 |   | 3.0                  | 800              | 800    | 800     |      |
|                                 |   | 4.5                  | 500              | 500    | 500     |      |
|                                 |   | 6.0                  | 400              | 400    | 400     |      |

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

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## FUNCTION TABLE

| Operation  | Inputs |                                |                        |                        |                                   |                           | Resulting Function |   |                                   |
|--|--------|--------------------------------|------------------------|------------------------|-----------------------------------|---------------------------|--------------------|---|-----------------------------------|
|  | Reset  | Serial Shift/<br>Parallel Load | Latch<br>Clock         | Shift<br>Clock         | Serial<br>Input<br>S <sub>A</sub> | Parallel<br>Inputs<br>A–H | Latch<br>Contents  | Shift<br>Register<br>Contents                               | Output<br>Q <sub>H</sub>          |
| Reset shift register   | L      | X                              | L, H, $\bar{\text{L}}$ | X                      | X                                 | X                         | U                  | L   | L                                 |
| Reset shift register; load parallel data into data latch                     | L      | X                              | $\bar{\text{L}}$       | X                      | X                                 | a–h                       | a–h                | L   | L                                 |
| Load parallel data into data latch   | H      | H                              | $\bar{\text{L}}$       | L, H, $\bar{\text{L}}$ | X                                 | a–h                       | a–h                | U   | U                                 |
| Transfer latch contents to shift register                                    | H      | L                              | L, H, $\bar{\text{L}}$ | X                      | X                                 | X                         | U                  | LR <sub>N</sub> → SR <sub>N</sub>                           | LR <sub>H</sub>                   |
| Contents of data latch and shift register are unchanged                      | H      | H                              | L, H, $\bar{\text{L}}$ | L, H, $\bar{\text{L}}$ | X                                 | X                         | U                  | U   | U                                 |
| Load parallel data into data latch and shift register                        | H      | L                              | $\bar{\text{L}}$       | X                      | X                                 | a–h                       | a–h                | a–h   | h                                 |
| Shift serial data into shift register  | H      | H                              | X                      | $\bar{\text{L}}$       | D                                 | X                         | *                  | SR <sub>A</sub> = D;<br>SR <sub>N</sub> → SR <sub>N+1</sub> | SR <sub>G</sub> → SR <sub>H</sub> |
| Load parallel data into data latch and shift serial data into shift register | H      | H                              | $\bar{\text{L}}$       | $\bar{\text{L}}$       | D                                 | a–h                       | a–h                | SR <sub>A</sub> = D;<br>SR <sub>N</sub> → SR <sub>N+1</sub> | SR <sub>G</sub> → SR <sub>H</sub> |

LR = latch register contents  
 SR = shift register contents  
 \* = depends on latch clock input

a–h = data at parallel data inputs A–H  
 D = data (L, H) at serial data input S<sub>A</sub>

U = remains unchanged  
 X = don't care

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## SWITCHING WAVEFORMS

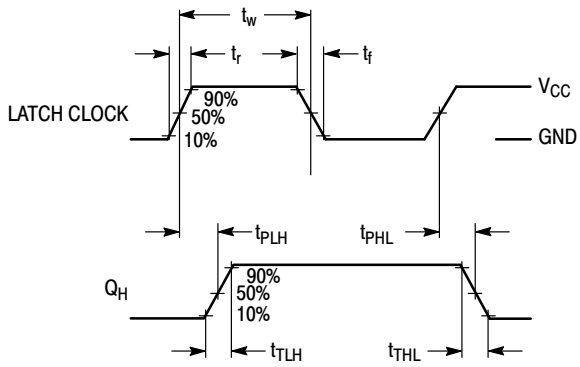


Figure 3. (Serial Shift/Parallel Load = L)

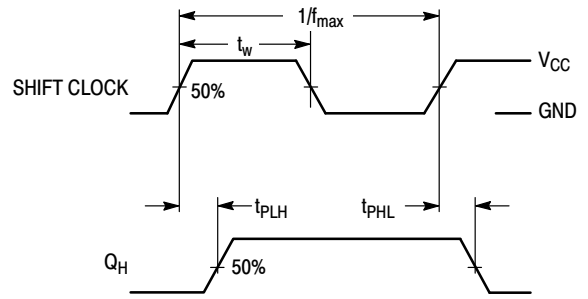


Figure 4. (Serial Shift/Parallel Load = H)

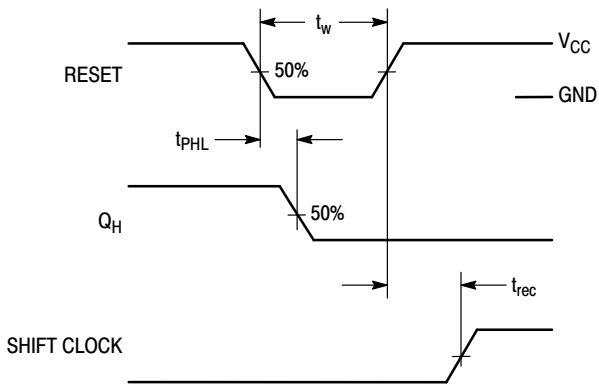


Figure 5.

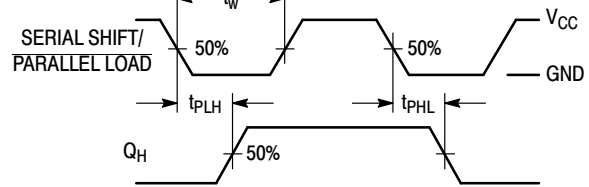


Figure 6.

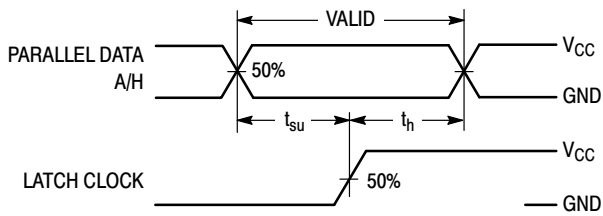


Figure 7.

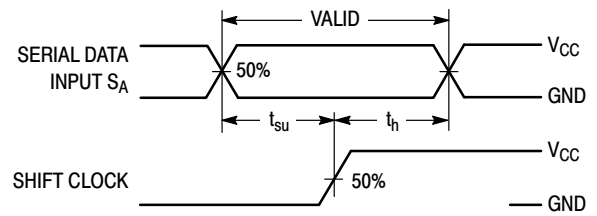


Figure 8.

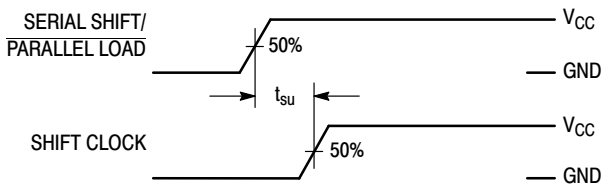
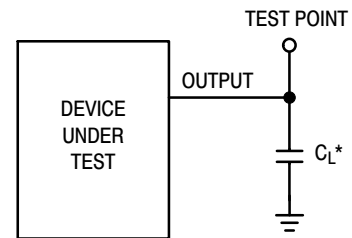


Figure 9.



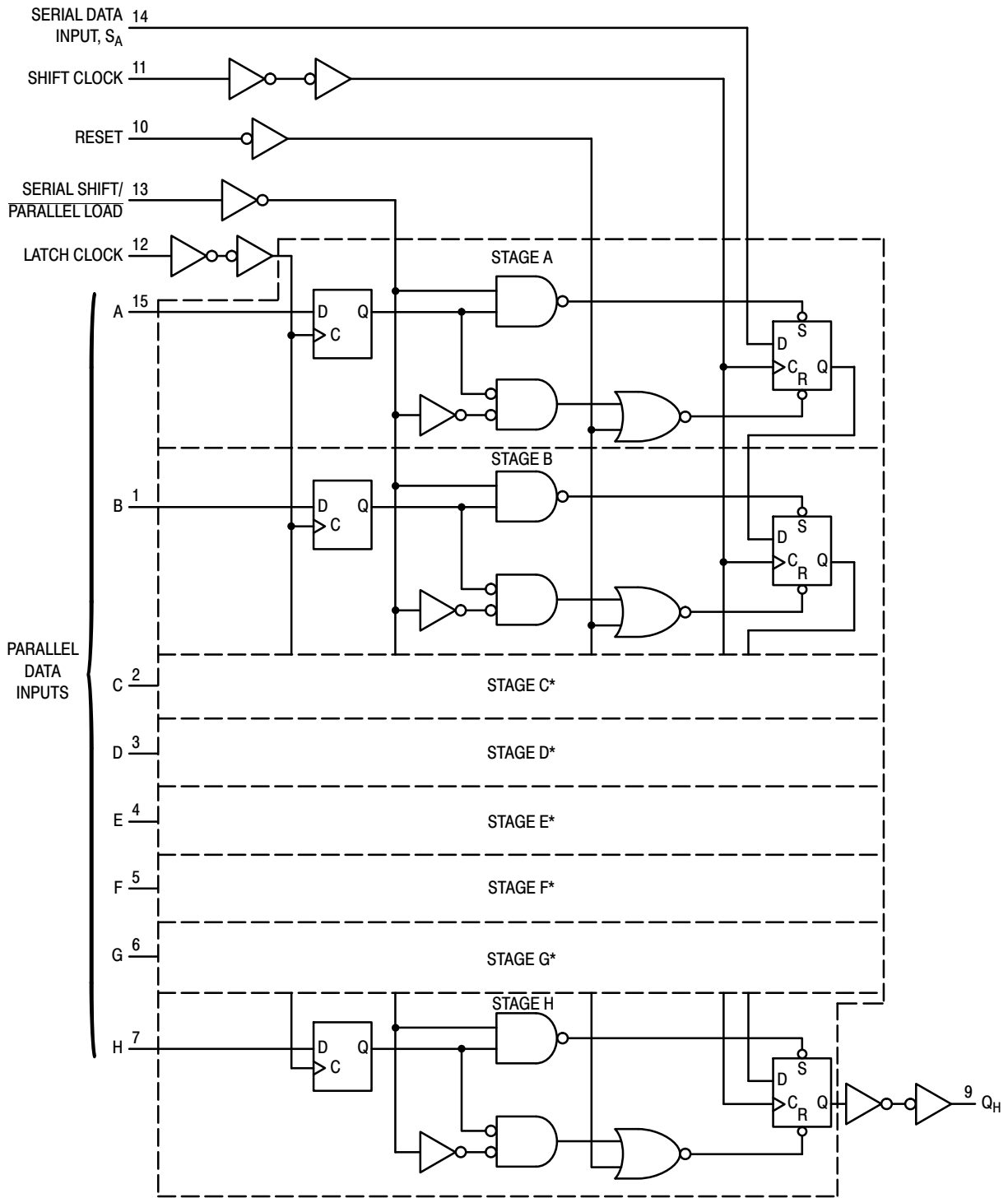
\*Includes all probe and jig capacitance

Figure 10. Test Circuit



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## EXPANDED LOGIC DIAGRAM



\*NOTE: Stages C thru G (not shown in detail) are identical to stages A and B above.

**Figure 11. Extended Logic Diagram**

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## TIMING DIAGRAM

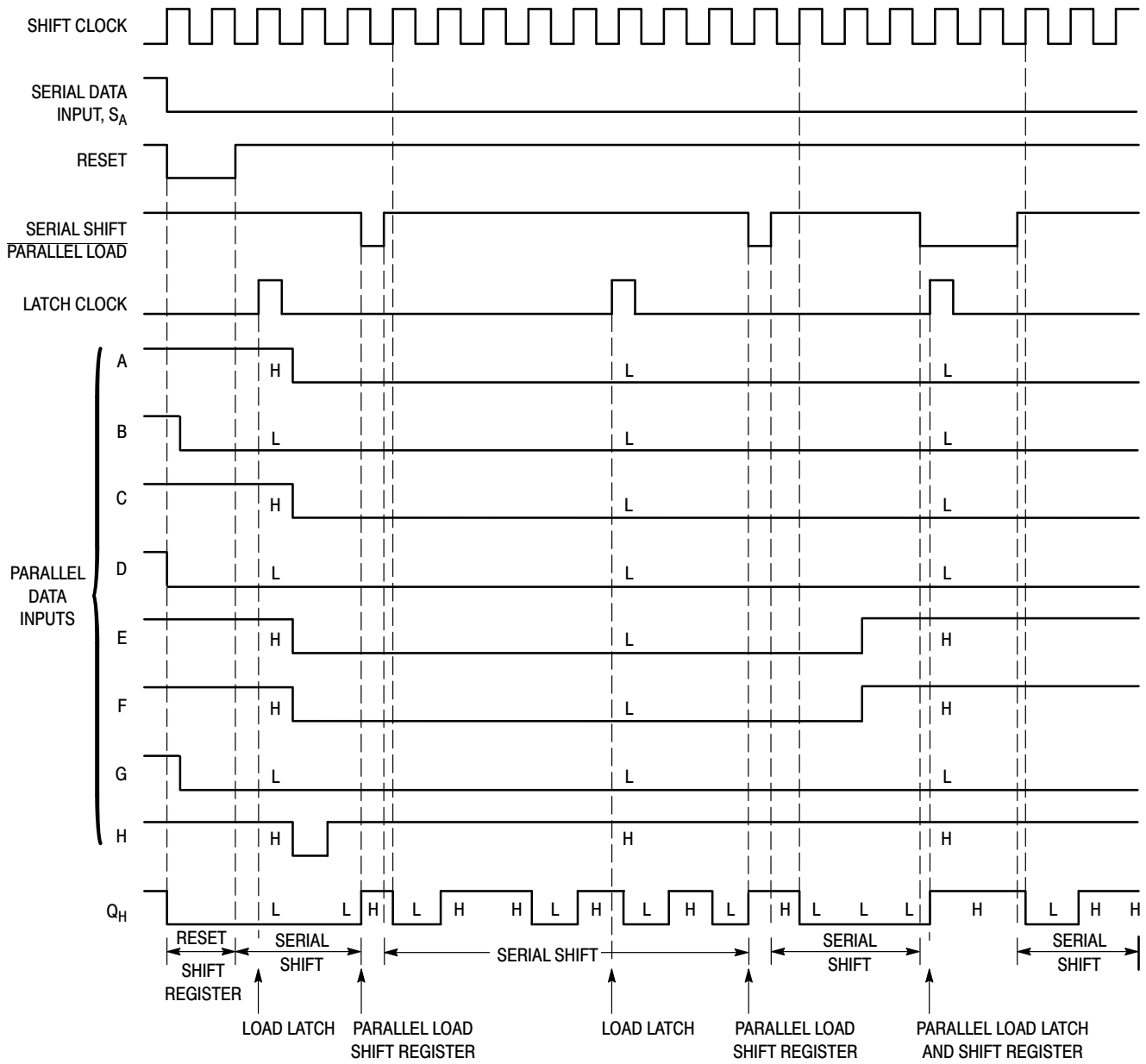
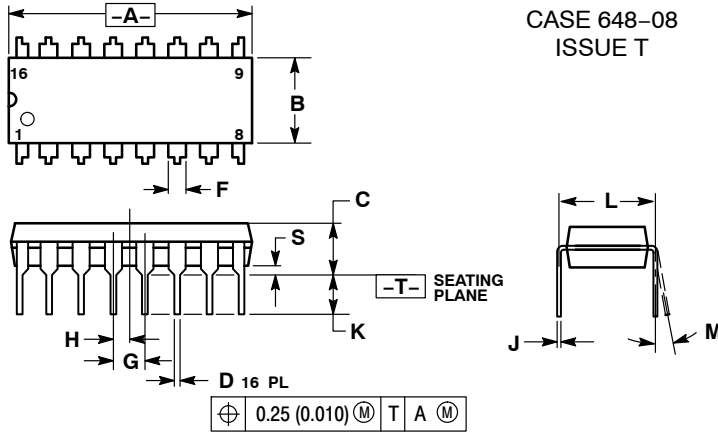


Figure 12. Timing Diagram

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## PACKAGE DIMENSIONS

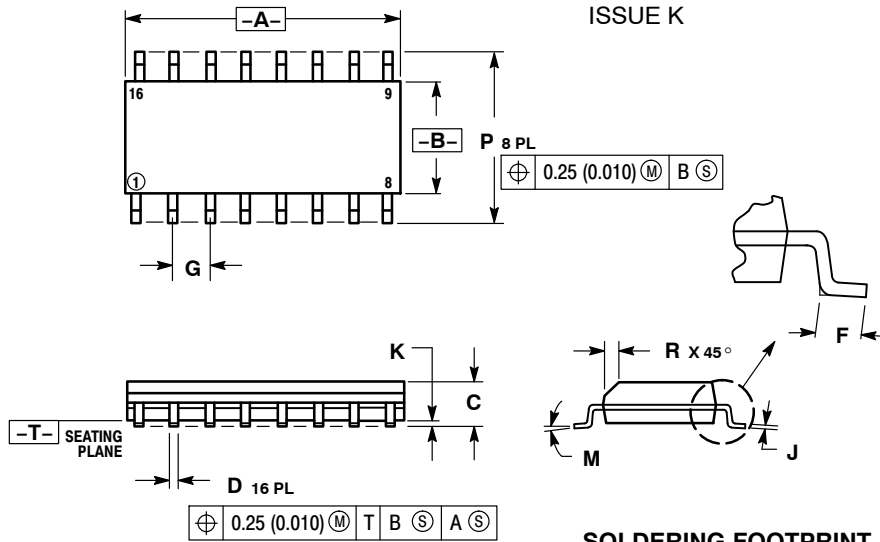
### PDIP-16 N SUFFIX CASE 648-08 ISSUE T



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.740     | 0.770 | 18.80       | 19.55 |
| B   | 0.250     | 0.270 | 6.35        | 6.85  |
| C   | 0.145     | 0.175 | 3.69        | 4.44  |
| D   | 0.015     | 0.021 | 0.39        | 0.53  |
| F   | 0.040     | 0.70  | 1.02        | 1.77  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| H   | 0.050 BSC |       | 1.27 BSC    |       |
| J   | 0.008     | 0.015 | 0.21        | 0.38  |
| K   | 0.110     | 0.130 | 2.80        | 3.30  |
| L   | 0.295     | 0.305 | 7.50        | 7.74  |
| M   | 0°        | 10°   | 0°          | 10°   |
| S   | 0.020     | 0.040 | 0.51        | 1.01  |

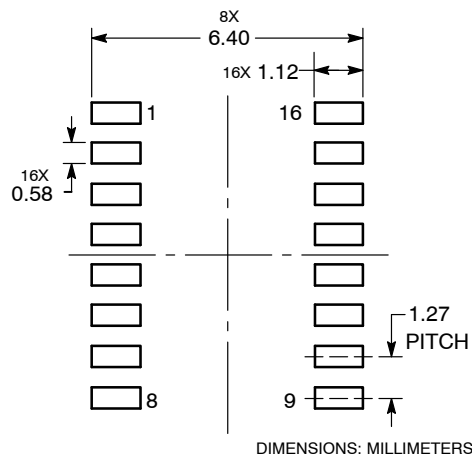
### SOIC-16 D SUFFIX CASE 751B-05 ISSUE K



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 9.80        | 10.00 | 0.386     | 0.393 |
| B   | 3.80        | 4.00  | 0.150     | 0.157 |
| C   | 1.35        | 1.75  | 0.054     | 0.068 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.40        | 1.25  | 0.016     | 0.049 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| J   | 0.19        | 0.25  | 0.008     | 0.009 |
| K   | 0.10        | 0.25  | 0.004     | 0.009 |
| M   | 0°          | 7°    | 0°        | 7°    |
| P   | 5.80        | 6.20  | 0.229     | 0.244 |
| R   | 0.25        | 0.50  | 0.010     | 0.019 |

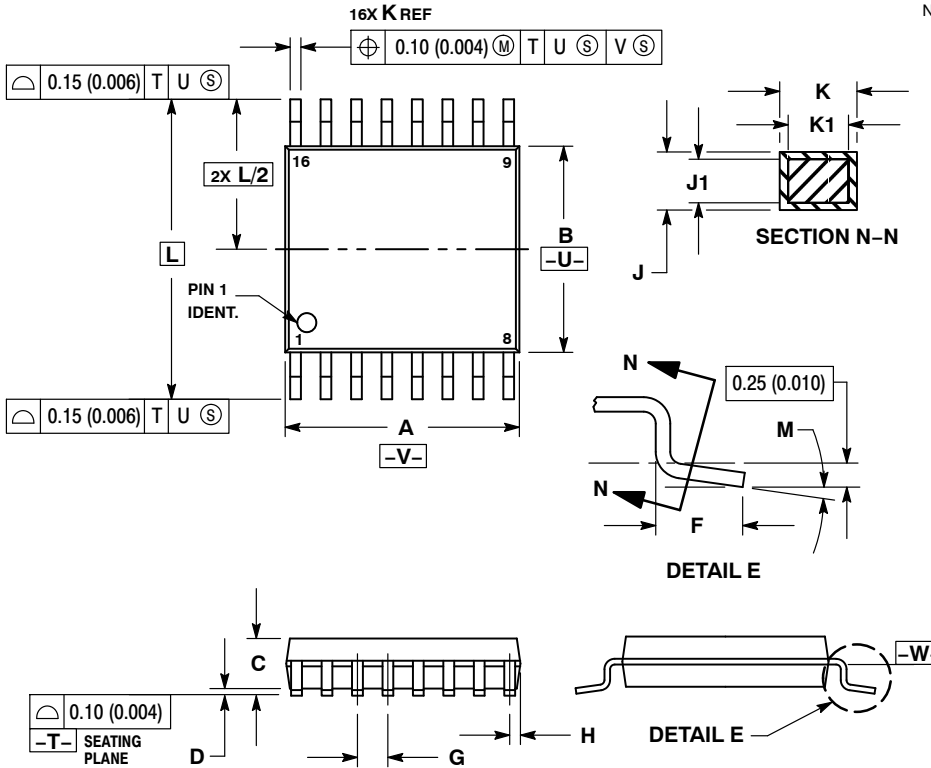
### SOLDERING FOOTPRINT



# MC74HC597A

## PACKAGE DIMENSIONS

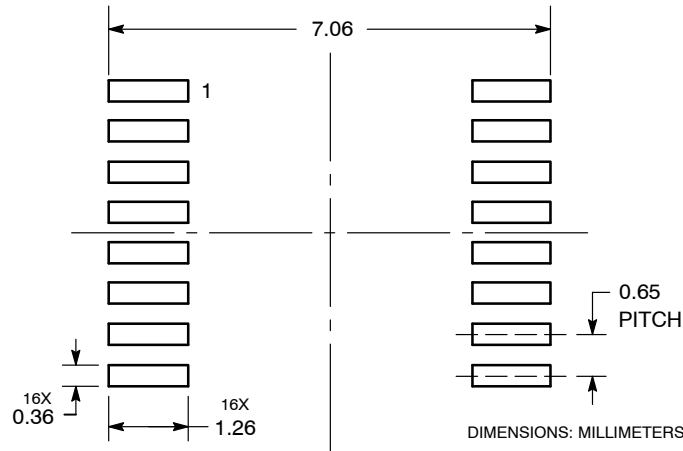
TSSOP-16  
DT SUFFIX  
CASE 948F-01  
ISSUE B



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.18        | 0.28 | 0.007     | 0.011 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

### SOLDERING FOOTPRINT



# MC74HC597A

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