

# 1/2.7-Inch 2.1 Mp/Full HD Digital Image Sensor

## AR0237/D, Rev. 2

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### Features

- Superior low-light performance
- Latest 3.0 μm pixel with ON Semiconductor DR-Pix™ technology with Dual Conversion Gain
- Full HD support at up to 1080P 60 fps for superior video performance
- Linear or high dynamic range capture
- Supports line interleaved T1/T2 readout to enable HDR processing in ISP chip
- Support for external mechanical shutter
- On-chip phase-locked loop (PLL) oscillator
- Integrated position-based color and lens shading correction
- Slave mode for precise frame-rate control
- Stereo/3D camera support
- Statistics engine
- Data interfaces: four-lane serial high-speed pixel interface (HiSPi) differential signaling (SLVS and HiVCM), or parallel
- Auto black level calibration
- High-speed configurable context switching
- Temperature sensor

### Applications

- Video surveillance
- 1080p60 (Surveillance) video applications
- High dynamic range imaging

### General Description

ON Semiconductor's AR0237 is a 1/2.7-inch CMOS digital image sensor with an active-pixel array of 1928Hx1088V. It captures images in either linear or high dynamic range modes, with a rolling-shutter readout. It includes sophisticated camera functions such as in-pixel binning, windowing and both video and single frame modes. It is designed for both low light and high dynamic range scene performance. It is programmable through a simple two-wire serial interface. The AR0237 produces extraordinarily clear, sharp digital pictures, and its ability to capture both continu-

ous video and single frames makes it the perfect choice for a wide range of applications, including surveillance and HD video.

**Table 1: Key Parameters**

| Parameter                   | Typical Value  |   |
|-----------------------------|--|---|
| Optical format              | 1/2.7-inch (6.6 mm)  |   |
| Active pixels               | 1928(H) x 1088(V) (16:9 mode)                                  |   |
| Pixel size                  | 3.0 μm x 3.0 μm  |   |
| Color filter array          | RGB Bayer  |   |
| Shutter type                | Electronic rolling shutter and GRR                             |   |
| Input clock range           | 6 – 48 MHz   |   |
| Output clock maximum        | 148.5 Mp/s (4-lane HiSPi)<br>74.25 Mp/s (Parallel)             |   |
| Output                      | Serial   | HiSPi 10-, 12-, 14-, 16-, or 20-bit         |
|                             | Parallel   | 10-, 12-bit                                 |
| Frame rate                  | 1080p  | 60 fps linear mode                          |
|                             |  | 30 fps line interleaved mode                |
| Responsivity                | 4.0 V/lux-sec  |   |
| SNR <sub>MAX</sub>          | 41 dB  |   |
| Max Dynamic range           | Up to 96 dB  |   |
| Supply voltage              | I/O  | 1.8 or 2.8 V                                |
|                             | Digital  | 1.8 V                                       |
|                             | Analog   | 2.8 V                                       |
|                             | HiSPi  | 0.3 V - 0.6 V (SLVS), 1.7 V - 1.9 V (HiVcm) |
| Power consumption (typical) | < 300mW Line interleaved 1080p30<br><190mW 1080p30 Linear Mode |   |
| Operating temperature       | –30°C to +85°C ambient   |   |
| Package options             | 10x10 mm 80-pin iBGA<br>11.43x11.43 mm 48-pin mPLCC            |   |

## Ordering Information

**Table 2: Available Part Numbers**

| Part Number             | Product Description                                  | Orderable Product Attribute Description |
|-------------------------|--|---|
| AR0237CSSC00SUEA0-DR    | 2 Mp 1/2.7" Image Sensor RGB, 0deg CRA, iBGA Package | Drypack                                 |
| AR0237CSSC00SUEAD3-GEVK | RGB, 0deg CRA, iBGA Demo Kit                         | Demo Kit                                |
| AR0237CSSC00SUEAH3-GEVB | RGB, 0deg CRA, iBGA Headboard                        | Headboard                               |
| AR0237CSSC00SHRA0-DR-E  | 2Mp 1/2.7" Image Sensor RGB, 0deg CRA, mPLCC, HiSpi  | Drypack                                 |
| AR0237CSSC00SHRAD3-GEVK | RGB, 0deg CRA, mPLCC, Demo Kit, HiSpi                | Demo Kit                                |
| AR0237CSSC00SHRAH3-GEVB | RGB 0deg CRA, mPLCC, Headboard, HiSpi                | Headboard                               |

See the ON Semiconductor Device Nomenclature document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at [www.onsemi.com](http://www.onsemi.com).

## Table of Contents

|   |    |
|---|----|
| Features . . . . .                          | 1  |
| Applications . . . . .                      | 1  |
| General Description . . . . .               | 1  |
| Ordering Information . . . . .              | 2  |
| General Description . . . . .               | 4  |
| Functional Overview . . . . .               | 5  |
| Pixel Data Format . . . . .                 | 13 |
| Features Overview . . . . .                 | 15 |
| Electrical Specifications . . . . .         | 21 |
| Power-On Reset and Standby Timing . . . . . | 28 |



## General Description

The ON Semiconductor AR0237 can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a 1080p-resolution image at 60 frames per second (fps) through the HiSPi port. In linear mode, it outputs 12-bit or 10-bit A-Law compressed raw data, using either the parallel or serial (HiSPi) output ports. In high dynamic range mode, it outputs two exposure values that the ISP will combine into an HDR image. The device may be operated in video (master) mode or in single frame trigger mode.

FRAME\_VALID and LINE\_VALID signals are output on dedicated pins, along with a synchronized pixel clock in parallel mode.

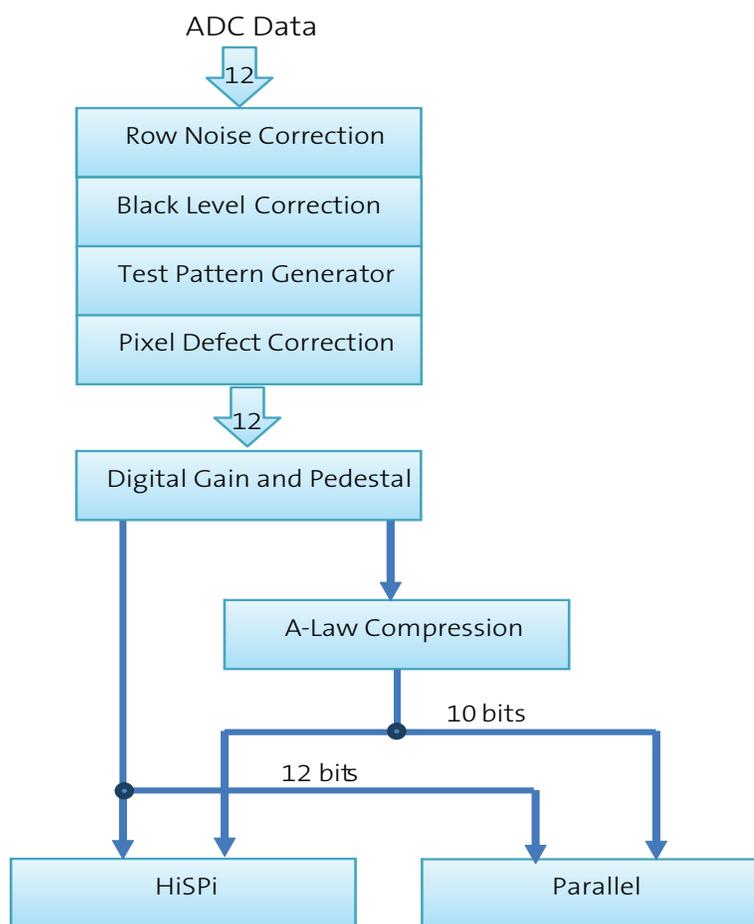
The AR0237 includes additional features to allow application-specific tuning: windowing and offset, auto black level correction, and on-board temperature sensor. Optional register information and histogram statistic information can be embedded in the first and last 2 lines of the image frame.

The AR0237 is designed to operate over a wide temperature range of -30°C to +85°C ambient.

## Functional Overview

The AR0237 is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) that can be optionally enabled to generate all internal clocks from a single master input clock running between 6 and 48 MHz. The maximum output pixel rate is 148.5 Mp/s, corresponding to a clock rate of 74.25 MHz. Figure 1 shows a block diagram of the sensor configured in linear mode, and in HDR mode.

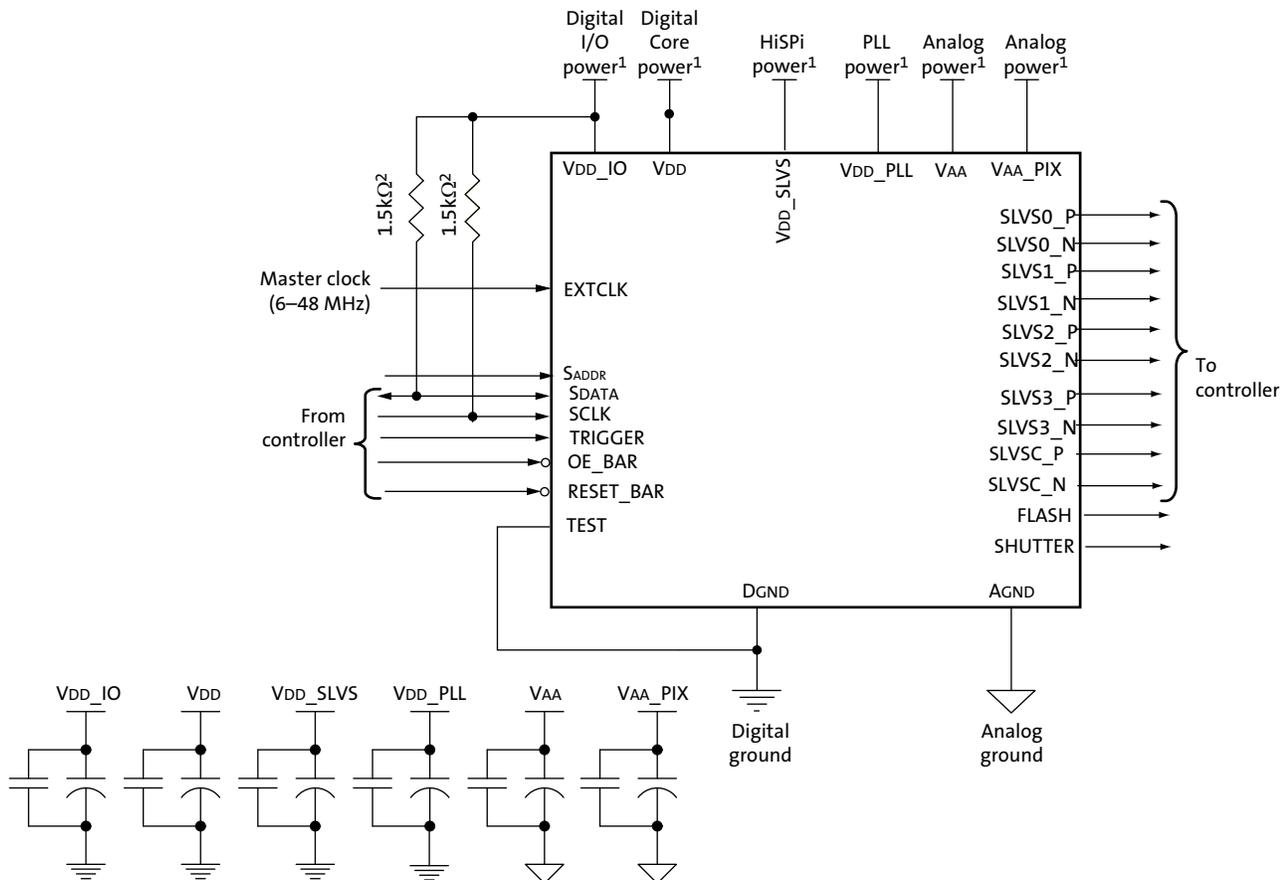
**Figure 1: Block Diagram of AR0237**



User interaction with the sensor is through the two-wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 2.1 Mp Active-Pixel Sensor array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an analog-to-digital converter (ADC). The output from the ADC is a 12-bit value for each pixel in the array. The ADC output passes through a digital processing chain (which provides further data path corrections and applies digital gain). The sensor also offers a

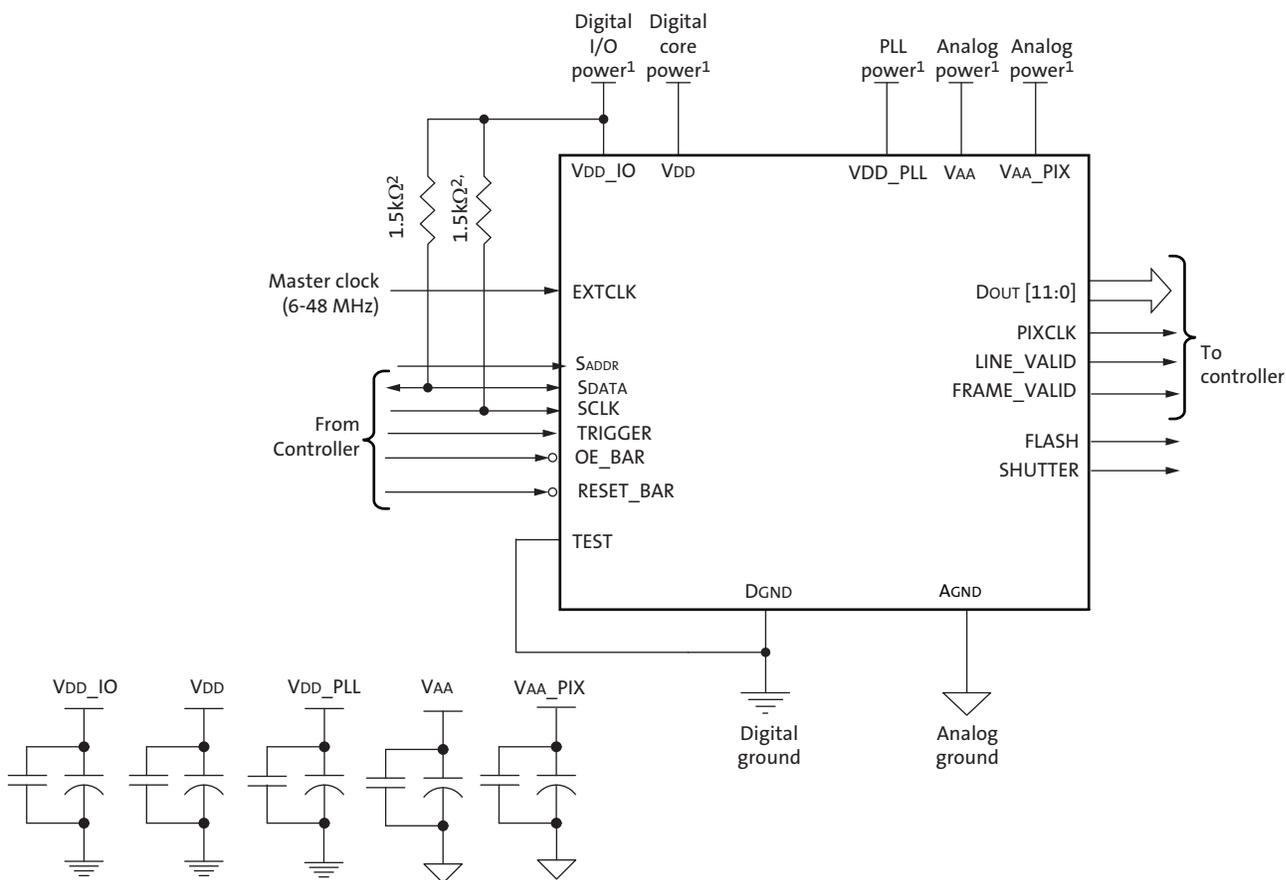
high dynamic range mode of operation where two images are taken using different exposures. These images are output from the sensor and the ISP must combine them into one high dynamic range image.

Figure 2: Typical Configuration: Serial Four-Lane HiSpi Interface



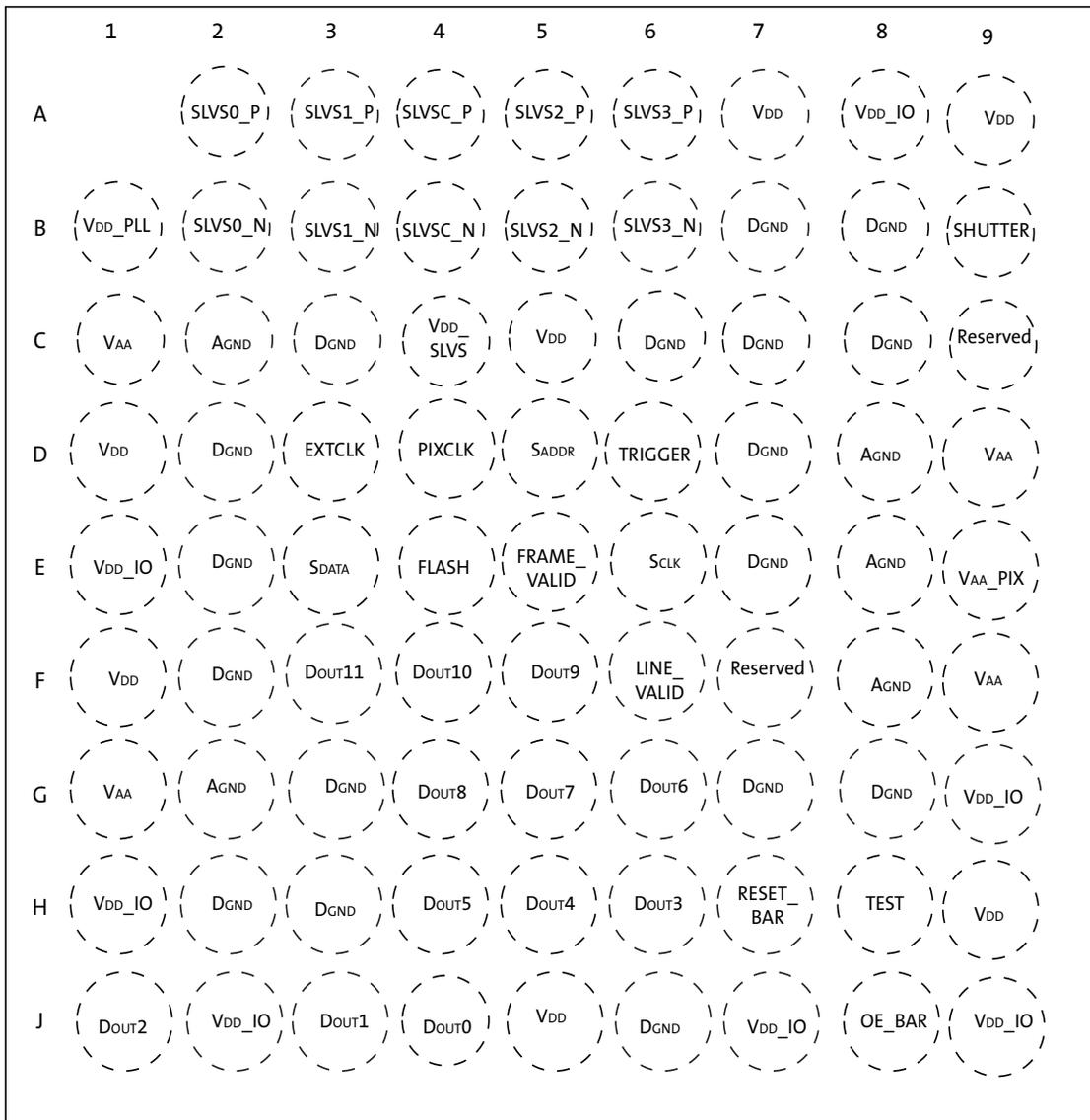
- Notes:
1. All power supplies must be adequately decoupled.
  2. ON Semiconductor recommends a resistor value of 1.5kΩ, but a greater value may be used for slower two-wire speed.
  3. The parallel interface output pads can be left unconnected if the serial output interface is used.
  4. ON Semiconductor recommends that 0.1μF and 10μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0230 demo headboard schematics for circuit recommendations.
  5. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
  6. I/O signals voltage must be configured to match VDD\_IO voltage to minimize any leakage currents.

Figure 3: Typical Configuration: Parallel Pixel Data Interface



- Notes:
1. All power supplies must be adequately decoupled.
  2. ON Semiconductor recommends a resistor value of 1.5kΩ, but a greater value may be used for slower two-wire speed.
  3. The serial interface output pads and VDDSLVS can be left unconnected if the parallel output interface is used.
  4. ON Semiconductor recommends that 0.1μF and 10μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0237 demo headboard schematics for circuit recommendations.
  5. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
  6. I/O signals voltage must be configured to match VDD\_IO voltage to minimize any leakage currents.
  7. The EXTCLK input is limited to 6-48 MHz.

Figure 4: 80-Ball IBGA Package



Top View  
(Ball Down)

**Table 3: Pin Descriptions, 80-ball iBGA**

| Name        | iBGA Pin   | Type   | Description   |
|-------------|--|--------|---|
| SLVS0_P     | A2   | Output | HiSPi serial data, lane 0, differential P.  |
| SLVS1_P     | A3   | Output | HiSPi serial data, lane 1, differential P.  |
| SLVSC_P     | A4   | Output | HiSPi serial DDR clock differential P.  |
| SLVS2_P     | A5   | Output | HiSPi serial data, lane 2, differential P.  |
| SLVS3_P     | A6   | Output | HiSPi serial data, lane 3, differential P.  |
| VDD_PLL     | B1   | Power  | PLL power.  |
| SLVS0_N     | B2   | Output | HiSPi serial data, lane 0, differential N.  |
| SLVS1_N     | B3   | Output | HiSPi serial data, lane 1, differential N.  |
| SLVSC_N     | B4   | Output | HiSPi serial DDR clock differential N.  |
| SLVS2_N     | B5   | Output | HiSPi serial data, lane 2, differential N.  |
| SLVS3_N     | B6   | Output | HiSPi serial data, lane 3, differential N.  |
| SHUTTER     | B9   | Output | Control for external mechanical shutter. Can be left floating if not used.  |
| VAA         | C1, G1, D9, F9   | Power  | Analog power.   |
| AGND        | C2, G2, D8, E8, F8   | Power  | Analog ground.  |
| VDD_SLVS    | C4   | Power  | 0.3V-0.6V or 1.7V - 1.9V port to HiSPi Output Driver. Set the High_VCM (R0x306E[9]) bit to 1 when configuring VDD_SLVS to 1.7 – 1.9V. |
| VDD         | C5, J5, A9, H9, A7, D1, F1   | Power  | Digital power.  |
| Reserved    | C9, F7   |        |   |
| DGND        | B7, C7, D7, E7, G7, B8, C8, G8, D2, E2, F2, H2, C3, G3, H3, C6, J6 | Power  | Digital ground.   |
| EXTCLK      | D3   | Input  | External input clock.   |
| PIXCLK      | D4   | Output | Pixel clock out. Dout is valid on rising edge of this clock.  |
| SADDR       | D5   | Input  | Two-Wire Serial address select. 0: 0x20. 1: 0x30  |
| TRIGGER     | D6   | Input  | Exposure synchronization input.   |
| VAA_PIX     | E9   | Power  | Pixel power.  |
| VDD_IO      | E1, H1, J2, J7, A8, G9, J9   | Power  | I/O supply power.   |
| SDATA       | E3   | I/O    | Two-Wire Serial data I/O.   |
| FLASH       | E4   | Output | Flash control output.   |
| FRAME_VALID | E5   | Output | Asserted when Dout frame data is valid.   |
| SCLK        | E6   | Input  | Two-Wire Serial clock input.  |
| DOUT11      | F3   | Output | Parallel pixel data output (MSB)  |
| DOUT10      | F4   | Output | Parallel pixel data output.   |
| DOUT9       | F5   | Output | Parallel pixel data output.   |
| LINE_VALID  | F6   | Output | Asserted when Dout line data is valid.  |
| DOUT8       | G4   | Output | Parallel pixel data output.   |
| DOUT7       | G5   | Output | Parallel pixel data output.   |
| DOUT6       | G6   | Output | Parallel pixel data output.   |
| DOUT5       | H4   | Output | Parallel pixel data output.   |
| DOUT4       | H5   | Output | Parallel pixel data output.   |
| DOUT3       | H6   | Output | Parallel pixel data output.   |
| RESET_BAR   | H7   | Input  | Asynchronous reset (active LOW). All settings are restored to factory default.  |

**Table 3: Pin Descriptions, 80-ball iBGA**

| Name   | iBGA Pin | Type   | Description                                      |
|--------|----------|--------|--|
| TEST   | H8       | Input  | Manufacturing test enable pin (connect to Dgnd). |
| DOUT2  | J1       | Output | Parallel pixel data output.                      |
| DOUT1  | J3       | Output | Parallel pixel data output.                      |
| DOUT0  | J4       | Output | Parallel pixel data output (LSB)                 |
| OE_BAR | J8       | Input  | Output enable (active LOW).                      |

**Figure 5: 48 Pin mPLCC Package**

|    |          |        |        |        |        |        |         |           |        |         |         |          |    |
|----|----------|--------|--------|--------|--------|--------|---------|-----------|--------|---------|---------|----------|----|
|    | 6        | 5      | 4      | 3      | 2      | 1      | 48      | 47        | 46     | 45      | 44      | 43       |    |
|    | VDD_SLVS | SLVSON | SLVSOP | SLVS1N | SLVS1P | SLVSON | SLVSLCP | SLVS2N    | SLVS2P | SLVS3N  | SLVS3P  | VDD_IO   |    |
| 7  | DGND     |        |        |        |        |        |         |           |        |         |         | VDD_IO   | 42 |
| 8  | VDD_PLL  |        |        |        |        |        |         |           |        |         |         | VDD      | 41 |
| 9  | EXTCLK   |        |        |        |        |        |         |           |        |         |         | DGND     | 40 |
| 10 | VAA      |        |        |        |        |        |         |           |        |         |         | AGND     | 39 |
| 11 | AGND     |        |        |        |        |        |         |           |        |         |         | VAA_PIX  | 38 |
| 12 | VDD_IO   |        |        |        |        |        |         |           |        |         |         | VAA      | 37 |
| 13 | VDD      |        |        |        |        |        |         |           |        |         |         | RESERVED | 36 |
| 14 | DGND     |        |        |        |        |        |         |           |        |         |         | VAA      | 35 |
| 15 | RESERVED |        |        |        |        |        |         |           |        |         |         | VAA_PIX  | 34 |
| 16 | VAA      |        |        |        |        |        |         |           |        |         |         | AGND     | 33 |
| 17 | AGND     |        |        |        |        |        |         |           |        |         |         | DGND     | 32 |
| 18 | DGND     |        |        |        |        |        |         |           |        |         |         | VDD      | 31 |
|    | VDD      | VDD_IO | FLASH  | DGND   | SDATA  | SADDR  | SCLK    | RESET_BAR | OE_BAR | TRIGGER | SHUTTER | VDD_IO   |    |
|    | 19       | 20     | 21     | 22     | 23     | 24     | 25      | 26        | 27     | 28      | 29      | 30       |    |

TOP SIDE VIEW

**Table 4: mPLCC Pin Out**

| Pin | Name      | Type   | Description   |
|-----|-----------|--------|---|
| 1   | SLVSCN    | Output | HiSPi serial DDR clock differential N   |
| 2   | SLVS1P    | Output | HiSPi serial data, lane 1, differential P   |
| 3   | SLVS1N    | Output | HiSPi serial data, lane 1, differential N   |
| 4   | SLVS0P    | Output | HiSPi serial data, lane 0, differential P   |
| 5   | SLVS0N    | Output | HiSPi serial data, lane 0, differential N   |
| 6   | VDD_SLVS  | Power  | 0.3V-0.6V or 1.7V-1.9V to HiSPi Output Driver. Set the High_VCM (R0x306E[9]) bit to 1 when configuring VDD_SLVS to 1.7-1.9V |
| 7   | DGND      | Power  | Digital ground  |
| 8   | VDD_PLL   | Power  | PLL power   |
| 9   | EXTCLK    | Input  | External input clock  |
| 10  | VAA       | Power  | Analog Power  |
| 11  | AGND      | Power  | Analog Ground   |
| 12  | VDD_IO    | Power  | I/O Power Supply  |
| 13  | VDD       | Power  | Digital Power   |
| 14  | DGND      | Power  | Digital ground  |
| 15  | Reserved  |        |   |
| 16  | VAA       | Power  | Analog Power  |
| 17  | AGND      | Power  | Analog Ground   |
| 18  | DGND      | Power  | Digital ground  |
| 19  | VDD       | Power  | Digital Power   |
| 20  | VDD_IO    | Power  | I/O Power Supply  |
| 21  | FLASH     | Output | Flash control output  |
| 22  | TEST      | Input  | Manufacturing test enable pin (connect to DGNG)   |
| 23  | SDATA     | I/O    | Two-Wire Serial data I/O  |
| 24  | SADDR     | Input  | Two-Wire Serial address select. 0: 0x20, 1: 0x30  |
| 25  | SCLK      | Input  | Two-Wire Serial clock input   |
| 26  | RESET_BAR | Input  | Asynchronous reset (active LOW). All settings are restored to factory default   |
| 27  | OE_BAR    | Input  | Output enable (active LOW)  |
| 28  | TRIGGER   | Input  | Exposure synchronization input  |
| 29  | SHUTTER   | Output | Control for external mechanical shutter. Can be left floating if not used.  |
| 30  | VDD_IO    | Power  | I/O Power Supply  |
| 31  | VDD       | Power  | Digital Power   |
| 32  | DGND      | Power  | Digital ground  |
| 33  | AGND      | Power  | Analog Ground   |
| 34  | VAA_PIX   | Power  | Pixel Power   |
| 35  | VAA       | Power  | Analog Power  |
| 36  | Reserved  |        |   |
| 37  | VAA       | Power  | Analog Power  |

**Table 4: mPLCC Pin Out**

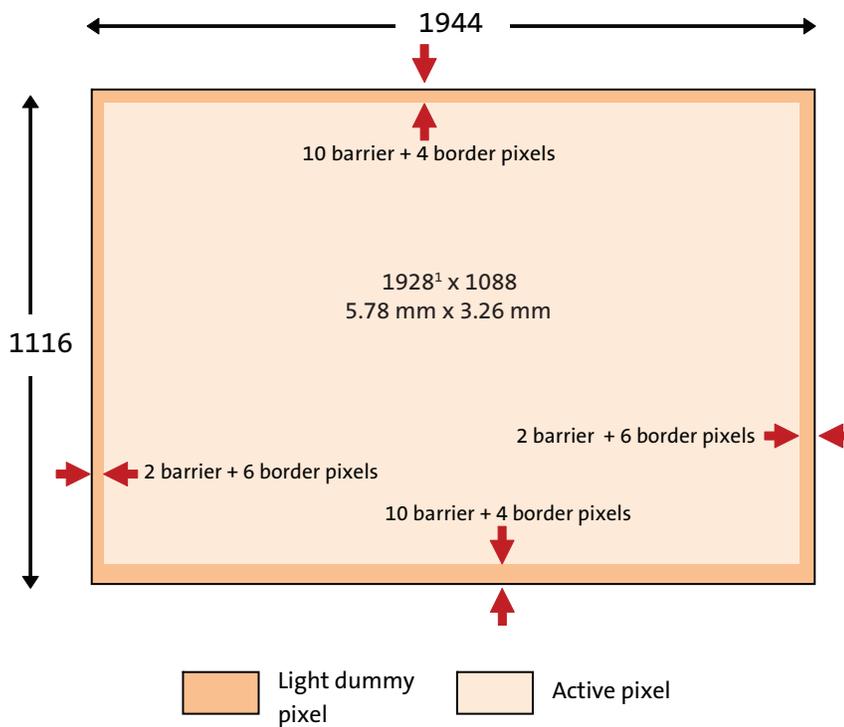
|    |         |        |   |
|----|---------|--------|---|
| 38 | VAA_PIX | Power  | Pixel Power                               |
| 39 | AGND    | Power  | Analog Ground                             |
| 40 | DGND    | Power  | Digital ground                            |
| 41 | VDD     | Power  | Digital Power                             |
| 42 | VDD_IO  | Power  | I/O Power Supply                          |
| 43 | VDD     | Power  | Digital Power                             |
| 44 | SLSV3P  | Output | HiSPi serial data, lane 3, differential P |
| 45 | SLVS3N  | Output | HiSPi serial data, lane 3, differential N |
| 46 | SLVS2P  | Output | HiSPi serial data, lane 2, differential P |
| 47 | SLVS2N  | Output | HiSPi serial data, lane 2, differential N |
| 48 | SLVSLCP | Output | HiSPi serial DDR clock differential P     |

## Pixel Data Format

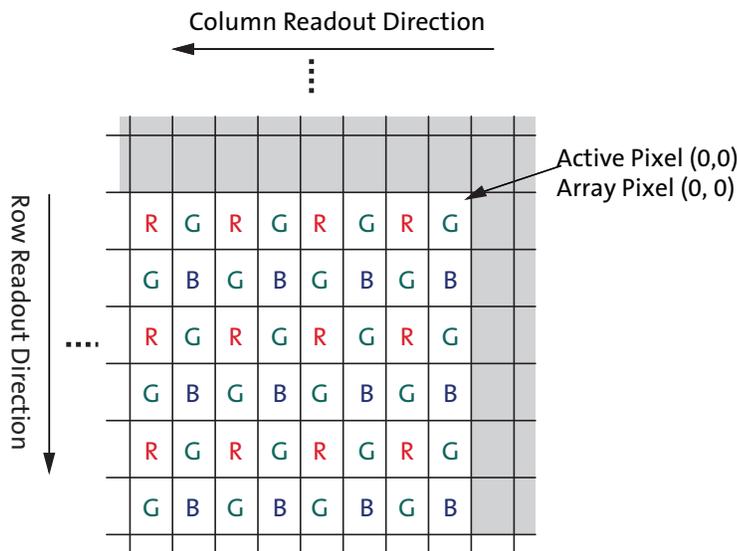
### Pixel Array Structure

While the sensor's format is 1928 x1088, additional active columns and active rows are included for use when horizontal or vertical mirrored readout is enabled, to allow readout to start on the same pixel. The pixel adjustment is always performed for mono-chrome or color versions. The active area is surrounded with optically transparent dummy pixels to improve image uniformity within the active area. Not all dummy pixels or barrier pixels can be read out.

Figure 6: Pixel Array Description



**Figure 7: Pixel Color Pattern Detail (Top Right Corner)**

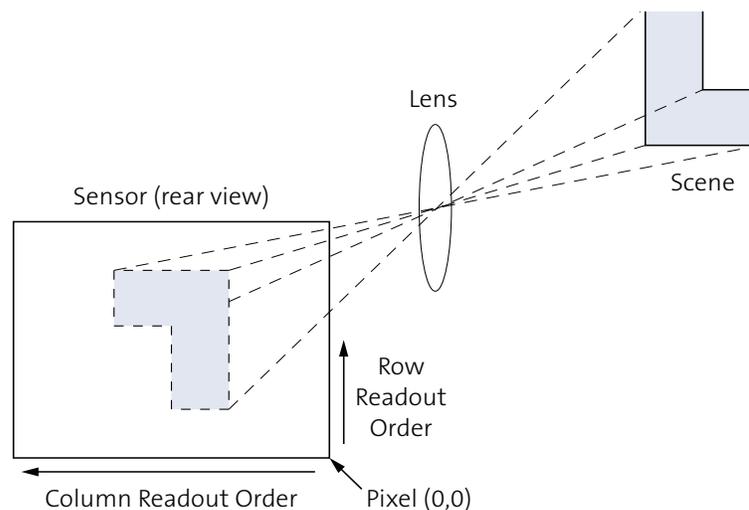


**Default Readout Order**

By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner (see Figure 7). This reflects the actual layout of the array on the die. Also, the first pixel data read out of the sensor in default condition is that of pixel (10, 14).

When the sensor is imaging, the active surface of the sensor faces the scene as shown in Figure 8. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced as shown in Figure 8.

**Figure 8: Imaging a Scene**



## Features Overview

For a complete description, recommendations, and usage guidelines for product features, refer to the AR0237 Developer Guide.

### 3.0 $\mu$ m Dual Conversion Gain Pixel

To improve the low light performance and keep the high dynamic range, a large (3.0 $\mu$ m) dual conversion gain pixel is implemented for better image optimization. With a dual conversion gain pixel, the conversion gain of the pixel may be dynamically changed to better adapt the pixel response based on dynamic range of the scene.

### HDR

By default, the sensor powers up in Linear Mode. One can change to HDR Mode. The HDR scheme used is multi-exposure HDR. This allows the sensor to handle up to 96 dB of dynamic range. In HDR mode, the sensor sequentially captures two exposures by maintaining two separate read and reset pointers that are interleaved within the rolling shutter readout. The exposure ratio may be set to 4x, 8x, 16x, or 32x. Sensor also provides flexibility to choose any exposure ratio by setting number of t2 exposure rows independent of the t1 exposure. The data will be output as line interleaved data as described in the T1/T2 Line Interleaved Mode section. There is also an option to output either T1 only or T2 only.

### Resolution

The active array supports a maximum of 1928x1088 pixels to support 1080p resolution. Utilizing a 3.0 $\mu$ m pixel will result in an optical format of 1/2.7-inch (approximately 6.6mm diagonal).

### Frame Rate

At full (1080p) resolution, the AR0237 is capable of running up to 60 fps in linear mode and 30 fps in line interleaved mode.

### Image Acquisition Mode

The AR0237 supports two image acquisition modes:

- Electronic rolling shutter (ERS) mode

This is the normal mode of operation. When the AR0237 is streaming, it generates frames at a fixed rate, and each frame is integrated (exposed) using the ERS. When ERS mode is in use, timing and control logic within the sensor sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and subsequently reading that row, the pixels in the row integrate incident light. The integration (exposure) time is controlled by varying the time between row reset and row readout. For each row in a frame, the time between row reset and row readout is the same, leading to a uniform integration time across the frame. When the integration time is changed (by using the two-wire serial interface to change register settings), the timing and control logic controls the transition from old to new integration

time in such a way that the stream of output frames from the AR0237 switches cleanly from the old integration time to the new while only generating frames with uniform integration. See “Changes to Integration Time” in the AR0237 Register Reference.

- Global reset mode.

This mode can be used to acquire a single image at the current resolution. In this mode, the end point of the pixel integration time is controlled by an external electromechanical shutter, and the AR0237 provides control signals to interface to that shutter. The benefit of using an external electromechanical shutter is that it eliminates the visual artifacts associated with ERS operation. Visual artifacts arise in ERS operation, particularly at low frame rates, because an ERS image effectively integrates each row of the pixel array at a different point in time.

## Embedded Data and Statistics

The AR0237 has the capability to output image data and statistics embedded within the frame timing. There are two types of information embedded within the frame readout.

- Embedded Data:  
If enabled, these are displayed on the two rows immediately before the first active pixel row is displayed.
- Embedded Statistics:  
If enabled, these are displayed on the two rows immediately after the last active pixel row is displayed.

## Multi-Camera Synchronization

The AR0237 supports advanced line synchronization controls for multi-camera (stereo) support.

## Slave Mode

The slave mode feature of the AR0237 supports triggering the start of a frame readout from an input signal that is supplied from an external ASIC. The slave mode signal allows for precise control of frame rate and register change updates.

## Context Switching and Register Updates

The user has the option of using the highly configurable context memory, or a simplified implementation in which only a subset of registers is available for switching. The AR0237 supports a highly configurable context switching RAM of size 256 x 16. Within this Context Memory, changes to any register may be stored. The register set for each context must be the same, but the number of contexts and registers per context are limited only by the size of the context memory.

Alternatively, the user may switch between two predefined register sets A and B by writing to a context switch change bit. When the context switch is configured to context A the sensor will reference the context A registers. If the context switch is changed from A to B during the readout of frame n, the sensor will then reference the context B coarse\_integration\_time registers in frame n+1 and all other context B registers at the beginning of reading frame n+2. The sensor will show the same behavior when changing from context B to context A. The registers listed in Table 5 are context-switchable:

**Table 5: List of Configurable Registers for Context A and Context B**

| Context A                | Context B                   |
|--------------------------|-----------------------------|
| Register Description     | Register Description        |
| coarse_integration_time  | coarse_integration_time_cb  |
| line_length_pck          | line_length_pck_cb          |
| frame_length_lines       | frame_length_lines_cb       |
| row_bin                  | row_bin_cb                  |
| col_bin                  | col_bin_cb                  |
| fine_gain                | fine_gain_cb                |
| coarse_gain              | coarse_gain_cb              |
| coarse_integration_time2 | coarse_integration_time2_cb |
| dcg_manual_set           | dcg_manual_set_cb           |
| dcg_manual_set_t1        | dcg_manual_set_t1_cb        |
| bypass_pix_comb          | bypass_pix_cb               |
| coarse_gain_t1           | coarse_gain_t1_cb           |
| fine_gain_t1             | fine_gain_t1_cb             |
| x_addr_start             | x_addr_start_cb             |
| y_addr_start             | y_addr_start_cb             |
| x_addr_end               | x_addr_end_cb               |
| y_addr_end               | y_addr_end_cb               |
| y_odd_inc                | y_odd_inc_cb                |
| x_odd_inc                | x_odd_inc_cb                |
| green1_gain              | green1_gain_cb              |
| blue_gain                | blue_gain_cb                |
| red_gain                 | red_gain_cb                 |
| green2_gain              | green2_gain_cb              |
| global_gain              | global_gain_cb              |
| operation_mode_ctrl      | operation_mode_ctrl_cb      |
| bypass_pix_comb          | bypass_pix_comb_cb          |

## Analog/Digital Gains

A programmable analog gain of 1.0x to 16x (linear and HDR) applied simultaneously to all color channels will be featured along with a digital gain of 1x to 16x that may be configured on a per color channel basis. Analog gain can be applied per exposure in line interleaved mode.

## Skipping/Binning Modes

The AR0237 supports subsampling. Subsampling allows the sensor to read out a smaller set of active pixels by either skipping, binning, or summing pixels within the readout window. Horizontal binning is achieved in the digital readout. The sensor will sample the combined 2x adjacent pixels within the same color plane. Vertical row binning is applied in the pixel readout. Row binning can be configured as 2x rows within the same color plane. Pixel skipping can be configured up to 2x in both the x-direction and y-

direction. Skipping pixels in the x-direction will not reduce the row time. Skipping pixels in the y direction will reduce the number of rows from the sensor effectively reducing the frame time. Skipping will introduce image artifacts from aliasing.

The AR0237 supports row wise vertical binning. Row wise vertical summing is only supported in monochrome sensors.

## Clocking Options

The sensor contains a phase-locked loop (PLL) that is used for timing generation and control. The required VCO clock frequency is attained through the use of a pre-PLL clock divider followed by a multiplier. The PLL multiplier should be an even integer. If an odd integer (M) is programmed, the PLL will default to the lower (M-1) value to maintain an even multiplier value. The multiplier is followed by a set of dividers used to generate the output clocks required for the sensor array, the pixel analog and digital readout paths, and the output parallel and serial interfaces. Use of the PLL is required when using the HiSPi interface.

## Temperature Sensor

The AR0237 sensor has a built-in PTAT-based temperature sensor, accessible through registers, that is capable of measuring die junction temperature. The value read out from the temperature sensor register is an ADC output value that needs to be converted downstream to a final temperature value in degrees Celsius. Since the PTAT device characteristic response is quite linear in the temperature range of operation required, a simple linear function can be used to convert the ADC output value to the final temperature in degrees Celsius.

A single reference point will be made available via register read as well as a slope for back-calculating the junction temperature value. An error of +/-5% or better over the full specified operating range of the sensor is to be expected.

## Silicon / Firmware / Sequencer Revision Information

A revision register will be provided to read out (via I<sup>2</sup>C) silicon and sequencer/OTPM revision information. This will be helpful to distinguish among different lots of material if there are future OTPM or sequencer revisions.

## Lens Shading Correction

The latest lens shading correction algorithm will be included for potential low Z height applications.

## Compression

When the AR0237 is configured for linear mode operation, the sensor can optionally compress 12-bit data to 10-bit using A-law compression. The A-law compression is disabled by default.

## Packaging

The AR0237 will be offered in a 10x10 80-iBGA package (parallel and HiSPi) and a 11.43x11.43 48 pin mPLCC (HiSSPi) package.

## Parallel Interface

The parallel pixel data interface uses these output-only signals:

- FRAME\_VALID
- LINE\_VALID
- PIXCLK
- DOUT[11:0]

The parallel pixel data interface is disabled by default at power up and after reset. It can be enabled by programming R0x301A. When the parallel pixel data interface is in use, the serial data output signals can be left unconnected.

## High Speed Serial Pixel (HiSPi) Interface

The HiSPi interface supports three protocols, Streaming-S, Streaming-SP, and Packetized SP. The streaming protocols conform to a standard video application where each line of active or intra-frame blanking provided by the sensor is transmitted at the same length. The Packetized SP protocol will transmit only the active data ignoring line-to-line and frame-to-frame blanking data.

The HiSPi interface building block is a unidirectional differential serial interface with four data and one double data rate (DDR) clock lanes. One clock for every four serial data lanes is provided for phase alignment across multiple lanes. The AR0237 supports serial data widths of 10 or 12 bits on one, two, or four lanes. The specification includes a DLL to compensate for differences in group delay for each data lane. The DLL is connected to the clock lane and each data lane, which acts as a control master for the output delay buffers. Once the DLL has gained phase lock, each lane can be delayed in 1/8 unit interval (UI) steps. This additional delay allows the user to increase the setup or hold time at the receiver circuits and can be used to compensate for skew introduced in PCB design. Delay compensation may be set for clock and/or data lines in the hispi\_timing register R0x31C0. If the DLL timing adjustment is not required, the data and clock lane delay settings should be set to a default code of 0x0000 to reduce jitter, skew, and power dissipation.

## Sensor Control Interface

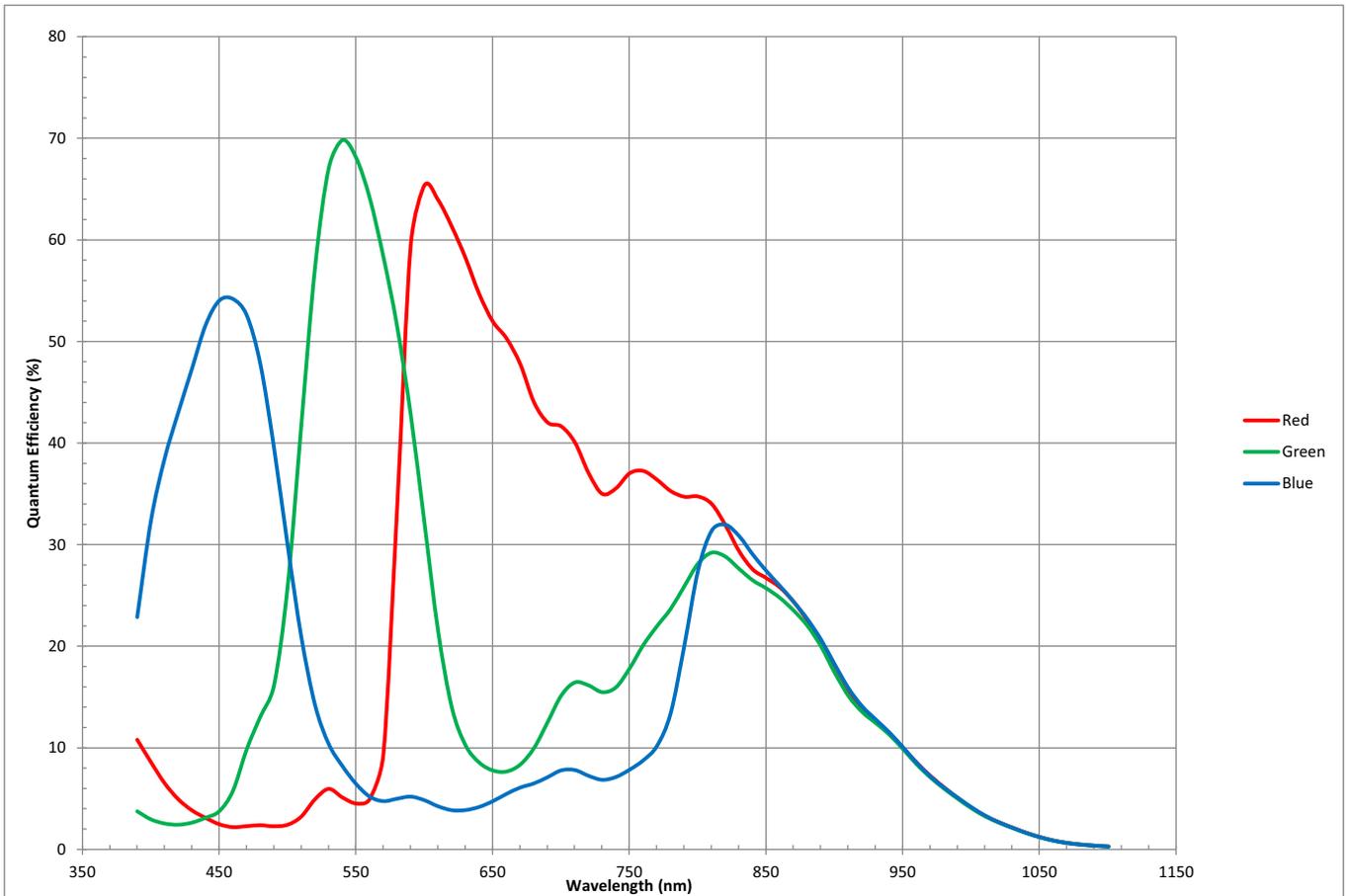
The two-wire serial interface bus enables read/write access to control and status registers within the AR0237. The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and is used to synchronize transfers.

Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD\_IO off-chip by a 1.5kΩ resistor. Either the slave or master device can drive SDATA LOW-the interface protocol determines which device is allowed to drive SDATA at any given time. The two-wire serial interface can run at 100 kHz or 400 kHz.

## T1/T2 Line Interleaved Mode

The AR0237 outputs the T1 and T2 exposures separately, in a line interleaved format. The purpose of this is to enable off chip HDR linear combination and processing. See the AR0237 Developer Guide for more information.

Figure 9: Quantum Efficiency



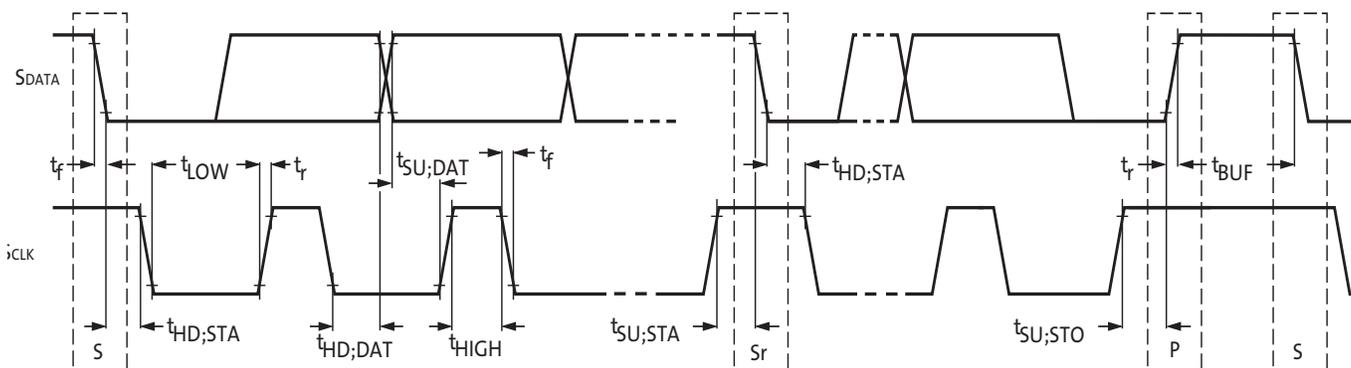
## Electrical Specifications

Unless otherwise stated, the following specifications apply under the following conditions:  $V_{DD} = 1.8V - 0.10/+0.15$ ;  $V_{DD\_IO} = V_{DD\_PLL} = V_{AA} = V_{AA\_PIX} = 2.8V \pm 0.3V$ ;  $V_{DD\_SLVS} = 0.4V - 0.1/+0.2$ ;  $T_A = -30^{\circ}C$  to  $+85^{\circ}C$ - $40^{\circ}C$  to  $+105^{\circ}C$ ; output load = 10pF; frequency = 74.25 MHz; HiSPi off.

### Two-Wire Serial Register Interface

The electrical characteristics of the two-wire serial register interface (SCLK, SDATA) are shown in Figure 10 and Table 6.

**Figure 10: Two-Wire Serial Bus Timing Parameters**



Note: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

**Table 6: Two-Wire Serial Bus Characteristics**

$f_{EXTCLK} = 27$  MHz;  $V_{DD} = 1.8V$ ;  $V_{DD\_IO} = 2.8V$ ;  $V_{AA} = 2.8V$ ;  $V_{AA\_PIX} = 2.8V$ ;  $V_{DD\_PLL} = 2.8V$ ;  $T_A = 25^{\circ}C$

| Parameter   | Symbol       | Standard Mode  |                   | Fast Mode        |                  | Unit    |
|---|--------------|----------------|-------------------|------------------|------------------|---------|
|   |              | Min            | Max               | Min              | Max              |         |
| SCLK Clock Frequency  | $f_{SCLK}$   | 0              | 100               | 0                | 400              | KHz     |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated | $t_{HD;STA}$ | 4.0            | -                 | 0.6              | -                | $\mu s$ |
| LOW period of the SCLK clock  | $t_{LOW}$    | 4.7            | -                 | 1.3              | -                | $\mu s$ |
| HIGH period of the SCLK clock   | $t_{HIGH}$   | 4.0            | -                 | 0.6              | -                | $\mu s$ |
| Set-up time for a repeated START condition  | $t_{SU;STA}$ | 4.7            | -                 | 0.6              | -                | $\mu s$ |
| Data hold time  | $t_{HD;DAT}$ | 0 <sup>4</sup> | 3.45 <sup>5</sup> | 0 <sup>6</sup>   | 0.9 <sup>5</sup> | $\mu s$ |
| Data set-up time  | $t_{SU;DAT}$ | 250            | -                 | 100 <sup>6</sup> | -                | ns      |
| Rise time of both SDATA and SCLK signals  | $t_r$        | -              | 1000              | $20 + 0.1Cb^7$   | 300              | ns      |
| Fall time of both SDATA and SCLK signals  | $t_f$        | -              | 300               | $20 + 0.1Cb^7$   | 300              | ns      |
| Set-up time for STOP condition  | $t_{SU;STO}$ | 4.0            | -                 | 0.6              | -                | $\mu s$ |
| Bus free time between a STOP and START condition  | $t_{BUF}$    | 4.7            | -                 | 1.3              | -                | $\mu s$ |
| Capacitive load for each bus line   | $C_b$        | -              | 400               | -                | 400              | pF      |

**Table 6: Two-Wire Serial Bus Characteristics (continued)**

$f_{EXTCLK} = 27 \text{ MHz}$ ;  $V_{DD} = 1.8\text{V}$ ;  $V_{DD\_IO} = 2.8\text{V}$ ;  $V_{AA} = 2.8\text{V}$ ;  $V_{AA\_PIX} = 2.8\text{V}$ ;  $V_{DD\_PLL} = 2.8\text{V}$ ;  $T_A = 25^\circ\text{C}$

| Parameter                              | Symbol   | Standard Mode |     | Fast Mode |     | Unit       |
|--|----------|---------------|-----|-----------|-----|------------|
|  |          | Min           | Max | Min       | Max |            |
| Serial interface input pin capacitance | CIN_SI   | -             | 3.3 | -         | 3.3 | pF         |
| SDATA max load capacitance             | CLOAD_SD | -             | 30  | -         | 30  | pF         |
| SDATA pull-up resistor                 | RSD      | 1.5           | 4.7 | 1.5       | 4.7 | K $\Omega$ |

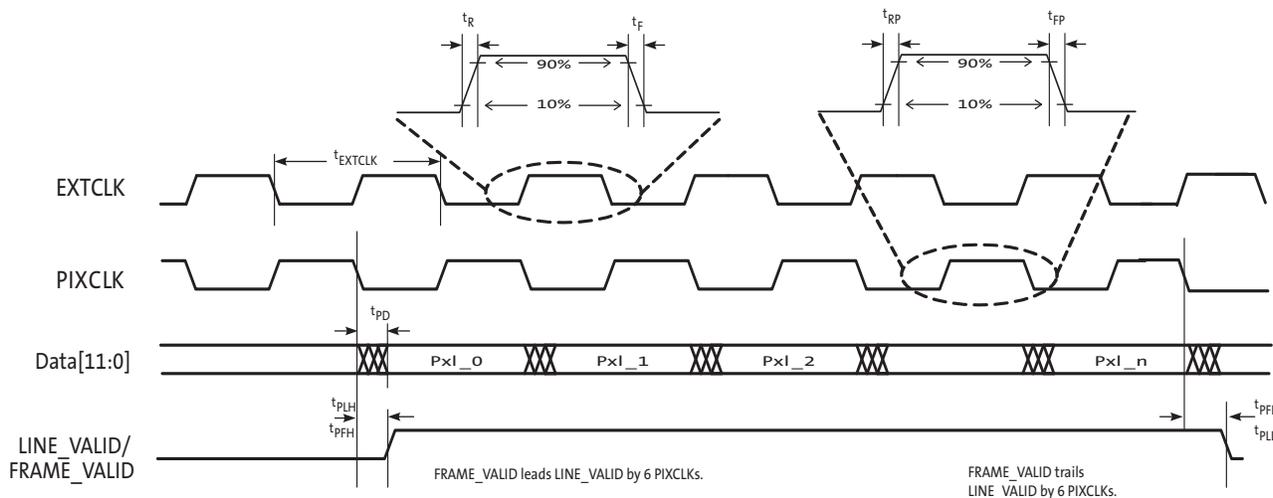
- Notes:
1. This table is based on I<sup>2</sup>C standard (v2.1 January 2000). Philips Semiconductor.
  2. Two-wire control is I<sup>2</sup>C-compatible.
  3. All values referred to  $V_{IHmin} = 0.9 V_{DD}$  and  $V_{ILmax} = 0.1V_{DD}$  levels. Sensor EXCLK = 27 MHz.
  4. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK.
  5. The maximum  $t_{HD;DAT}$  has only to be met if the device does not stretch the LOW period ( $t_{LOW}$ ) of the SCLK signal.
  6. A Fast-mode I<sup>2</sup>C-bus device can be used in a Standard-mode I<sup>2</sup>C-bus system, but the requirement  $t_{SU;DAT} \geq 250 \text{ ns}$  must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDATA line  $t_r \text{ max} + t_{SU;DAT} = 1000 + 250 = 1250 \text{ ns}$  (according to the Standard-mode I<sup>2</sup>C-bus specification) before the SCLK line is released.
  7.  $C_b$  = total capacitance of one bus line in pF.

## I/O Timing

By default, the AR0237 launches pixel data, FV, and LV with the falling edge of PIXCLK. The expectation is that the user captures DOUT[11:0], FV, and LV using the rising edge of PIXCLK.

See Figure 11 below and Table 7 on page 23 for I/O timing (AC) characteristics.

**Figure 11: I/O Timing Diagram**



**Table 7: I/O Timing Characteristics**

| Symbol         | Definition                         | Condition                      | Min  | Typ | Max   | Unit |
|----------------|------------------------------------|--------------------------------|------|-----|-------|------|
| $f_{EXTCLK1s}$ | Input clock frequency              |                                | 6    | –   | 48    | MHz  |
| $t_{EXTCLK1}$  | Input clock period                 |                                | 20.8 | –   | 166   | ns   |
| $t_R$          | Input clock rise time              |                                | –    | 3   | –     | ns   |
| $t_F$          | Input clock fall time              |                                | –    | 3   | –     | ns   |
| $t_{RP}$       | Pixclk rise time                   |                                | 2    | 3.5 | 5     | ns   |
| $t_{FP}$       | Pixclk fall time                   |                                | 2    | 3.5 | 5     | ns   |
|                | Clock duty cycle                   |                                | 45   | 50  | 55    | %    |
| $t_{CP}$       | EXTCLK to PIXCLK propagation delay | Nominal voltages, PLL Disabled | 10   | 14  | 18    | ns   |
| $f_{PIXCLK}$   | PIXCLK frequency                   | Default, Nominal Voltages      | 6    | –   | 74.25 | MHz  |
| $t_{PD}$       | PIXCLK to data valid               | Default, Nominal Voltages      | –    | 3   | –     | ns   |
| $t_{PFH}$      | PIXCLK to FV HIGH                  | Default, Nominal Voltages      | –    | 3   | –     | ns   |
| $t_{PLH}$      | PIXCLK to LV HIGH                  | Default, Nominal Voltages      | –    | 3   | –     | ns   |
| $t_{PFL}$      | PIXCLK to FV LOW                   | Default, Nominal Voltages      | –    | 3   | –     | ns   |
| $t_{PLL}$      | PIXCLK to LV LOW                   | Default, Nominal Voltages      | –    | 3   | –     | ns   |
| CLOAD          | Output load capacitance            |                                | –    | <10 | –     | pF   |
| CIN            | Input pin capacitance              |                                | –    | 2.5 | –     | pF   |

Note: I/O timing characteristics are measured under the following conditions:  
 - Temperature is 25°C ambient  
 - 10 pF load  
 - 1.8V I/O supply voltage

## DC Electrical Characteristics

The DC electrical characteristics are shown in the tables below.

**Table 8: DC Electrical Characteristics**

| Symbol   | Definition            | Condition  | Min                    | Typ     | Max                    | Unit |
|----------|-----------------------|--|------------------------|---------|------------------------|------|
| VDD      | Core digital voltage  |  | 1.7                    | 1.8     | 1.95                   | V    |
| VDD_IO   | I/O digital voltage   |  | 1.7/2.5                | 1.8/2.8 | 1.9/3.1                | V    |
| VAA      | Analog voltage        |  | 2.5                    | 2.8     | 3.1                    | V    |
| VAA_PIX  | Pixel supply voltage  |  | 2.5                    | 2.8     | 3.1                    | V    |
| VDD_PLL  | PLL supply voltage    |  | 2.5                    | 2.8     | 3.1                    | V    |
| VDD_SLVS | HiSPi supply voltage  |  | 0.3                    | 0.4     | 0.6                    | V    |
| VIH      | Input HIGH voltage    |  | $V_{DD\_IO} \cdot 0.7$ | –       | –                      | V    |
| VIL      | Input LOW voltage     |  | –                      | –       | $V_{DD\_IO} \cdot 0.3$ | V    |
| IIN      | Input leakage current | No pull-up resistor; $V_{IN} = V_{DD\_IO}$ or DGND | 20                     | –       | –                      | μA   |
| VOH      | Output HIGH voltage   |  | $V_{DD\_IO} - 0.3$     | –       | –                      | V    |
| VOL      | Output LOW voltage    |  | –                      | –       | 0.4                    | V    |
| IOH      | Output HIGH current   | At specified VOH                                   | -22                    | –       | –                      | mA   |
| IOL      | Output LOW current    | At specified VOL                                   | –                      | –       | 22                     | mA   |

**Caution** Stresses greater than those listed in Table 9 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**Table 9: Absolute Maximum Ratings**

| Symbol       | Definition                | Condition | Min  | Max | Unit |
|--------------|---------------------------|-----------|------|-----|------|
| VDD_MAX      | Core digital voltage      |           | -0.3 | 2.4 | V    |
| VDD_IO_MAX   | I/O digital voltage       |           | -0.3 | 4   | V    |
| VAA_MAX      | Analog voltage            |           | -0.3 | 4   | V    |
| VAA_PIX      | Pixel supply voltage      |           | -0.3 | 4   | V    |
| VDD_PLL      | PLL supply voltage        |           | -0.3 | 4   | V    |
| VDD_SLVS_MAX | HiSPi I/O digital voltage |           | -0.3 | 2.4 | V    |
| $t_{ST}$     | Storage temperature       |           | -40  | 85  | °C   |

Note: Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 10: 1080p30 Linear 74 MHz Parallel 2.8V**

| Definition                    | Condition         | Symbol  | Voltage      | Min   | Typ    | Max   | Unit |
|-------------------------------|-------------------|---------|--------------|-------|--------|-------|------|
| Digital operating current     | Streaming 1080p30 | IDD     | 1.8          | 20    | 34     | 50    | mA   |
| I/O digital operating current | Streaming 1080p30 | IDD_IO  | 2.8          | 15    | 28     | 50    | mA   |
| Analog operating current      | Streaming 1080p30 | IAA     | 2.8          | 15    | 26     | 50    | mA   |
| Pixel supply current          | Streaming 1080p30 | IAA_PIX | 2.8          | 1     | 3      | 7     | mA   |
| PLL supply current            | Streaming 1080p30 | IDD_PLL | 2.8          | 5.5   | 6.4    | 7     | mA   |
|                               |                   |         | <b>Power</b> | 138.2 | 238.72 | 409.2 | mW   |

Note: Operating currents are measured in mA at the following conditions:  
 - VAA = VAA\_PIX = VDD\_PLL = VDD\_IO = 2.8 V  
 - VDD = 1.8 V  
 - PLL Enabled and PIXCLK = 74.25 MHz  
 - Low power mode enabled  
 - TA = 25°C

**Table 11: 1080p30 Linear 74 MHz Parallel 1.8V**

| Definition                    | Condition         | Symbol  | Voltage      | Min   | Typ    | Max   | Unit |
|-------------------------------|-------------------|---------|--------------|-------|--------|-------|------|
| Digital operating current     | Streaming 1080p30 | IDD     | 1.8          | 20    | 34     | 50    | mA   |
| I/O digital operating current | Streaming 1080p30 | IDD_IO  | 1.8          | 10    | 14     | 30    | mA   |
| Analog operating current      | Streaming 1080p30 | IAA     | 2.8          | 15    | 26     | 50    | mA   |
| Pixel supply current          | Streaming 1080p30 | IAA_PIX | 2.8          | 1     | 3      | 7     | mA   |
| PLL supply current            | Streaming 1080p30 | IDD_PLL | 2.8          | 5.5   | 6.4    | 7     | mA   |
|                               |                   |         | <b>Power</b> | 114.2 | 185.52 | 323.2 | mW   |

Note: Operating currents are measured in mA at the following conditions:  
 - VAA = VAA\_PIX = VDD\_PLL = 2.8 V  
 - VDD = VDD\_IO = 1.8 V  
 - PLL Enabled and PIXCLK = 74.25 MHz  
 - Low power mode enabled  
 - TA = 25°C Dark Image, 8x Analog Gain, HCG, 20ms integration time

**Table 12: 1080p30 Linear 74 MHz HiSPi SLVS**

| Definition                | Condition         | Symbol   | Voltage | Min | Typ   | Max | Unit |
|---------------------------|-------------------|----------|---------|-----|-------|-----|------|
| Digital Operating Current | Streaming 1080p30 | IDD      | 1.8     | 25  | 44    | 65  | mA   |
| Analog Operating Current  | Streaming 1080p30 | IAA      | 2.8     | 15  | 26    | 50  | mA   |
| Pixel Supply Current      | Streaming 1080p30 | IAA_PIX  | 2.8     | 1   | 3     | 7   | mA   |
| PLL Supply Current        | Streaming 1080p30 | IDD_PLL  | 2.8     | 6   | 7.5   | 8.5 | mA   |
| SLVS Supply Current       | Streaming 1080p30 | IDD_SLVS | 0.4     | 6   | 9.5   | 14  | mA   |
|                           |                   |          | Power   | 109 | 185.2 | 306 | mW   |

Note: Operating currents are measured in mA at the following conditions:  
 - VAA = VAA\_PIX = VDD\_PLL = 2.8 V  
 - VDD = VDD\_IO = 1.8 V  
 - VDD\_SLVS = 0.4V  
 - PLL Enabled and PIXCLK = 74.25 MHz  
 - 4-lane HiSPi mode  
 - Low power mode enabled  
 - TA = 25°C Dark Image, 8x Analog Gain, HCG, 20ms integration time

**Table 13: 1080p30 Linear 74 MHz HiSPi HiVcm**

| Definition                | Condition         | Symbol   | Voltage | Min   | Typ   | Max   | Unit |
|---------------------------|-------------------|----------|---------|-------|-------|-------|------|
| Digital Operating Current | Streaming 1080p30 | IDD      | 1.8     | 25    | 44    | 65    | mA   |
| Analog Operating Current  | Streaming 1080p30 | IAA      | 2.8     | 15    | 26    | 50    | mA   |
| Pixel Supply Current      | Streaming 1080p30 | IAA_PIX  | 2.8     | 1     | 3     | 7     | mA   |
| PLL Supply Current        | Streaming 1080p30 | IDD_PLL  | 2.8     | 6     | 7.5   | 8.5   | mA   |
| SLVS Supply Current       | Streaming 1080p30 | IDD_SLVS | 1.8     | 12    | 20    | 35    | mA   |
|                           |                   |          | Power   | 128.2 | 217.4 | 363.4 | mW   |

Note: Operating currents are measured in mA at the following conditions:  
 - VAA = VAA\_PIX = VDD\_PLL = 2.8 V  
 - VDD = VDD\_IO = VDD\_SLVS = 1.8 V  
 - PLL Enabled and PIXCLK = 74.25 MHz  
 - 4-lane HiSPi mode  
 - Low power mode enabled  
 - TA = 25°C Dark Image, 8x Analog Gain, HCG, 20ms integration time

**Table 14: 1080p30 74 MHz Line Interleaved SLVS**

| Definition                | Condition         | Symbol   | Voltage      | Min   | Typ | Max   | Unit |
|---------------------------|-------------------|----------|--------------|-------|-----|-------|------|
| Digital Operating Current | Streaming 1080p30 | IDD      | 1.8          | 50    | 88  | 130   | mA   |
| Analog Operating Current  | Streaming 1080p30 | IAA      | 2.8          | 20    | 36  | 60    | mA   |
| Pixel Supply Current      | Streaming 1080p30 | IAA_PIX  | 2.8          | 1     | 4   | 8     | mA   |
| PLL Supply Current        | Streaming 1080p30 | IDD_PLL  | 2.8          | 7     | 8.5 | 9.5   | mA   |
| SLVS Supply Current       | Streaming 1080p30 | IDD_SLVS | 0.4          | 6     | 9.5 | 14    | mA   |
|                           |                   |          | <b>Power</b> | 170.8 | 298 | 442.6 | mW   |

Note: Operating currents are measured in mA at the following conditions:  
 - VAA = VAA\_PIX = VDD\_PLL = 2.8 V  
 - VDD = VDD\_IO = 1.8 V  
 - VDD\_SLVS = 0.4V  
 - PLL Enabled and PIXCLK = 74.25 MHz  
 - 4-lane HiSPi mode  
 - TA = 25°C Dark Image, 8x Analog Gain, HCG, 20ms integration time

**Table 15: 1080p30 74 MHz Line Interleaved HiVcm**

| Definition                | Condition         | Symbol   | Voltage      | Min | Typ   | Max | Unit |
|---------------------------|-------------------|----------|--------------|-----|-------|-----|------|
| Digital Operating Current | Streaming 1080p30 | IDD      | 1.8          | 50  | 88    | 130 | mA   |
| Analog Operating Current  | Streaming 1080p30 | IAA      | 2.8          | 20  | 36    | 60  | mA   |
| Pixel Supply Current      | Streaming 1080p30 | IAA_PIX  | 2.8          | 1   | 4     | 8   | mA   |
| PLL Supply Current        | Streaming 1080p30 | IDD_PLL  | 2.8          | 7   | 8.5   | 9.5 | mA   |
| SLVS Supply Current       | Streaming 1080p30 | IDD_SLVS | 1.8          | 12  | 20    | 35  | mA   |
|                           |                   |          | <b>Power</b> | 190 | 330.2 | 500 | mW   |

Note: Operating currents are measured in mA at the following conditions:  
 - VAA = VAA\_PIX = VDD\_PLL = 2.8 V  
 - VDD = VDD\_IO = 1.8 V  
 - VDD\_SLVS = 1.8 V  
 - PLL Enabled and PIXCLK = 74.25 MHz  
 - 4-lane HiSPi mode  
 - TA = 25°C Dark Image, 8x Analog Gain, HCG, 20ms integration time

## HiSPi Electrical Specifications

The ON Semiconductor AR0237 sensor supports both SLVS and HiVCM HiSPi modes. Refer to the High-Speed Serial Pixel (HiSPi) Interface Physical Layer Specification v2.00.00 for electrical definitions, specifications, and timing information. The VDD\_SLVS supply in this datasheet corresponds to VDD\_TX in the HiSPi Physical Layer Specification. Similarly, VDD is equivalent to VDD\_HiSPi as referenced in the specification. The DLL as implemented on AR0237 is limited in the number of available delay steps and differs from the HiSPi specification as described in this section.

**Table 16: Channel Skew**

Measurement Conditions: VDD\_HiSPi = 1.8V; VDD\_HiSPi\_TX = 0.4V; Data Rate = 480 Mbps; DLL set to 0

|                                      |             |      |    |
|--------------------------------------|-------------|------|----|
| Data Lane Skew in Reference to Clock | tCHSKEW1PHY | -150 | ps |
|--------------------------------------|-------------|------|----|

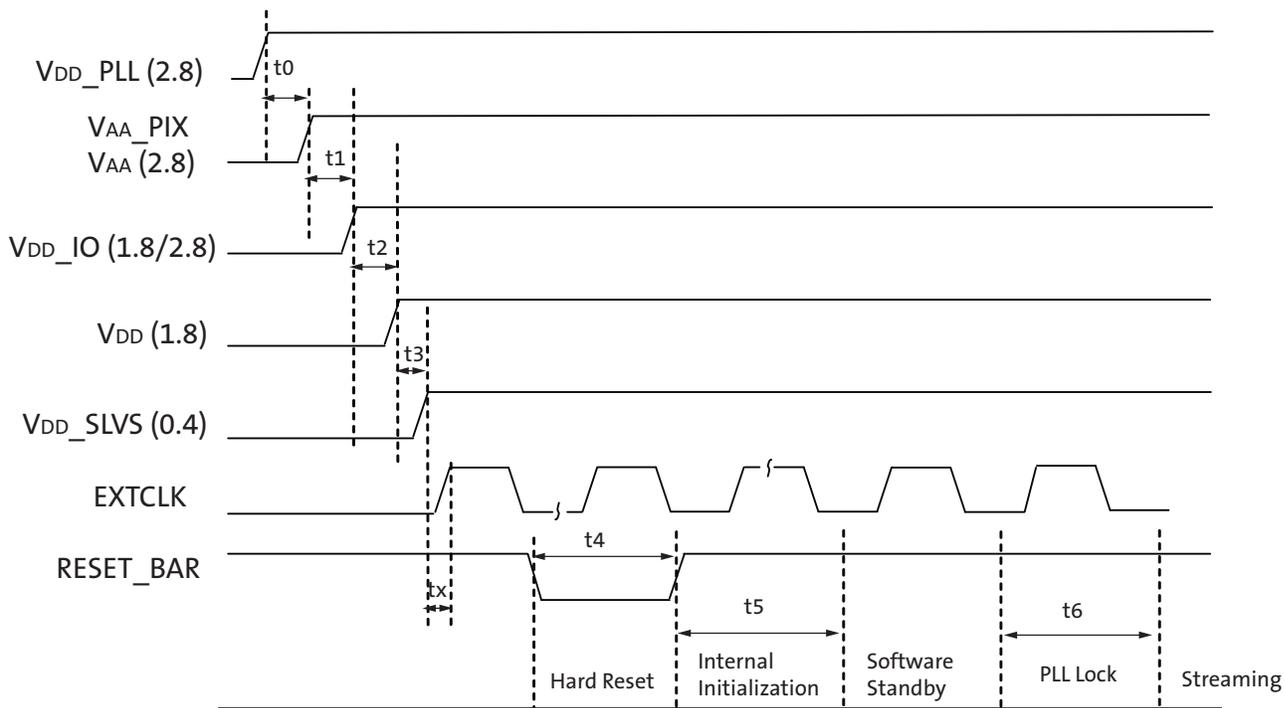
## Power-On Reset and Standby Timing

### Power-Up Sequence

The recommended power-up sequence for the AR0237 is shown in Figure 12. The available power supplies (VDD\_IO, VDD, VDD\_SLVS, VDD\_PLL, VAA, VAA\_PIX) must have the separation specified below.

1. Turn on VDD\_PLL power supply.
2. After 100μs, turn on VAA and VAA\_PIX power supply.
3. After 100μs, turn on VDD\_IO power supply.
4. After 100μs, turn on VDD power supply.
5. After 100μs, turn on VDD\_SLVS power supply.
6. After the last power supply is stable, enable EXTCLK.
7. Assert RESET\_BAR for at least 1ms. The parallel interface will be tri-stated during this time.
8. Wait 150000 EXTCLKs (for internal initialization into software standby).
9. Configure PLL, output, and image settings to desired values.
10. Wait 1ms for the PLL to lock.
11. Set streaming mode (R0x301a[2] = 1).

**Figure 12: Power Up**



**Table 17: Power-Up Sequence**

| Definition                          | Symbol | Minimum        | Typical         | Maximum | Unit    |
|-------------------------------------|--------|----------------|-----------------|---------|---------|
| VDD_PLL to VAA/VAA_PIX <sup>3</sup> | t0     | 0              | 100             | –       | μs      |
| VAA/VAA_PIX to VDD_IO               | t1     | 0              | 100             | –       | μs      |
| VDD_IO to VDD                       | t2     | 0              | 100             | –       | μs      |
| VDD to VDD_SLVS                     | t3     | 0              | 100             | –       | μs      |
| Xtal settle time                    | tx     | –              | 30 <sup>1</sup> | –       | ms      |
| Hard Reset                          | t4     | 1 <sup>2</sup> | –               | –       | ms      |
| Internal Initialization             | t5     | 150000         | –               | –       | EXTCLKs |
| PLL Lock Time                       | t6     | 1              | –               | –       | ms      |

- Notes:
1. Xtal settling time is component-dependent, usually taking about 10 – 100 ms.
  2. Hard reset time is the minimum time required after power rails are settled. In a circuit where Hard reset is held down by RC circuit, then the RC time must include the all power rail settle time and Xtal settle time.
  3. It is critical that VDD\_PLL is not powered up after the other power supplies. It must be powered before or at least at the same time as the others. If the case happens that VDD\_PLL is powered after other supplies then sensor may have functionality issues and will experience high current draw on this supply.

### Power-Down Sequence

The recommended power-down sequence for the AR0237 is shown in Figure 13. The available power supplies (VDD\_IO, VDD, VDD\_SLVS, VDD\_PLL, VAA, VAA\_PIX) must have the separation specified below.

1. Disable streaming if output is active by setting standby R0x301a[2] = 0
2. The soft standby state is reached after the current row or frame, depending on configuration, has ended.
3. Turn off VDD\_SLVS.
4. Turn off VDD.
5. Turn off VDD\_IO.
6. Turn off VAA/VAA\_PIX.
7. Turn off VDD\_PLL.

Figure 13: Power Down

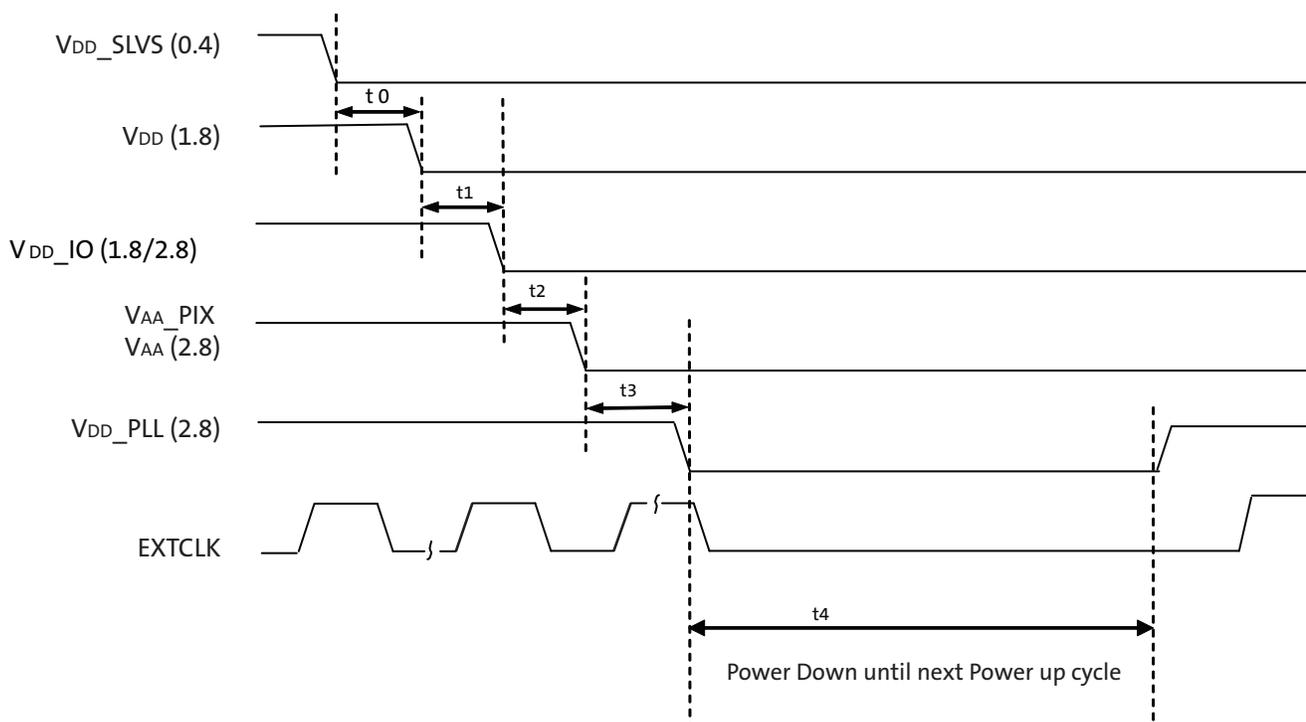


Table 18: Power-Down Sequence

| Definition                          | Symbol | Minimum | Typical | Maximum | Unit |
|-------------------------------------|--------|---------|---------|---------|------|
| VDD_SLVS to VDD                     | t0     | 0       | –       | –       | μs   |
| VDD to VDD_IO                       | t1     | 0       | –       | –       | μs   |
| VDD_IO to VAA/VAA_PIX               | t2     | 0       | –       | –       | μs   |
| VAA/VAA_PIX to VDD_PLL              | t3     | 0       | –       | –       | μs   |
| Power Down until Next Power Up Time | t4     | 100     | –       | –       | ms   |

t4 is required between power down and next power up time; all decoupling caps from regulators must be completely discharged.

## Package Diagrams

Figure 14: PLCC 48 11.43 x 11.43 Package Diagram (Case 776AQ)

PLCC48 11.43x11.43  
CASE 776AQ  
ISSUE A

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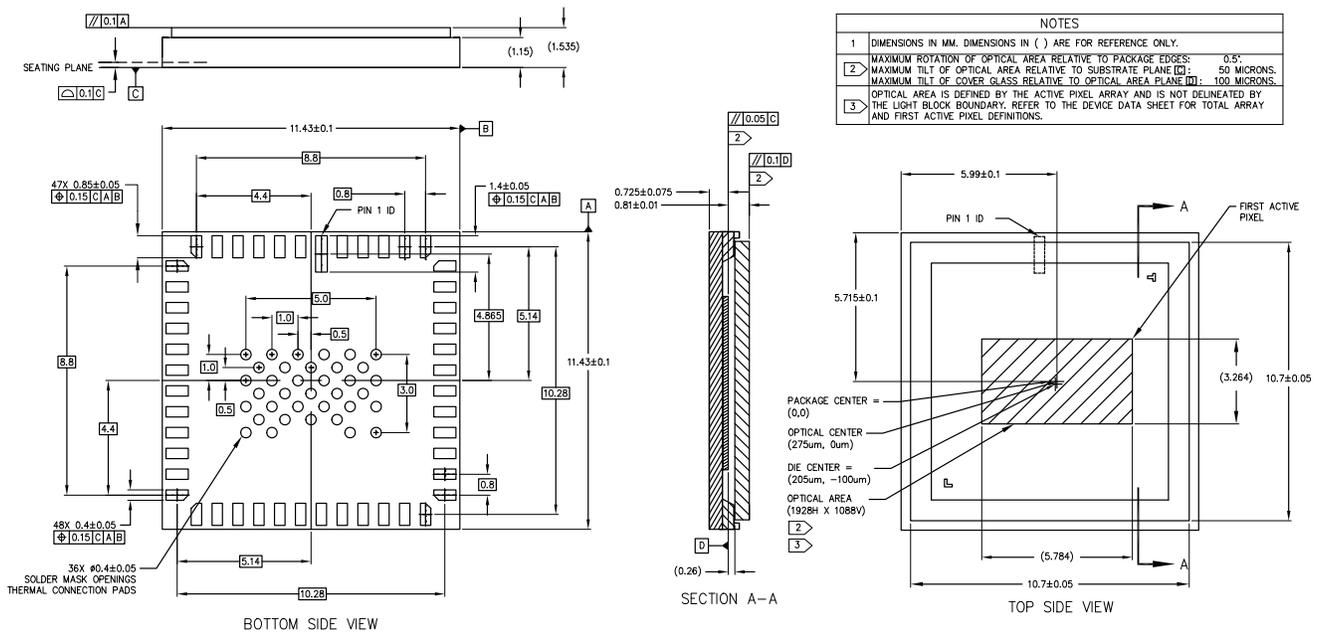
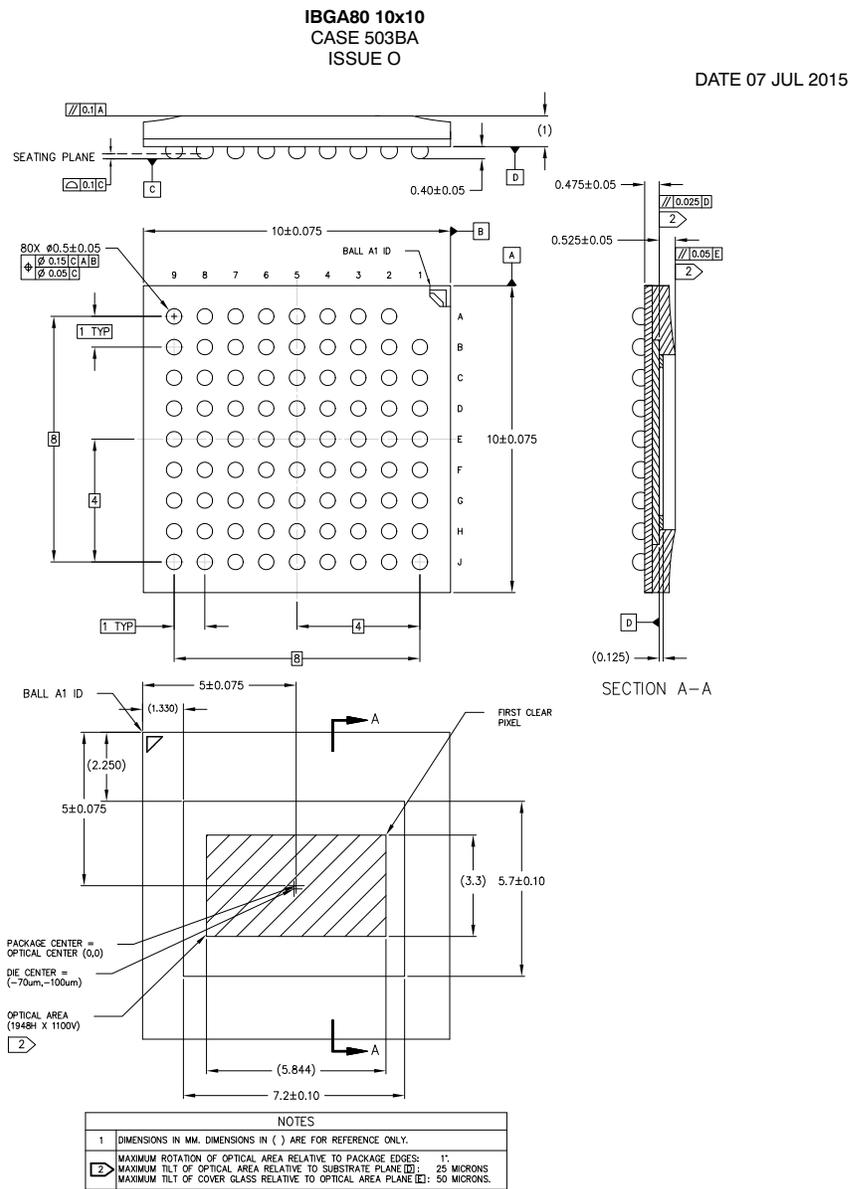


Figure 15: 80iBGA 10x10 Package Diagram (Case 503BA)





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