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NTE74C73, NTE74C76, NTE74C107
Integrated Circuit
TTL– CMOS Dual J–K Flip–Flops

Description:

These NTE dual J–K flip–flops are monolithic complementary MOS (CMOS) integrate circuits constructed with N– and P–channel enhancement transistors. Each flip–flop has independent J, K, clock and clear inputs and Q and $\overline{Q}$ outputs. The NTE74C76 flip–flop also includes preset inputs and is supplied in a 16–Lead DIP type package. These flip–flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulses. Clear or preset is independent of the clock and is accomplished by a low level on the respective input.

Features:

- Supply Voltage Range: 3V to 15V
- Tenth Power TTL Compatible: Drive 2 LPTTL Loads
- High Noise Immunity: 0.45 V_{CC} (Typ)
- Low Power Consumption: 50nW (Typ)
- Medium Speed Operation: 10Mhz (Typ) with 10V Supply

Applications:

- Automotive
- Data Terminals
- Instrumentation
- Medical Electronics
- Alarm Systems
- Industrial Electronics
- Remote Metering
- Computers

Function:

- NTE74C73 – Dual J–K Flip–Flop with Clear (14–Lead DIP)
- NTE74C76 – Dual J–K Flip–Flop with Clear and Preset (14–Lead DIP)
- NTE74C107 – Dual J–K Flip–Flop with Clear (16–Lead DIP)

Absolute Maximum Ratings: (Note 1)

Voltage at Any Pin (Note 2) . . . . . –0.3V to V_{CC} +0.3V
Operating V_{CC} Range . . . . . 3V to 15V
Maximum V_{CC} Voltage 16V
Package Dissipation 500mW
Operating Temperature Range . . . . . 0° to +70°C
Storage Temperature Range . . . . . –65° to +150°C

Note 1. “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. Except for “Operating Temperature Range” they are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” provides conditions for actual device operation.

Note 2. These devices should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

Electrical Characteristics:

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
CMOS to CMOS							
Logical “1” Input Voltage	$V_{IN(1)}$	V_{CC} = 5V		3.5	–	–	V
		V_{CC} = 10V		8.0	–	–	V
Logical “0” Input Voltage	$V_{IN(0)}$	V_{CC} = 5V		–	–	1.5	V
		V_{CC} = 10V		–	–	2.0	V
Logical “1” Output Voltage	$V_{OUT(1)}$	V_{CC} = 5V		4.5	–	–	V
		V_{CC} = 10V		9.0	–	–	V
Logical “0” Output Voltage	$V_{OUT(0)}$	V_{CC} = 5V		–	–	0.5	V
		V_{CC} = 10V		–	–	1.0	V
Logical “1” Input Current	$I_{IN(1)}$	V_{CC} = 15V		–	–	1.0	µA
Logical “0” Input Current	$I_{IN(0)}$	V_{CC} = 15V		–1.0	–	–	µA
Supply Current	I_{CC}	V_{CC} = 15V		–	0.05	60	µA
Propagation Delay Time to a Logical “0” or Logical “1” from Clock to Q or $\overline{Q}$	t_{pd0}, t_{pd1}	C_L = 50pF, T_A = +25°C	V_{CC} = 5V	–	180	300	ns
			V_{CC} = 10V	–	70	110	ns
Propagation Delay Time to a Logical “0” or Ligical “1” from Preset or Clear	t_{pd0}, t_{pd1}	C_L = 50pF, T_A = +25°C	V_{CC} = 5V	–	200	300	ns
			V_{CC} = 10V	–	80	130	ns
Time Prior to Clock Pulse that Data must be Present	t_{SETUP}	C_L = 50pF, T_A = +25°C	V_{CC} = 5V	–	110	175	ns
			V_{CC} = 10V	–	45	70	ns
Time After Clock Pulse that J and K must be Held	t_{HOLD}	C_L = 50pF, T_A = +25°C	V_{CC} = 5V	–	–40	0	ns
			V_{CC} = 10V	–	–20	0	ns
Minimum Clock Pulse Width	t_{WL} = t_{WH}	C_L = 50pF, T_A = +25°C	V_{CC} = 5V	–	120	190	ns
			V_{CC} = 10V	–	50	80	ns
Minimum Preset and Clear Pulse Width		C_L = 50pF, T_A = +25°C	V_{CC} = 5V	–	90	130	ns
			V_{CC} = 10V	–	40	60	ns
Maximum Toggle Frequency		C_L = 50pF, T_A = +25°C	V_{CC} = 5V	2.5	4.0	–	MHz
			V_{CC} = 10V	7.0	11.0	–	MHz
Clock Pulse Rise and Fall Time		C_L = 50pF, T_A = +25°C	V_{CC} = 5V	–	–	15	µs
			V_{CC} = 10V	–	–	5	µs
Low Power to CMOS							
Logical “1” Input Voltage	$V_{IN(1)}$	V_{CC} = 4.75V		V_{CC}–1.5	–	–	V
Logical “0” Input Voltage	$V_{IN(0)}$	V_{CC} = 4.75V		–	–	0.8	V
Logical “1” Output Voltage	$V_{OUT(1)}$	V_{CC} = 4.75V, I_O = –360µA		2.4	–	–	V
Logical “0” Output Voltage	$V_{OUT(0)}$	V_{CC} = 4.75V, I_O = 360µA		–	–	0.4	V
Propagation Delay Time to a Logical “0” or Logical “1” from Clock	t_{pd0}, t_{pd1}	V_{CC} = 5V, C_L = 50pF, T_A = +25°C		–	250	–	ns

Truth Table:

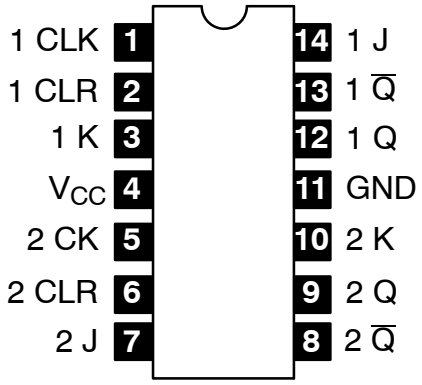
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

t_n = bit time before clock pulse

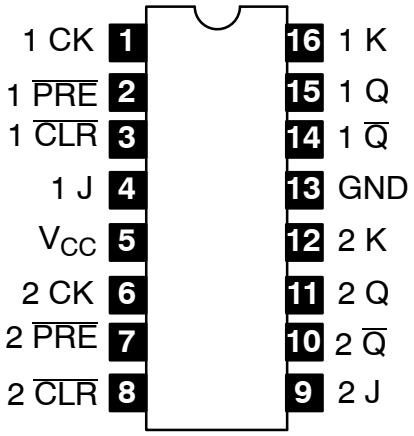
t_{n+1} = bit time after clock pulse

Pin Connection Diagram

NTE74C73



NTE74C76



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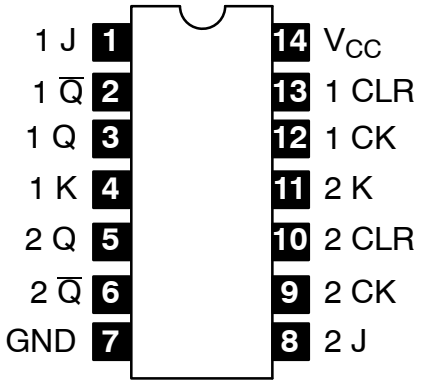

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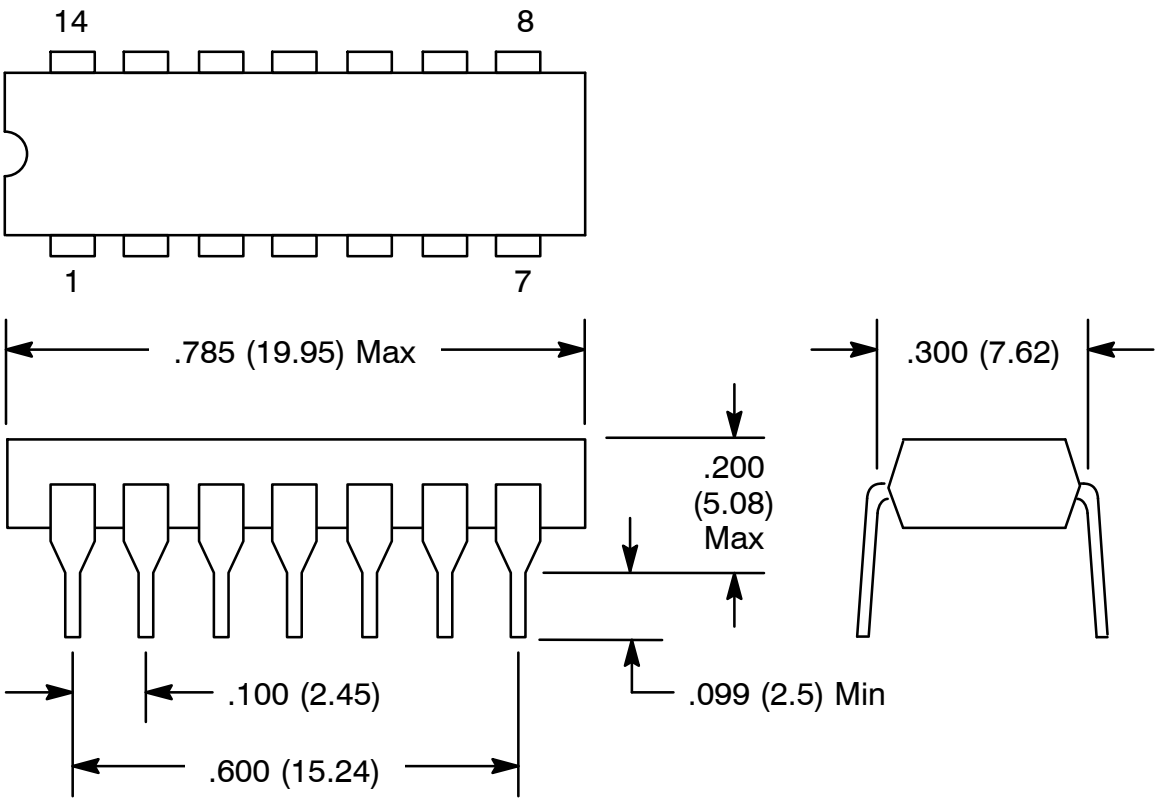
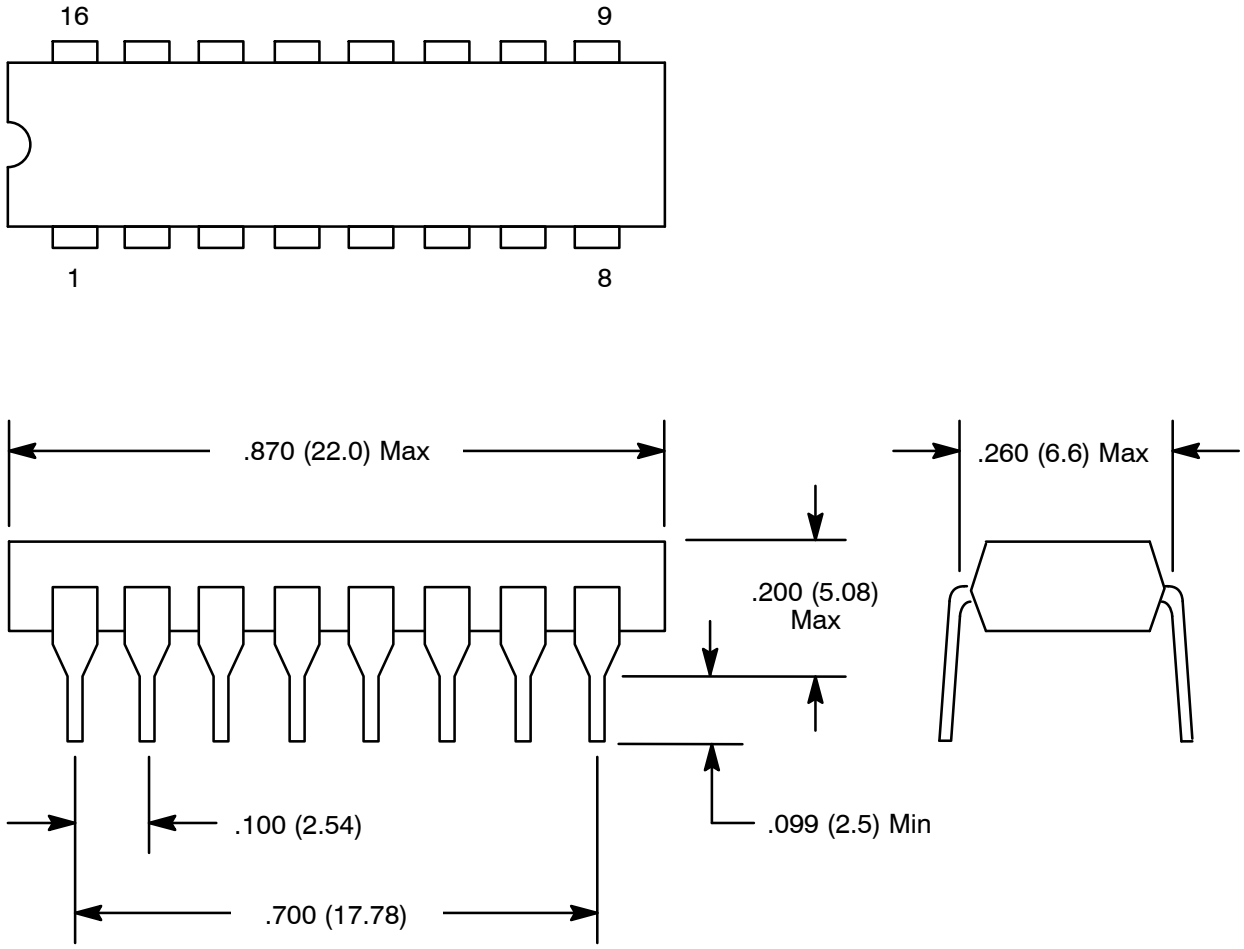


NTE74C76


16
9
1
8
.870 (22.0) Max
.260 (6.6) Max
.200 (5.08)
Max
.100 (2.54)
.099 (2.5) Min
.700 (17.78)