ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE74C30
Integrated Circuit
TTL– CMOS 8–Input Positive NAND Gate
14–Lead DIP

Description:

The NTE74C30 logic gate employs complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption and high noise immunity. Function and pin–out compatibility with series 74 devices minimizes design time for those designers familiar with the standard 74 logic family.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features:

- Wide Supply Range: 3V to 15V
- Guaranteed Noise Margin: 1.0V
- High Noise Immunity: 0.45 V_{CC} (typ)
- Low Power TTL Compatible: Fan Out of 2 Driving 74L

Absolute Maximum Ratings: (Note 1)

Voltage at Any Pin . . . . . –0.3V to V_{CC} +0.3V
Power Dissipation, P_D 500mW
Operating V_{CC} Range . . . . . 3V to 15V
Absolute Maximum V_{CC} Voltage 16V
Operating Temperature Range, T_A . . . . . –0° to +70°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 10sec), T_L . . . . . +300°C

Note 1. “Absolute Maximum Ratings” are those values beyond which th safety of the device cannot be guaranteed. Except for “Operating Temperature Range”, they are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” provides conditions for actual device operation.

DC Electrical Characteristics: (T_A = 0° to +70°C unless otherwise specified)

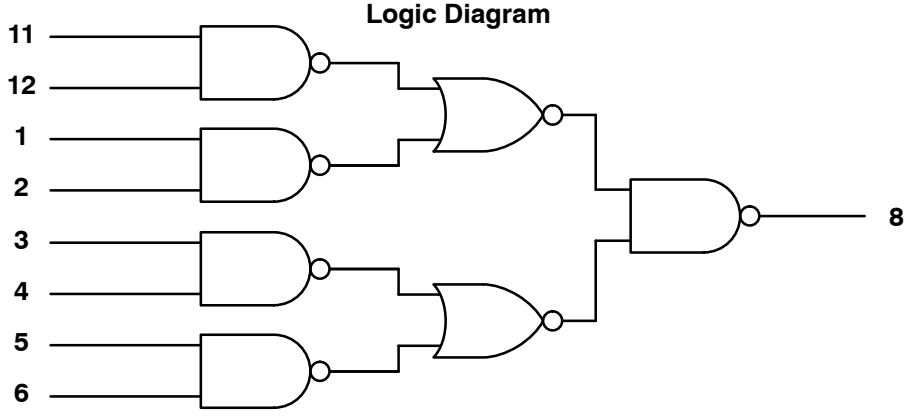
Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
CMOS to CMOS							
Logical “1” Input Voltage	$V_{IN(1)}$	V_{CC} = 5V		3.5	–	–	V
		V_{CC} = 10V		8.0	–	–	V
Logical “0” Input Voltage	$V_{IN(0)}$	V_{CC} = 5V		–	–	1.5	V
		V_{CC} = 10V		–	–	2.0	V
Logical “1” Output Voltage	$V_{OUT(1)}$	V_{CC} = 5V	I_O = −10μA	4.5	–	–	V
		V_{CC} = 10V		9.0	–	–	V
Logical “0” Output Voltage	$V_{OUT(0)}$	V_{CC} = 5V	I_O = 10μA	–	–	0.5	V
		V_{CC} = 10V		–	–	1.0	V
Logical “1” Input Current	$I_{IN(1)}$	V_{CC} = 15V, V_{IN} = 15V		–	0.005	1.0	μA
Logical “0” Input Current	$I_{IN(0)}$	V_{CC} = 15V, V_{IN} = 0V		–1.0	–0.005	–	μA
Supply Current	I_{CC}	V_{CC} = 15V		–	0.01	15	μA
CMOS/LPTTL Interface							
Logical “1” Input Voltage	$V_{IN(1)}$	V_{CC} = 4.75V		V_{CC}–1.5	–	–	V
Logical “0” Input Voltage	$V_{IN(0)}$	V_{CC} = 4.75V		–	–	0.8	V
Logical “1” Output Voltage	$V_{OUT(1)}$	V_{CC} = 4.75V, I_O = −360μA		2.4	–	–	V
Logical “0” Output Voltage	$V_{OUT(0)}$	V_{CC} = 4.75V, I_O = 360μA		–	–	0.4	V
Output Drive							
Output Source Current (P−Channel)	I_{SOURCE}	V_{CC} = 5V	V_{OUT} = 0, T_A = +25°C	–1.75	–3.3	–	mA
		V_{CC} = 10V		–8	–15	–	mA
Output Sink Current (N−Channel)	I_{SINK}	V_{CC} = 5V	V_{OUT} = V_{CC}, T_A = +25°C	1.75	3.6	–	mA
		V_{CC} = 10V		8	16	–	mA

AC Electrical Characteristics: (T_A = +25°, C_L = 50pF unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time to Logical “1” or Logical “0”	t_{pd}	V_{CC} = 5V	–	125	180	ns
		V_{CC} = 10V	–	55	90	ns
Input Capacitance	C_{IN}	Note 2	–	4	–	pF
Power Dissipation Capacitance	C_{pd}	Per Gate, Note 3	–	26	–	pF

Note 2. Capacitance is guaranteed by periodic testing.
Note 3. C_{pd} determines the no load AC power consumption of any CMOS device.

Logic Diagram



Pin Connection Diagram