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NTE74C175
Integrated Circuit
TTL– CMOS Quad D–Type Flip–Flop
w/Common Direct Clear and Complementary Outputs
16–Lead DIP

Description:

The NTE74C175 consists of four positive–edge triggered D–type flip–flops implemented with monolithic CMOS technology in a 16–Lead DIP type package. This device has a direct clear input and features complementary outputs from each flip–flop. All four flip–flops are controlled by a common clock and a common clear. Information at the D inputs meeting the set–up time requirements is transferred to the Q outputs on the positive–going edge of the clock pulse. The clearing operation, enabled by a negative pulse at Clear input, clears all four Q outputs to a logical “0” and Q’s to a logical “1”.

All inputs are protected from static discharge by diode clamps to V_{CC} and GND.

Features:

- Wide Supply Range: 3V to 15V
- Guaranteed Noise Margin: 1.0V
- High Noise Immunity: 0.45 V_{CC} (typ)
- Low Power TTL Compatible: Fan Out of 2 Driving 74L

Absolute Maximum Ratings: (Note 1)

Voltage at Any Pin . . . . . –0.3V to V_{CC} +0.3V
Power Dissipation, P_D 700mW
Operating V_{CC} Range . . . . . 3V to 15V
Maximum V_{CC} Voltage 18V
Operating Temperature Range, T_A . . . . . –40° to +85°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 10sec), T_L . . . . . +260°C

Note 1. “Absolute Maximum Ratings” are those values beyond which th safety of the device cannot be guaranteed. Except for “Operating Temperature Range”, they are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” provides conditions for actual device operation.

DC Electrical Characteristics: (T_A = −40° to +85°C unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
CMOS to CMOS							
Logical “1” Input Voltage	$V_{IN(1)}$	V_{CC} = 5V		3.5	–	–	V
		V_{CC} = 10V		8.0	–	–	V
Logical “0” Input Voltage	$V_{IN(0)}$	V_{CC} = 5V		–	–	1.5	V
		V_{CC} = 10V		–	–	2.0	V
Logical “1” Output Voltage	$V_{OUT(1)}$	V_{CC} = 5V	I_O = −10μA	4.5	–	–	V
		V_{CC} = 10V		9.0	–	–	V
Logical “0” Output Voltage	$V_{OUT(0)}$	V_{CC} = 5V	I_O = 10μA	–	–	0.5	V
		V_{CC} = 10V		–	–	1.0	V
Logical “1” Input Current	$I_{IN(1)}$	V_{CC} = 15V, V_{IN} = 15V		–	0.005	1.0	μA
Logical “0” Input Current	$I_{IN(0)}$	V_{CC} = 15V, V_{IN} = 0V		–1.0	–0.005	–	μA
Supply Current	I_{CC}	V_{CC} = 15V		–	0.05	300	μA
CMOS/LPTTL Interface							
Logical “1” Input Voltage	$V_{IN(1)}$	V_{CC} = 4.75V		V_{CC}–1.5	–	–	V
Logical “0” Input Voltage	$V_{IN(0)}$	V_{CC} = 4.75V		–	–	0.8	V
Logical “1” Output Voltage	$V_{OUT(1)}$	V_{CC} = 4.75V, I_O = −360μA		2.4	–	–	V
Logical “0” Output Voltage	$V_{OUT(0)}$	V_{CC} = 4.75V, I_O = 360μA		–	–	0.4	V
Output Drive							
Output Source Current (P−Channel)	I_{SOURCE}	V_{CC} = 5V	V_{OUT} = 0, T_A = +25°C	–1.75	–3.3	–	mA
		V_{CC} = 10V		–8	–15	–	mA
Output Sink Current (N−Channel)	I_{SINK}	V_{CC} = 5V	V_{OUT} = V_{CC}, T_A = +25°C	1.75	3.6	–	mA
		V_{CC} = 10V		8	16	–	mA

AC Electrical Characteristics: (T_A = +25°, C_L = 50pF, Note 2 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time to a Logical “0” or Logical “1” from Clock to Q or $\overline{Q}$	t_{pd}	V_{CC} = 5V	–	190	300	ns
		V_{CC} = 10V	–	75	110	ns
Propagation Delay Time to a Logical “0” from Clear to Q	t_{pd}	V_{CC} = 5V	–	180	300	ns
		V_{CC} = 10V	–	70	110	ns
Propagation Delay Time to a Logical “1” from Clear to Q	t_{pd}	V_{CC} = 5V	–	230	400	ns
		V_{CC} = 10V	–	90	150	ns
Time Prior to Clock Pulse that Data Must be Present	t_S	V_{CC} = 5V	100	45	–	ns
		V_{CC} = 10V	40	16	–	ns
Time After Clock Pulse that Data Must be Held	t_H	V_{CC} = 5V	0	–11	–	ns
		V_{CC} = 10V	0	–4	–	ns
Minimum Clock Pulse Width	t_W	V_{CC} = 5V	–	130	250	ns
		V_{CC} = 10V	–	45	100	ns
Minimum Clear Pulse Width	t_W	V_{CC} = 5V	–	120	250	ns
		V_{CC} = 10V	–	45	100	ns
Maximum Clock Rise Time	t_r	V_{CC} = 5V	15	450	–	μs
		V_{CC} = 10V	5	125	–	μs

Note 2. AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics (Cont'd): (T_A = +25°, C_L = 50pF, Note 2 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Fall Time	t_f	V_{CC} = 5V	15	50	–	µs
		V_{CC} = 10V	5	50	–	µs
Maximum Clock Frequency	f_{MAX}	V_{CC} = 5V	2.0	3.5	–	MHz
		V_{CC} = 10V	5.0	10.0	–	MHz
Input Capacitance	C_{IN}	Clear Input, Note 3	–	10	–	pF
		Any Other Input	–	5	–	pF
Power Dissipation Capacitance	C_{pd}	Per Package, Note 4	–	130	–	pF

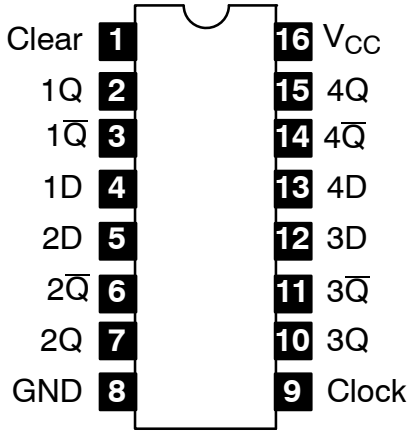
Note 2. AC Parameters are guaranteed by DC correlated testing.
Note 3. Capacitance is guaranteed by periodic testing.
Note 4. C_{pd} determines the no load AC power consumption of any CMOS device.

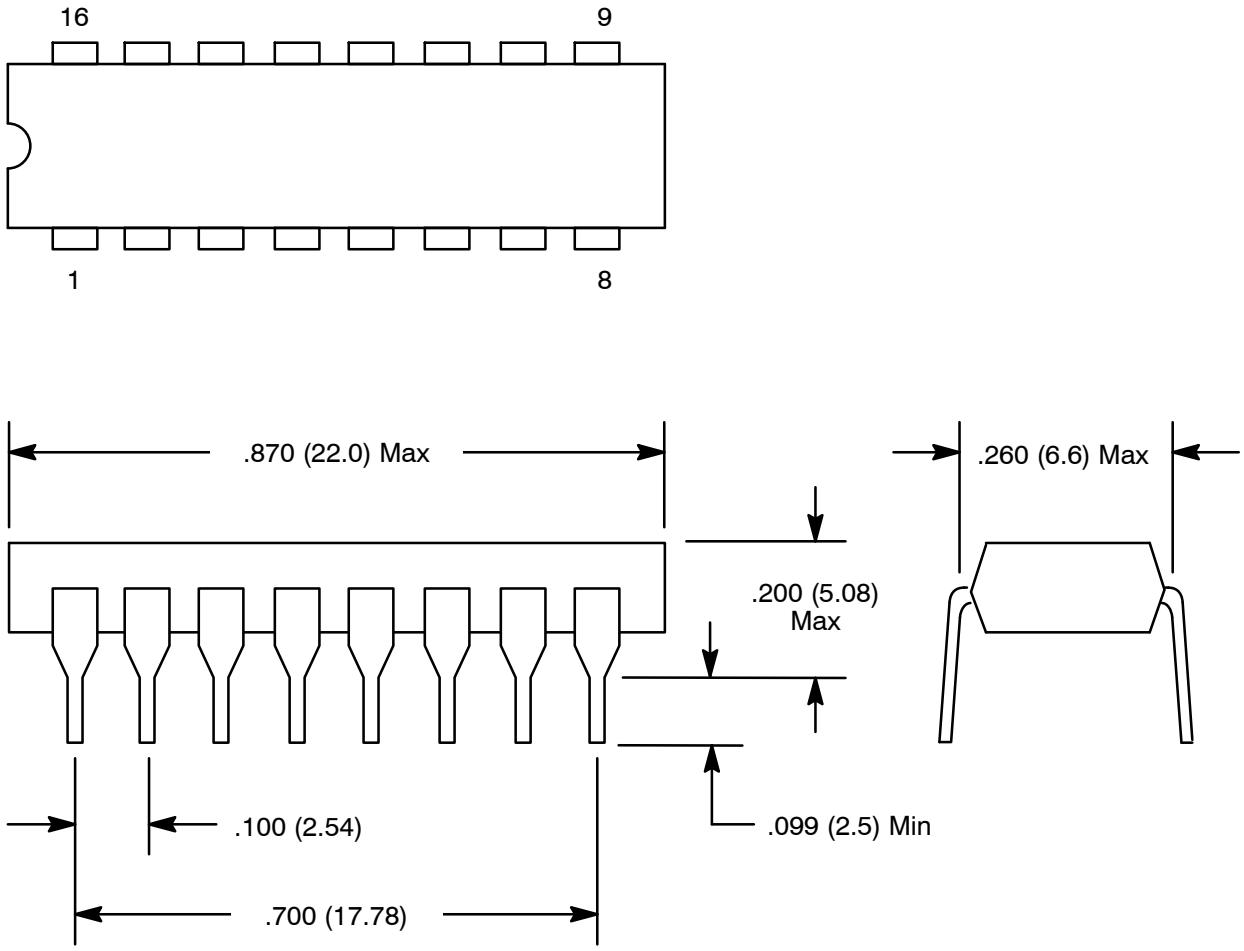
Truth Table (Each Flip−Flop):

Inputs			Outputs	
Clear	**Clock**	**D**	**Q**	**$\overline{Q}$**
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	H	X	NC	NC
H	L	X	NC	NC

H = High Level
L = Low Level
X = Irrelevant
↑ = Transition from Low to High Level
NC = No Change

Pin Connection Diagram




16
9
1
8
.870 (22.0) Max
.260 (6.6) Max
.200 (5.08)
Max
.100 (2.54)
.099 (2.5) Min
.700 (17.78)