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NTE4541B and NTE4541BT
Integrated Circuit
CMOS, Programmable Timer

Description:

The NTE4541B (14–Lead DIP) and NTE4541BT (SOIC–14) programmable timers consist of a 10–stage binary counter, an integrated oscillator for use with an external capacitor and two resistors, an automatic power–on reset circuit, and output control logic.

Timing is initialized by turning on power, whereupon the power–on reset is enabled and initializes the counter, within the specified V_{DD} range. With the power already on, an external reset pulse can be applied. Upon release of the initial reset command, the oscillator will oscillate with a frequency determined by the external RC network. For 16–stage counter divides the oscillator frequency (f_{OSC}) with the n^{th} stage frequency being $f_{OSC}/2^n$.

Features:

- Available Outputs 2^8, 2^{10}, 2^{13}, or 2^{16}
- Increments on Positive Edge Clock Transitions
- Low Symmetrical Output Resistance (Typically 10Ω at 15Vdc)
- Built–In Low Power RC Oscillatior
  (±2% Accuracy over Temperature Range and ±10% Supply and ±3% over Processing at < 10kHz)
- Oscillator Frequency Range ≈ DC to 100kHz
- Oscillator may be Bypassed if External Clock is Available (Apply External Clock to Pin3)
- Automatic Reset Initializes All Counters when Power Turn On
  (Limits – V_{DD} from 8.5Vdc to 18Vdc when Enabled)
- External Master Reset Totally Independent of Automatic Reset Operation
- Operates as 2^n Frequency Divider or Single Transition Timer
- Q/Q Select Provides Output Logic Level Flexibility
- Reset (Auto or Master) Disables Oscillator during Resetting to Provide No Active Power Dissipation
- Clock Conditioning Circuit Permits Operation with Very Slow Clock Rise and Fall Times
- Supply Voltage Range = 3Vdc to 18Vdc

Absolute Maximum Ratings: (Voltages Referenced to V_{SS})

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (All Inputs), V_{in} . . . . . –0.5 to V_{DD} + 0.5V
DC Current Drain (Per Pin), I 45mA
Operating Temperature Range, T_A . . . . . –55 to +125°C
Storage Temperature Range, T_{stg} . . . . . –65 to +150°C

Electrical Characteristics: (Note 1)

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage “0” Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
“1” Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage (Note 3) “0” Level	V_{IL}									
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
“1” Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current Source	I_{OH}									
(V_{OH} = 2.5Vdc)		5.0	7.96	–	6.42	12.83	–	4.49	–	mAdc
(V_{OH} = 9.5Vdc)		10	4.19	–	3.38	6.75	–	2.37	–	mAdc
(V_{OH} = 13.5Vdc)		15	16.3	–	13.2	26.33	–	9.24	–	mAdc
Sink	I_{OL}									
(V_{OL} = 0.4Vdc)		5.0	1.93	–	1.56	3.12	–	1.09	–	mAdc
(V_{OL} = 0.5Vdc)		10	4.96	–	4.0	8.0	–	2.5	–	mAdc
(V_{OL} = 1.5Vdc)		15	19.3	–	15.6	31.2	–	10.9	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	μAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Pin5 is High)		10	–	10	–	0.010	10	–	300	μAdc
Auto Reset Disabled		15	–	20	–	0.015	20	–	600	μAdc
Auto Reset Quiescent Current	I_{DDR}	5.0	–	200	–	7	200	–	1200	μAdc
(Pin5 is Low)		10	–	250	–	30	250	–	1500	μAdc
		15	–	500	–	82	500	–	2000	μAdc
Total Supply Current	I_T	5.0	I_D = (0.4μA/kHz) f + I_{DD}							μAdc
(Dynamic plus Quiescent,		10	I_D = (0.8μA/kHz) f + I_{DD}							μAdc
Note 2, Note 4)		15	I_D = (1.2μA/kHz) f + I_{DD}							μAdc

Note 1. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 2. The formulas given are for the typical characteristics only at +25°C.

Note 3. Noise immunity specified for worst−case input combination.
Noise margin for both “1” and “0” = 1.0Vdc min @ V_{DD} = 5Vdc
2.0Vdc min @ V_{DD} = 10Vdc
2.5Vdc min @ V_{DD} = 15Vdc

Note 4. When using the on−chip oscillator the total supply current (in μAdc) becomes:

$$I_T - I_D + 2\ C_{tc}\ V_{DD} f \times 10^{-3}$$

where I_D is in μA, C_{tc} is in pF, V_{DD} in Vdc, and f in kHz.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					
t_{TLH} = (3.0ns/pF) C_L + 30ns		5.0	–	180	360	ns
t_{TLH} = (1.5ns/pF) C_L + 15ns		10	–	90	180	ns
t_{TLH} = (1.1ns/pF) C_L + 10ns		15	–	65	130	ns
Output Fall Time	t_{THL}					
t_{THL} = (1.5ns/pF) C_L + 25ns		5.0	–	100	200	ns
t_{THL} = (0.75ns/pF) C_L + 12.5ns		10	–	50	100	ns
t_{THL} = (0.55ns/pF) C_L + 9.5ns		15	–	40	80	ns
Turn−Off, Turn−On Clock to Q (2^8 Output)	t_{PLH}, t_{PHL}					
t_{PLH}, t_{PHL} = (1.7ns/pF) C_L + 3415ns		5.0	–	3.5	10.5	μs
t_{PLH}, t_{PHL} = (0.66ns/pF) C_L + 1217ns		10	–	1.25	3.8	μs
t_{PLH}, t_{PHL} = (0.5ns/pF) C_L + 875ns		15	–	0.9	2.9	μs
Turn−Off, Turn−On Clock to Q (2^{16} Output)	t_{PLH}, t_{PHL}					
t_{PLH}, t_{PHL} = (1.7ns/pF) C_L + 5915ns		5.0	–	6.0	18	μs
t_{PLH}, t_{PHL} = (0.66ns/pF) C_L + 3467ns		10	–	3.5	10	μs
t_{PLH}, t_{PHL} = (0.5ns/pF) C_L + 2475ns		15	–	2.5	7.5	μs
Clock Pulse Width	$t_{WH(cl)}$	5.0	900	300	–	ns
		10	300	100	–	ns
		15	225	85	–	ns
Clock Pulse Frequency	f_{cl}	5.0	–	1.5	–	MHz
		10	–	4.0	–	MHz
		15	–	6.0	–	MHz
MR Pulse Width	$t_{WH(R)}$	5.0	900	300	–	ns
		10	300	100	–	ns
		15	225	85	–	ns

Note 2. The formulas given are for the typical characteristics only at +25°C.

Frequency Selection Table

A	B	Number of Counter Stages n	Count 2^0
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

Truth Table

Pin	Stage	
	0	1
5	Auto Reset Operating	Auto Reset Disabled
6	Timer Operational	Master Reset On
9	Output Initially Low after Reset	Output Initially High after Reset
10	Single Cycle Mode	Recycle Mode

Operating Characteristics:

With Auto Reset pin set to a “0” the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a “1”. Both types of reset will result in synchronously resetting all counter stages independent of counter state. Auto Reset pin set to a “1” provides a lo power operation.

The RC oscillator will oscillate with a frequency determined by the external RC network i.e.,

$$f = \frac{1}{2.3\ R_{tc}C_{tc}} \qquad \text{If } (1\text{kHz} \le f \le 100\text{kHz})$$

and $R_S \approx 2\ R_{tc}$ where $R_S \ge 10\text{k}\Omega$

The time select inputs (A and B) provide a two−bit address to output any one or four counter stages (2^8, 2^{10}, 2^{13} and 2^{16}). The 2^n counts as shown in the Frequency Selection Table represents the Q output of the N^{th} stage of the counter. When A is “1”, 2^{16} is selected for both states of B. However, when B is “0”, normal counting is interrupted and the 9^{th} counter stage receives its clock directly from the oscillator (i.e., effectively outputting 2^8).

The Q/$\overline{Q}$ select output control pin provides for a choice of output level. When the counter is in a reset condition and Q/$\overline{Q}$ select pin is set to a “0” the Q output is a “0”, correspondingly when Q/$\overline{Q}$ select pin is set to a “1” the Q output is a “1”.

When the mode control pin is set to a “1”, the selected count is continually transmitted to the output. But, with mode pin “0” and after a reset condition the RS flip−flop resets, counting commenced and after 2^{n-1} counts the RS flip−flop sets which causes the output to change state. Hence, after another 2^{n-1} counts the output will not change. Thus, a Master Reset pulse must b applied or a change in the mode pin level is required to reset the single cycle operation.

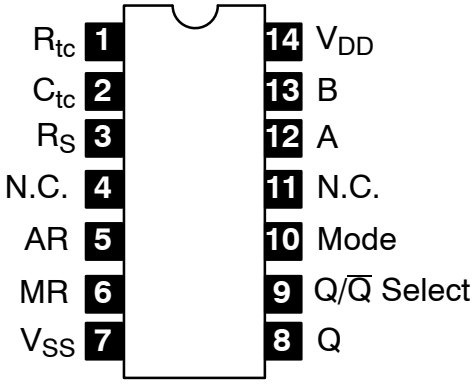
Digital Timer Application:

When Master Reset (MR) receives a positive pulse, the internal counters and latch are reset. The Q output goes high and remains high until the selected (via A and B) number of clock pulses are counted, the Q output then goes low and remains low until another input pulse is received.

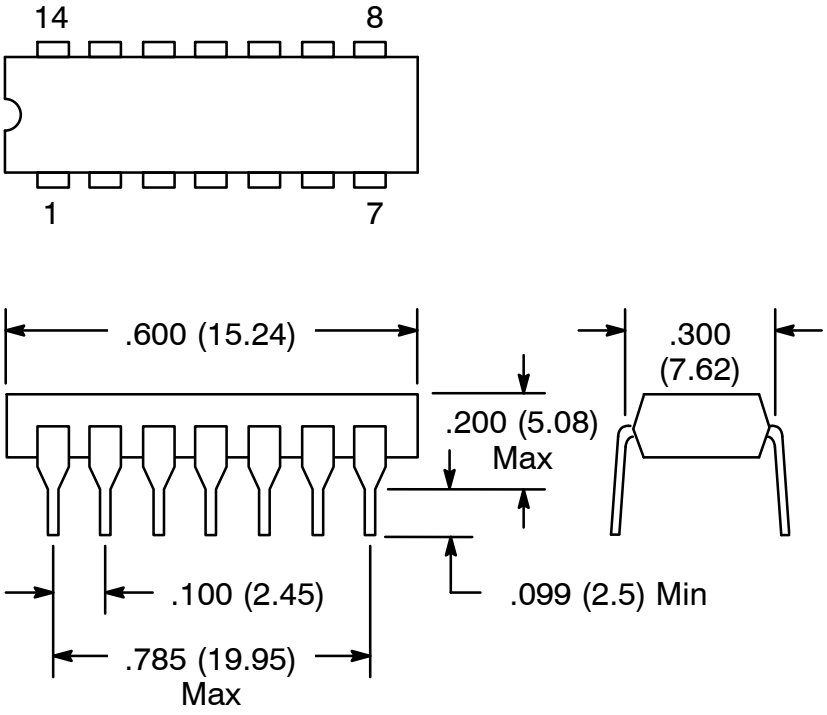
The “one shot” is fully retriggerable and as accurate as the input frequency. An external clock can be used (Pin3 is the clock input, Pin1 and Pin2 are outputs) if additional accuracy is needed.

Notice hat a setup time equal to the desired pulse with output is required immediately following initial power up, during which time Q output will be high.

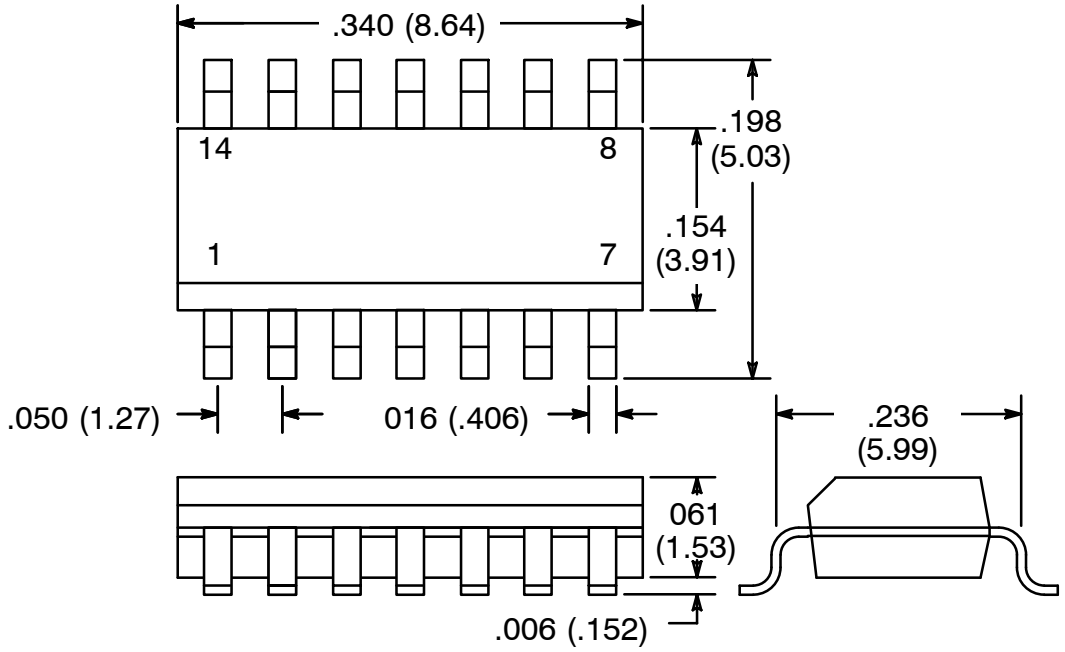
Pin Connection Diagram



NTE4541B



NTE4541BT



NOTE: Pin1 on Beveled Edge