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NTE4532B
Integrated Circuit
CMOS, 8-Bit Priority Encoder

Description:

The NTE4532B is an 8-bit priority encoder in a 16-Lead DIP type package constructed with complementary MOS (CMOS) enhancement mode devices. The primary function of the priority encoder is to provide a binary address for the active input with the highest priority. Eight data inputs (Do thru D7) and an enable input E_{in}) are provided. Five outputs are available, three are address outputs (Q0 thru Q2), one group select (GS) and one enable output (E_{out}).

Features:

- Quiescent Current = 5nA/Package (Typ) at 5Vdc
- Noise Immunity = 45% of V_{DD} (Typ)
- Diode Protection on All Inputs
- Low Input Capacitance - 5pF (Typ)
- Supply Voltage Range: 3Vdc to 18Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

Absolute Maximum Ratings: (Voltages referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . −0.5 to +18.0V
Input Voltage (All Inputs), V_{in} . . . . −0.5 to V_{DD} to +0.5V
DC Current Drain (Per Pin), I 10mA
Operating Temperature Range, T_A . . . . −55° to +125°C
Storage Temperature Range, T_{stg} . . . . −65° to +150°C

Note 1. This device contains circuitry to protect the input against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Electrical Characteristics: (Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level $V_{in} = 0$ or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage (Note 4) "0" Level (V_O = 4.5 or 0.5Vdc)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 123.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
"1" Level (V_O = 0.5 or 4.5Vdc)	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current Source (V_{OH} = 2.5Vdc)	I_{OH}	5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	mAdc
(V_{OH} = 4.6Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	mAdc
(V_{OH} = 9.5Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	mAdc
(V_{OH} = 13.5Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	mAdc
Sink (V_{OL} = 0.4Vdc)	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	µAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	µAdc
		15	–	20	–	0.015	20	–	600	µAdc
Total Supply Current (Dynamic plus Quiescent, Per Package, C_L = 50pF on all outputs, all buffers switching, Note 3, Note 5)	I_T	5.0	I_T = (1.74µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.65µA/kHz) f + I_{DD}							µAdc
		15	I_T = (5.73µA/kHz) f + I_{DD}							µAdc

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. Noise immunity specified for worst−case input combination.
Noise margin for both "1" and "0" = 1.0Vdc min @ V_{DD} = 5Vdc
2.0Vdc min @ V_{DD} = 10Vdc
2.5Vdc min @ V_{DD} = 15Vdc

Note 5. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + 5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, f in kHz is input frequency.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					
t_{TLH} = (3.0ns/pf) C_L + 30ns		5.0	–	180	360	ns
t_{TLH} = (1.5ns/pf) C_L + 15ns		10	–	90	180	ns
t_{TLH} = (1.1ns/pf) C_L + 10ns		15	–	65	130	ns
Output Fall Time	t_{THL}					
t_{THL} = (1.5ns/pf) C_L + 25ns		5.0	–	100	200	ns
t_{THL} = (0.75ns/pf) C_L + 12.5ns		10	–	50	100	ns
t_{THL} = (0.55ns/pf) C_L + 9.5ns		15	–	40	80	ns
Propagation Delay Time, E_{in} to E_{out}	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7ns/pF) C_L + 120ns	t_{PHL}	5.0	–	205	410	
t_{PLH}, t_{PHL} = (0.66ns/pF) C_L + 77ns		10	–	110	220	ns
t_{PLH}, t_{PHL} = (0.5ns/pF) C_L + 55ns		15	–	80	160	ns
Propagation Delay Time, E_{in} to GS	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7ns/pF) C_L + 90ns	t_{PHL}	5.0	–	175	350	
t_{PLH}, t_{PHL} = (0.66ns/pF) C_L + 57ns		10	–	90	180	ns
t_{PLH}, t_{PHL} = (0.5ns/pF) C_L + 40ns		15	–	65	130	ns
Propagation Delay Time, E_{in} to Q_n	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7ns/pF) C_L + 195ns	t_{PHL}	5.0	–	280	560	
t_{PLH}, t_{PHL} = (0.66ns/pF) C_L + 107ns		10	–	140	280	ns
t_{PLH}, t_{PHL} = (0.5ns/pF) C_L + 75ns		15	–	100	200	ns
Propagation Delay Time, D_n to Q_n	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7ns/pF) C_L + 265ns	t_{PHL}	5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.66ns/pF) C_L + 137ns		10	–	170	340	ns
t_{PLH}, t_{PHL} = (0.5ns/pF) C_L + 85ns		15	–	110	220	ns
Propagation Delay Time, D_n to GS	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7ns/pF) C_L + 195ns	t_{PHL}	5.0	–	280	560	
t_{PLH}, t_{PHL} = (0.66ns/pF) C_L + 107ns		10	–	140	280	ns
t_{PLH}, t_{PHL} = (0.5ns/pF) C_L + 75ns		15	–	100	200	ns

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Truth Table

Input									Output				
E_{in}	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E_{out}
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	1	0	0
1	0	0	0	0	0	0	1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care

Pin Connection Diagram